

BC856ALT1 Series

Preferred Devices

General Purpose Transistors

PNP Silicon

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BC856 BC857 BC858, BC859	V_{CEO}	-65 -45 -30	V
Collector-Base Voltage BC856 BC857 BC858, BC859	V_{CBO}	-80 -50 -30	V
Emitter-Base Voltage	V_{EBO}	-5.0	V
Collector Current – Continuous	I_C	-100	mAdc

THERMAL CHARACTERISTICS

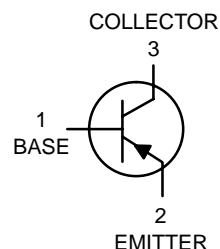
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

- FR-5 = 1.0 x 0.75 x 0.062 in
- Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

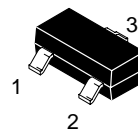


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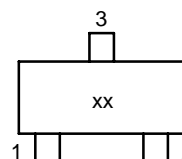
<http://onsemi.com>



MARKING DIAGRAM



SOT-23
CASE 318
STYLE 6



xx = Device Code
(See Table Below)

ORDERING INFORMATION

Device	Package	Mark	Shipping
BC856ALT1	SOT-23	3A	3000/Tape & Reel
BC856BLT1	SOT-23	3B	3000/Tape & Reel
BC857ALT1	SOT-23	3E	3000/Tape & Reel
BC857BLT1	SOT-23	3F	3000/Tape & Reel
BC858ALT1	SOT-23	3J	3000/Tape & Reel
BC858BLT1	SOT-23	3K	3000/Tape & Reel
BC858CLT1	SOT-23	3L	3000/Tape & Reel
BC859BLT1	SOT-23	4B	3000/Tape & Reel
BC859CLT1	SOT-23	4C	3000/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

BC856ALT1 Series

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage ($I_C = -10\text{ mA}$)	BC856 Series BC857 Series BC858, BC859 Series	$V_{(BR)CEO}$	-65 -45 -30	- - -	- - -	V
Collector–Emitter Breakdown Voltage ($I_C = -10\ \mu\text{A}$, $V_{EB} = 0$)	BC856 Series BC857 Series BC858, BC859 Series	$V_{(BR)CES}$	-80 -50 -30	- - -	- - -	V
Collector–Base Breakdown Voltage ($I_C = -10\ \mu\text{A}$)	BC856 Series BC857 Series BC858, BC859 Series	$V_{(BR)CBO}$	-80 -50 -30	- - -	- - -	V
Emitter–Base Breakdown Voltage ($I_E = -1.0\ \mu\text{A}$)	BC856 Series BC857 Series BC858, BC859 Series	$V_{(BR)EBO}$	-5.0 -5.0 -5.0	- - -	- - -	V
Collector Cutoff Current ($V_{CB} = -30\text{ V}$) ($V_{CB} = -30\text{ V}$, $T_A = 150^\circ\text{C}$)		I_{CBO}	- -	- -	-15 -4.0	nA μA

ON CHARACTERISTICS

DC Current Gain ($I_C = -10\ \mu\text{A}$, $V_{CE} = -5.0\text{ V}$)	BC856A, BC857A, BC858A BC856B, BC857B, BC858B BC858C	h_{FE}	- - -	90 150 270	- - -	-
($I_C = -2.0\text{ mA}$, $V_{CE} = -5.0\text{ V}$)	BC856A, BC857A, BC858A BC856B, BC857B, BC858B, BC859B BC858C, BC859C		125 220 420	180 290 520	250 475 800	
Collector–Emitter Saturation Voltage ($I_C = -10\text{ mA}$, $I_B = -0.5\text{ mA}$) ($I_C = -100\text{ mA}$, $I_B = -5.0\text{ mA}$)		$V_{CE(sat)}$	- -	- -	-0.3 -0.65	V
Base–Emitter Saturation Voltage ($I_C = -10\text{ mA}$, $I_B = -0.5\text{ mA}$) ($I_C = -100\text{ mA}$, $I_B = -5.0\text{ mA}$)		$V_{BE(sat)}$	- -	-0.7 -0.9	- -	V
Base–Emitter On Voltage ($I_C = -2.0\text{ mA}$, $V_{CE} = -5.0\text{ V}$) ($I_C = -10\text{ mA}$, $V_{CE} = -5.0\text{ V}$)		$V_{BE(on)}$	-0.6 -	- -	-0.75 -0.82	V

SMALL–SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product ($I_C = -10\text{ mA}$, $V_{CE} = -5.0\text{ Vdc}$, $f = 100\text{ MHz}$)		f_T	100	-	-	MHz
Output Capacitance ($V_{CB} = -10\text{ V}$, $f = 1.0\text{ MHz}$)		C_{ob}	-	-	4.5	pF
Noise Figure ($I_C = -0.2\text{ mA}$, $V_{CE} = -5.0\text{ Vdc}$, $R_S = 2.0\text{ k}\Omega$, $f = 1.0\text{ kHz}$, $BW = 200\text{ Hz}$)	BC856, BC857, BC858 Series BC859 Series	NF	- -	- -	10 4.0	dB

BC856ALT1 Series

BC857/BC858/BC859

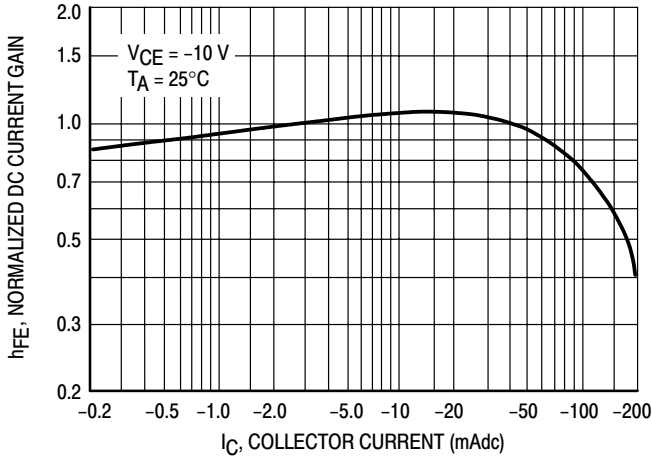


Figure 1. Normalized DC Current Gain

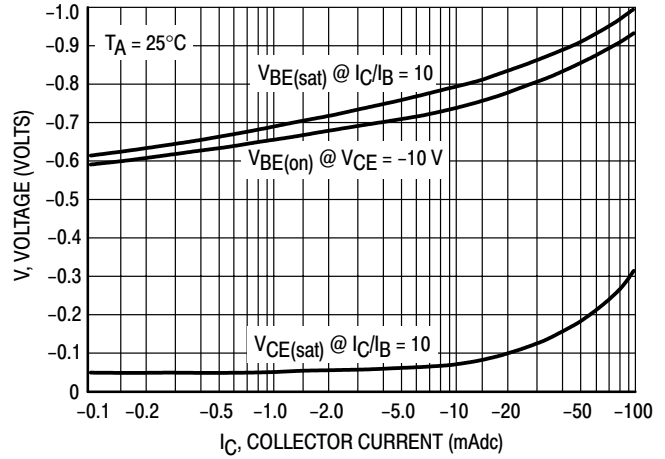


Figure 2. "Saturation" and "On" Voltages

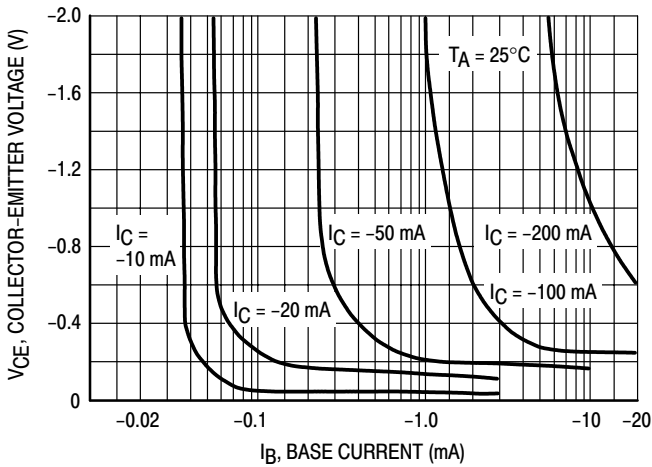


Figure 3. Collector Saturation Region

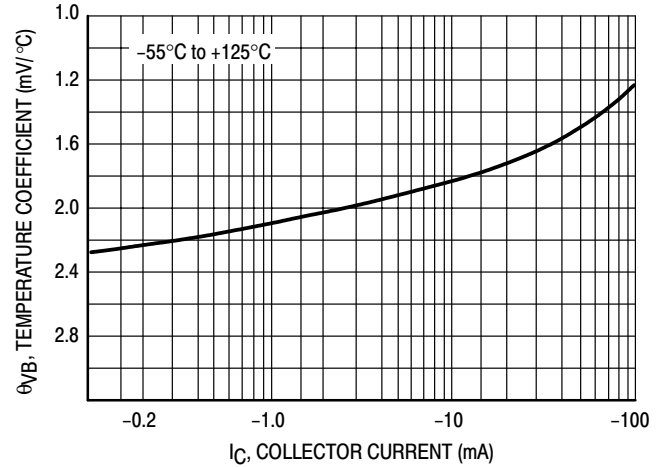


Figure 4. Base-Emitter Temperature Coefficient

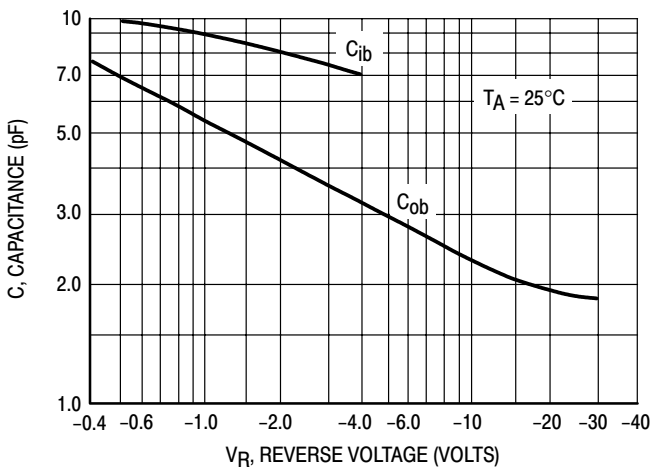


Figure 5. Capacitances

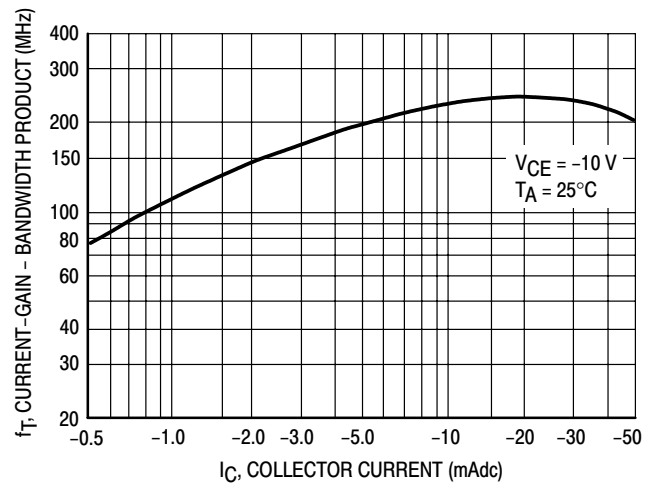


Figure 6. Current-Gain - Bandwidth Product

BC856ALT1 Series

BC856

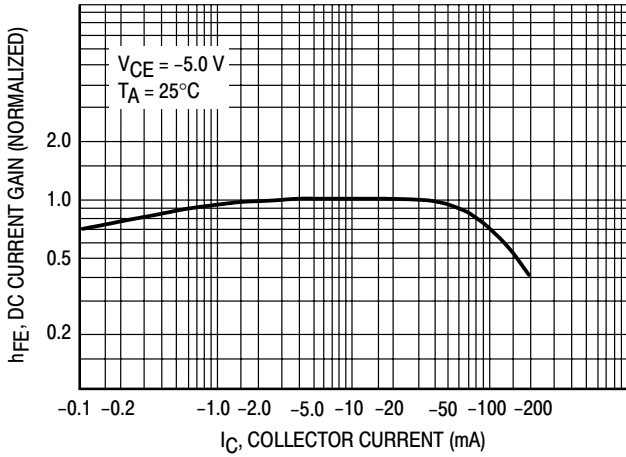


Figure 7. DC Current Gain

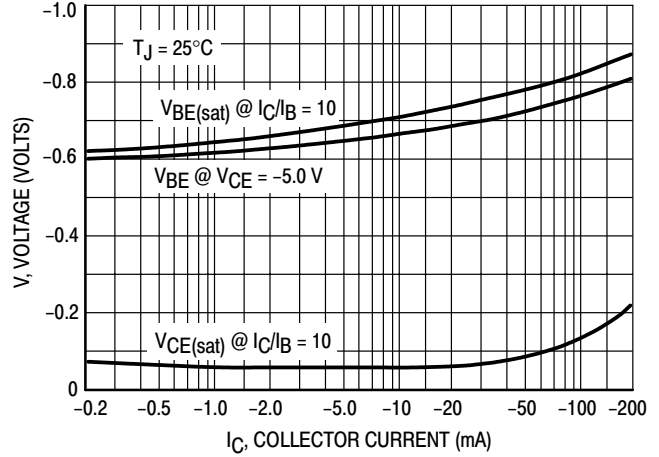


Figure 8. "On" Voltage

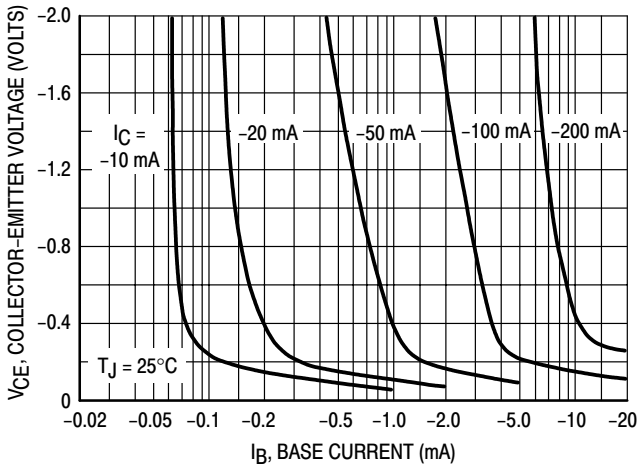


Figure 9. Collector Saturation Region

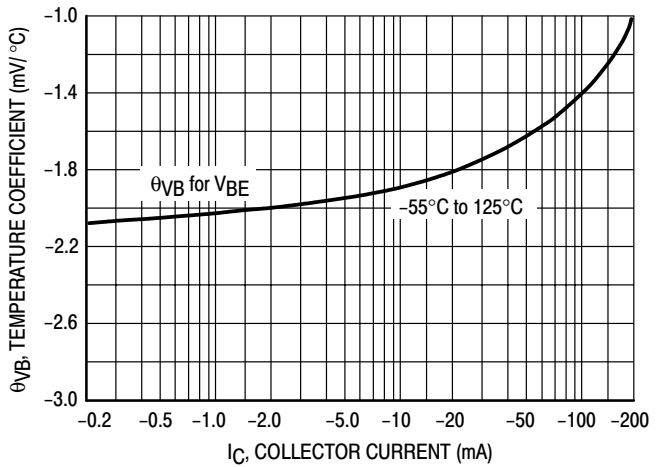


Figure 10. Base-Emitter Temperature Coefficient

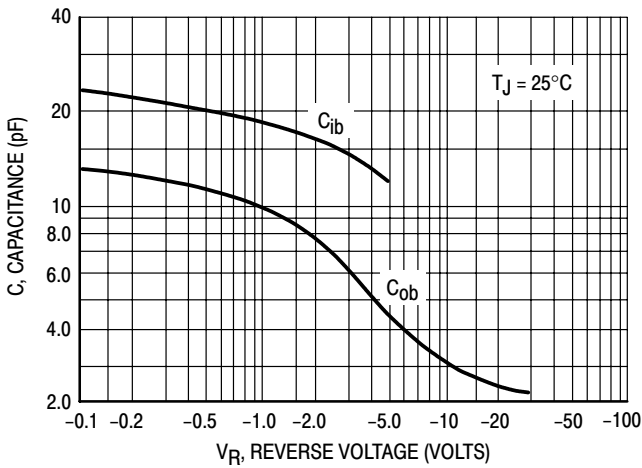


Figure 11. Capacitance

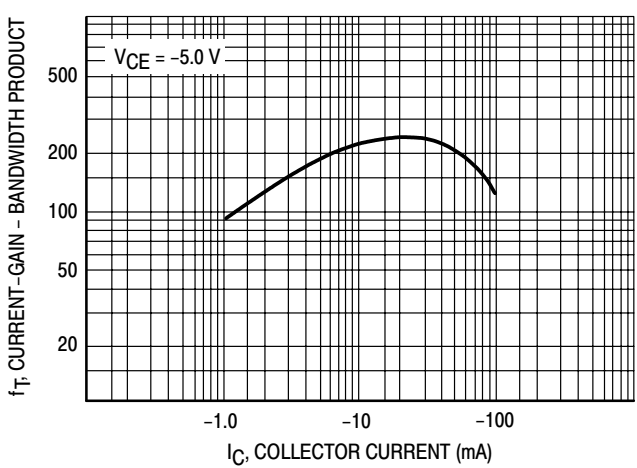


Figure 12. Current-Gain - Bandwidth Product

BC856ALT1 Series

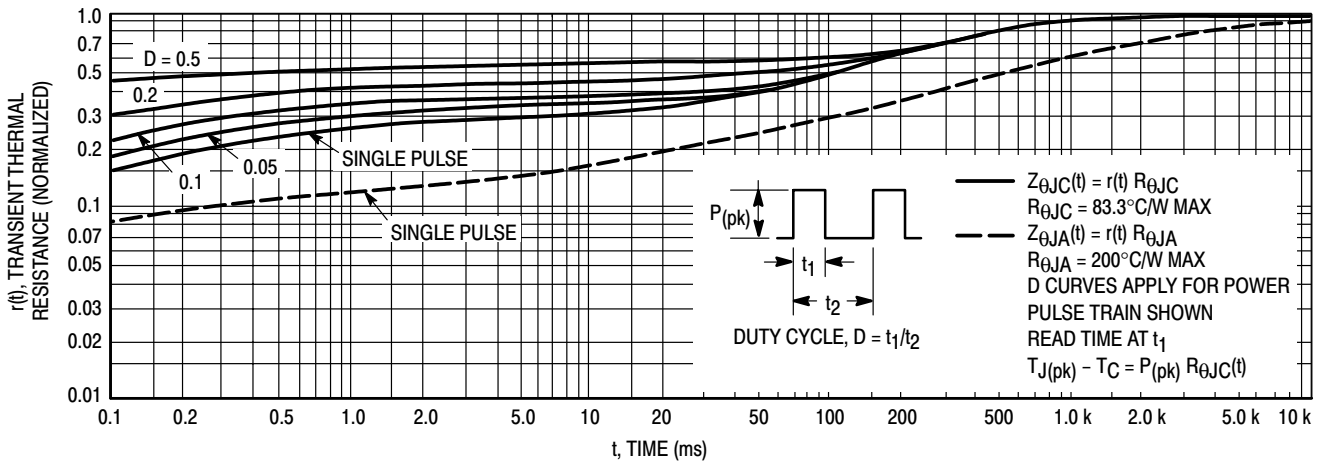


Figure 13. Thermal Response

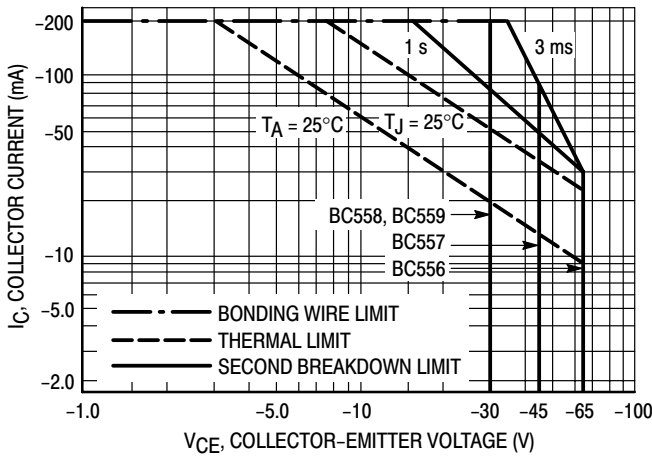


Figure 14. Active Region Safe Operating Area

The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

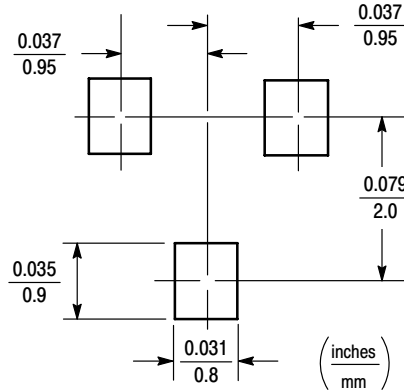
The data of Figure 14 is based upon $T_{J(pk)} = 150^{\circ}C$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

SOT-23 POWER DISSIPATION

The power dissipation of the SOT-23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT-23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{556^\circ\text{C/W}} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

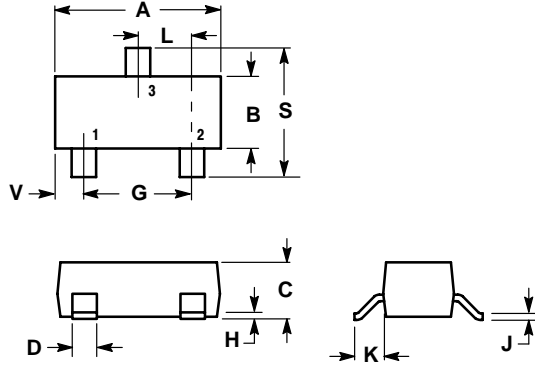
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

BC856ALT1 Series

PACKAGE DIMENSIONS

SOT-23
TO-236AB
CASE 318-08
ISSUE AF



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:

- PIN 1. BASE
2. EMITTER
3. COLLECTOR

BC856ALT1 Series

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