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FUJITSU

DATA SHEET

CG51/CE51 SERIES

3V, 0.50 MICRON HIGH PERFORMANCE/LOW POWER CMOS GATE ARRAYS

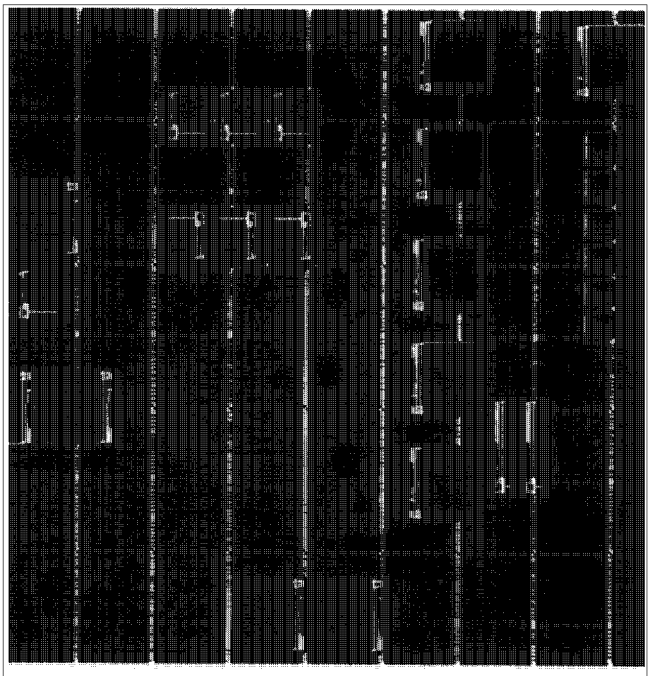
DESCRIPTION

The Fujitsu CG51/CE51 is a series of ultra high performance CMOS gate arrays. The CG51 is a high density Sea-of-Gates array for applications requiring high levels of integration or low power. The CE51 is a high performance embedded gate array family offering full support of diffused high speed RAMS, ROMS and embedded megafunctions. The CE51 series offers density and performance approaching that achievable with standard cell solutions with the time-to-market advantage of a gate array.

True 3V products, the CG51/CE51 feature very low power (1.2 microwatt/Mhz) and both 3.3V and 5.0V compatible I/Os. These advanced product families are targeted at users who are seeking very high performance or very high levels of integration. Potential end-user applications include computers, supercomputers, workstations, graphic terminals, telecom networking, and signal processing.

FEATURES

- 0.5 Micron Drawn Channel Length
- Triple layer metal
- 3.3V $\pm$ 0.3V supply voltage
- Chanelless, Sea-of-gates Architecture
- Internal gate delay of 210ps, F/O = 2, L = 1mm
- Low power consumption: 1.2 microwatt/gate/Mhz
- Maximum toggle frequency: 600Mhz
- High speed I/Os: PCML (PECL), LVTC
- Supports 3.3V and 5.0V I/O
- RAM compiler supports Single/Dual/Triple port RAM
- Supports JTAG boundary scan, full and partial scan
- Phase Locked Loop for interchip clock skew control
- Clock net for optimized on-chip clock skew control
- Advanced packaging options include QFP, PGA, BGA, and MCM
- High drive capability: 2, 4, 8, 12, or 24mA
- Supports all major third party EDA tools including: Cadence, Mentor, Synopsys



Fujitsu Microelectronics, Inc.'s CE51654 647,000 Available Gate .5 Micron Embedded Array, Containing 28 Embedded Macro Cells

PRODUCT SUMMARY

Device Name	Available Gates	Number of Pads	Metal Wiring
CG51754	753,768	496	3LM
CG51654	647,948	456	3LM
CG51484	477,632	400	3LM
CG51364	363,084	352	3LM
CG51284	277,380	304	3LM
CG51214	214,760	272	3LM
CG51164	160,140	240	3LM
CG51114	113,520	208	3LM
CG51343	34,272	120	3LM

DC CHARACTERISTICS

Measuring conditions: V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_j = –0 to 100°C

Parameter	Symbol	Test Conditions			Requirements Min.	Requirements Typ.	Requirements Max.	Unit
Supply current[2]	I_{DDS}	Standby mode[1]		CG51343 to CG51214	–1.0	–	1.0	mA
				CG51284 to CG51484	–2.0	–	2.0	
				CG51654 to CG51754	–3.0	–	3.0	
High-level input voltage[3]	V_{IH}	CMOS level	Normal cell		$V_{DD} \times 0.7$	–	V_{DD}	V
			Schmitt trigger cell		$V_{DD} \times 0.8$	–	V_{DD}	
		TTL level	Normal cell		2.2	–	V_{DD}	
Low-level input voltage[3]	V_{IL}	CMOS level	Normal cell		V_{SS}	–	$V_{DD} \times 0.2$	V
			Schmitt trigger cell		V_{SS}	–	$V_{DD} \times 0.2$	
		TTL level	Normal cell		V_{SS}	–	0.8	
High-level output voltage	V_{oH}	I_{OH} = –2, –4, –8, –12, –18			V_{DD} –0.4	–	V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL} = 2, 4, 8, 12, 18			V_{SS}	0	0.4	V
Input leakage current (Tri-state pin input)[4]	I_{LI}	V_I = 0V to V_{DD}			–10	–	10	µA
	I_{LZ}				–10	–	10	
Input pull–up/ pull–down resistor[5]	R_P	Pull-up $V_I = V_{DDI}$ Pull-down V_I = 0V			20	50	140	kΩ
Output Short-circuit current[6]	I_O	**Type**	**Condition**		**$V_O = V_{DD}$**		**V_O = 0V**	mA
		Output buffer	Low power I_{OL} = 2mA		–20		+20	
			Normal I_{OL} = 4mA		–40		+40	
			Power I_{OL} = 8mA		–80		+80	
			High power I_{OL} = 12mA		–120		+120	
			Very high power I_{OL} = 24mA		–180		+180	

NOTES:

1. When $V_{IH} = V_{DD}$ and $V_{IL} = V_{SS}$, memory is in the standby mode.
2. If an input buffer with pull-up/pull-down resistor is used, the supply current may not be assured depending on the circuit configuration.
3. 5V interface is only for CMOS level.
4. If an input buffer with pull-up/pull-down resistor is used, the input leakage current may exceed the above value.
5. Either a buffer without a resistor or with a pull–up/pull–down resistor can be selected from the input and bidirectional buffers.
6. Maximum supply current at the short–circuit of output and V_{DD} or V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Requirements		Unit
Supply voltage	V_{DDE}	(External) V_{SS}* –0.5 to 6.0		V
	V_{DDI}	(Internal) V_{SS}* –0.5 to 4.0		
Input voltage	V_I	V_{SS}* –0.5 to V_{DD} +0.5		V
Output voltage	V_O	V_{SS}* –0.5 to V_{DD} +0.5		V
Storage ambient temperature	T_{ST}	Plastic –55 to +125		°C
		Ceramic –65 to +150		
Supply pin current	I_D	For one V_{DD} pin	90	mA
		For one V_{SS} pin	90	
Output current	I_O	Low power-type output buffer I_{OL} = 2 mA	±14	mA
		Normal-type output buffer I_{OL} = 4mA	±14	
		Power-type output buffer I_{OL} = 8mA	±14	
		High-power type output buffer I_{OL} = 12mA	±21	
		Very high-power type of output buffer I_{OL} = 24mA	±58	

* V_{SS} = 0V

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Requirements			Unit
			Min.	Typ.	Max.	
Supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	3.0	3.3	4.6	
High-level input voltage	CMOS level	V_{IH}	$V_{DD} \times 0.7$	–	V_{DDI}	V
	TTL level		2.2	–	V_{DDI}	
Low-level input voltage	CMOS level	V_{IL}	V_{SS}*	–	$V_{DDI} \times 0.2$	V
	TTL level		V_{SS}*	–	0.8	
Junction temperature		T_j	0	–	100	°C

* V_{SS} = 0V

THIRD PARTY EDA TOOL SUPPORTED

Fujitsu supports a third party environment allowing an ASIC designer the widest possible range of design options. Both the CG51 gate array and CE51 embedded array product families are fully supported by Fujitsu's ASIC design kits, running on leading workstations and provides a seamless link from leading third party ASIC design flows to Fujitsu's ASIC back end environment. These kits provide an easy environment for design entry, design rule checking. They also provide a complete pre- and post-layout timing back annotating capabilities. The following leading third party tools are supported.

Cadence:	Verilog-XL
Mentor:	Design Architect 8.2, Autologic I, QuickSim II
Motive:	Motive 4.2 (Static Timing Analyzer)
Sunrise Systems:	ATPG 2.1
Synopsys:	Design Analyzer 3.2a, VSS

PACKAGE OPTIONS

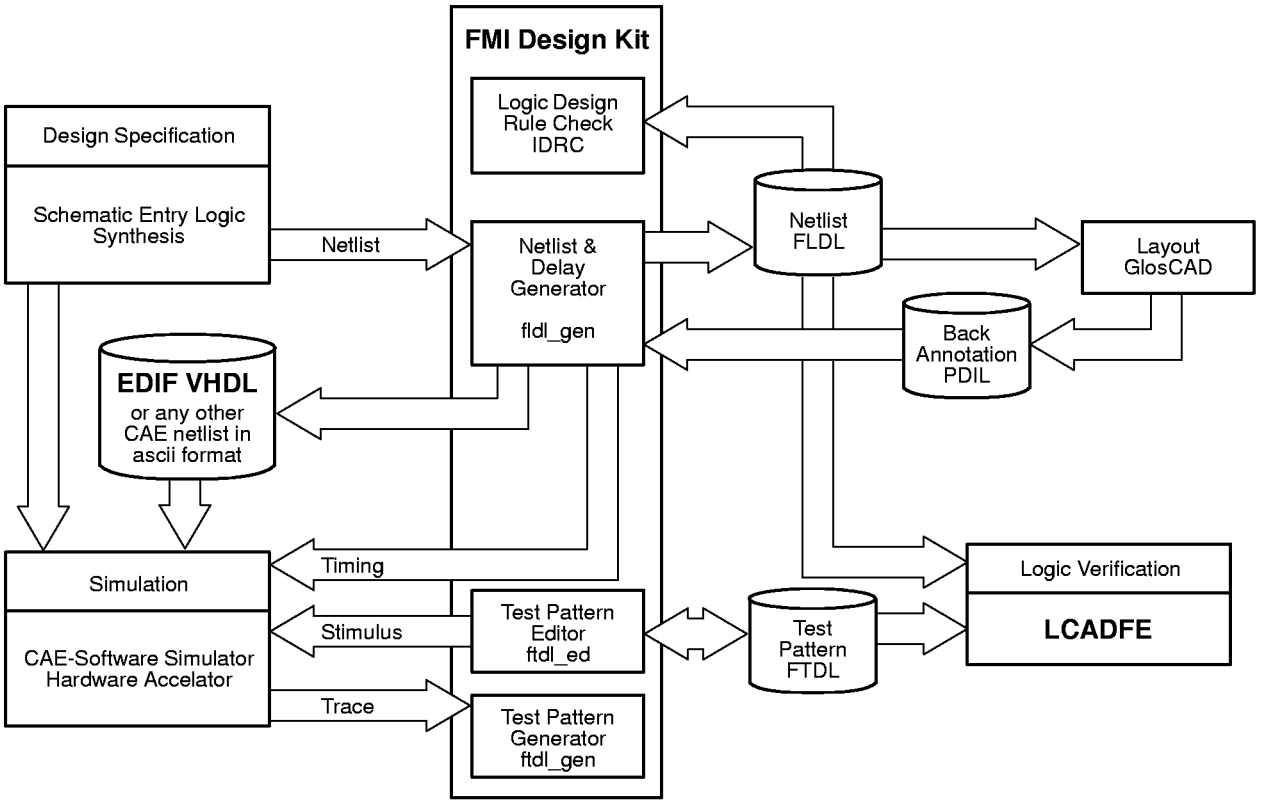
In addition to offering plastic and ceramic versions of industry standard packages such as PQFPs and PGAs, Fujitsu also offers an impressive array of advanced packaging technology. Our long experience with high speed logic and thermal management has led us to develop some of the most advanced packaging available anywhere. From cost effective, single chip packages to sophisticated multichip modules, Fujitsu has a packaging option to suit your requirements. Whether you need a 208 PQFP, the newest in high I/O count surface mounted Ball Grid Array (BGA) packages or full custom packaging we can deliver the optimal solution.

Packaging Options

	343	114	164	214	284	364	484	654	754
Quad Flat Package (1.0, 0.8, 0.65 mm pin pitch)									
100	P								
120	P								C
160		P,C	P,C	P,C	P,C	P,C	P,C	P,C	
Shrink Quad Flat Package (0.5 mm pin pitch)									
80	P								
100	P								
120	P								
144		P	P	P	P				
176		P,C	P,C	P,C	P,C	P,C			
208		P,C	P,C	P,C	P,C	P,C	P,C	P,C	
240			P,C	P,C	P,C	P,C	P,C	P,C	
256				C	P,C	P,C	P,C	P,C	
304					C1	C1	C	C	C
Fine Pitch Flat Package (0.4 mm pin pitch)									
304						C	C	C	C
Pin Grid Array Package									
256					C	C	C	C	C
299					C	C	C	C	C
321						C	C	C	C
361							C	C	C
401						C	C	C	C
Ball Grid Array (BGA)									
256			P	P	P				
352					P	P	P		
416								P1	P1
576									P1

NOTES: 1 : Under Development
C : Ceramic Package
P : Plastic Package

FRONT-END DESIGN FLOW



CLOCK SKEW CONTROL

To maximize performance in high speed, high density arrays, a designer must maintain tight clock skew control. In addition to an available PLL to manage interchip clock skew, Fujitsu's clock driven design methodology (CDDM) offers accurate on chip clock skew control. CDDM offers accurate RC extraction of clock tree parameters, interactive clock tree implementation, simplifies trade-offs between clock tree delay and clock skew, early verification of potential design hold time errors and race conditions.