DENSE-PAC MICROSYSTEMS

256Kx8 ROM/32Kx8 SRAM Combo Memory
DP50CM232

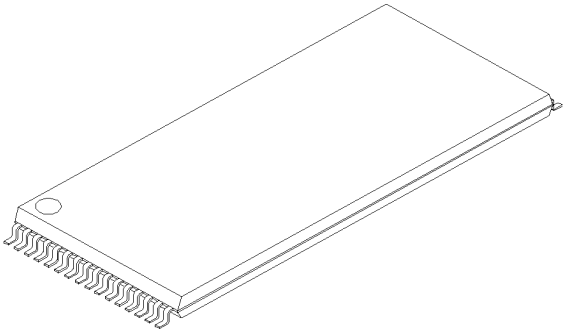
DESCRIPTION:

The DP50CM232 is a combination memory chip consist of 2M-bit Read Only Memory organized as 256K words by 8 bits and a 256K-bit Static Random Access Memory organized as 32K words by 8 bits.

The device is fabricated using Dense-Pac's advanced CMOS low power process technology.

The DP50CM232 has an output enable input for precise control of the data outputs. It also has two (2) separate chip enable inputs for selection of either RAM or ROM and minimize current drain during power-down mode.

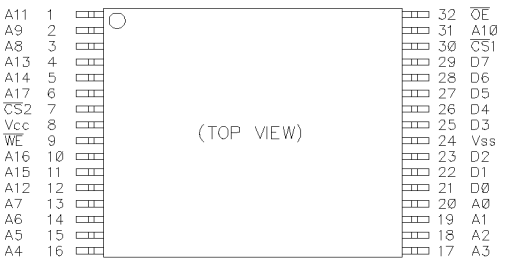
The DP50CM232 is particularly well suited for use in low voltage (1.8 - 3.3 V) operation such as pager and other hand held applications.



FEATURES:

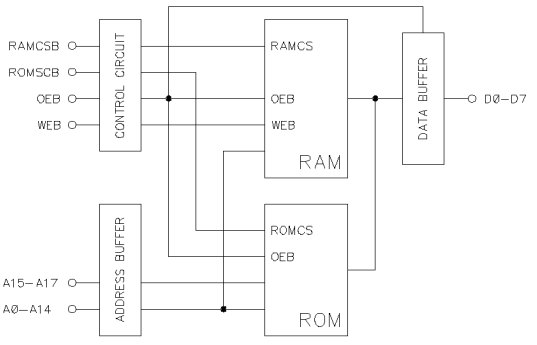
- 256Kx8 ROM and 32Kx8 SRAM
- Wide Operating Voltage Range: 1.8-3.3V
- Fast Access Times:
  - 1.8 Volt Operation: 500ns (max.)
  - 3.0 Volt Operation: 300ns (max.)
- Low Power Dissipation:
  - Standby
    - 1.8 Volt Operation: .018mW (typ.)
    - 3.0 Volt Operation: .10mW (typ.)
  - Operating
    - 1.8 Volt Operation: 1.6mW (typ.)
    - 3.0 Volt Operation: 20mW (typ.)
- Fully Static Operation
  - No clock or refresh required
- Three State Outputs
- Standard 32-pin TSOP type 1 package

PIN-OUT DIAGRAM



PIN NAMES	
A0 - A17	Address Inputs
D0 - D7	Data Input/Output
$\overline{CE}$1, ROMCSB	ROM Enable Input
$\overline{CE}$2, RAMCSB	RAM Enable Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



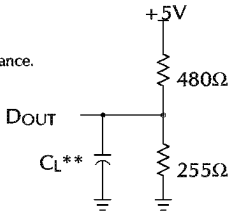
ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	Parameter	Value	Unit
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to V_{CC}+0.5	V
V_{CC}	Voltage on V_{CC} Supply Relative to V_{SS}	-0.5 to +4.0	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Operating Temperature	-20 to +70	°C
T_{SDR}	Soldering Temperature & Time	260°C, 10sec. (Lead Only)	-

RECOMMENDED OPERATING RANGE [1]					
Symbol	Characteristic		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.8	3.3	V
V_{SS}	Ground		0	0	V
V_{IH}	Input HIGH Voltage	1.8V	1.4	V_{CC}+0.5	V
		3.0V	2.4	V_{CC}+0.5	
V_{IL}	Input LOW Voltage	1.8V	-0.3	0.3	V
		3.0V	-0.3	0.3	

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Condition	Unit
C_{IN}	Input	6	V_{IN} = 0V	pF
$C_{I/O}$	Data Input/Output	8	$V_{I/O}$ = 0V	pF

TEST CONDITIONS (TA = -20 to 70°C)		
PARAMETER	VALUE	
	V_{CC} = 1.8V	V_{CC} = 3.0V
Input Pulse Levels	0V to 3.0V	0V to 3.0V
Input Pulse Rise and Fall Time (10% to 90% V_{CC})	5ns	5ns
Input and Output Timing Reference Levels	0.90V	1.5V
Output Load	C_L = 100pF	C_L = 100pF

Figure 1. Output Load
** Including Probe and Jig Capacitance.



TRUTH TABLE						
Mode	Address	ROMCSB*	RAMCSB*	$\overline{WE}$	$\overline{OE}$	D0-D7
Standby	X	H	H	X	X	High-Z
Output Floating	A0-A17	L	H	X	H	High-Z
ROM Read	A0-A17	L	H	X	L	D_{OUT}
Output Floating	Only A0-A14 are Valid **	H	L	H	H	High-Z
RAM Read	Only A0-A14 are Valid **	H	L	H	L	D_{OUT}
RAM Write	Only A0-A14 are Valid **	H	L	L	X	D_{IN}

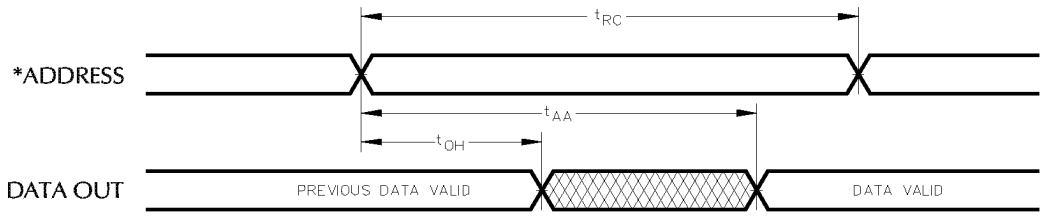
H = HIGH L = LOW X = Don't Care
* It is forbidden that ROMCSB pin and RAMCSB pin will be "0" at the same time.
** A15 - A17 must be fixed to "L" or "H".

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	V_{CC} = 1.8V		V_{CC} = 3.0±0.3V		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}	-500	+500	-500	+500	nA
I_{OUT}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	-500	+500	-500	+500	nA
I_{CC1}	ROM Operating Supply Current	$\overline{CS1}$ = V_{IL}, $\overline{CS2}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		0.350		4.0=1.1(f)	mA
I_{CC2}	RAM Operating Supply Current	$\overline{CS1}$ = V_{IH}, $\overline{CS2}$ = V_{IL}, $I_{I/O}$ = 0mA		0.275		2.5=1.0(f)	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V, V_{IN} ≤ 0.2V, V_{IN} ≥ V_{CC} -2.0V		0.90		10	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.0mA @ 3.3V		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.5mA @ 3.3V	0.8		2.2		V

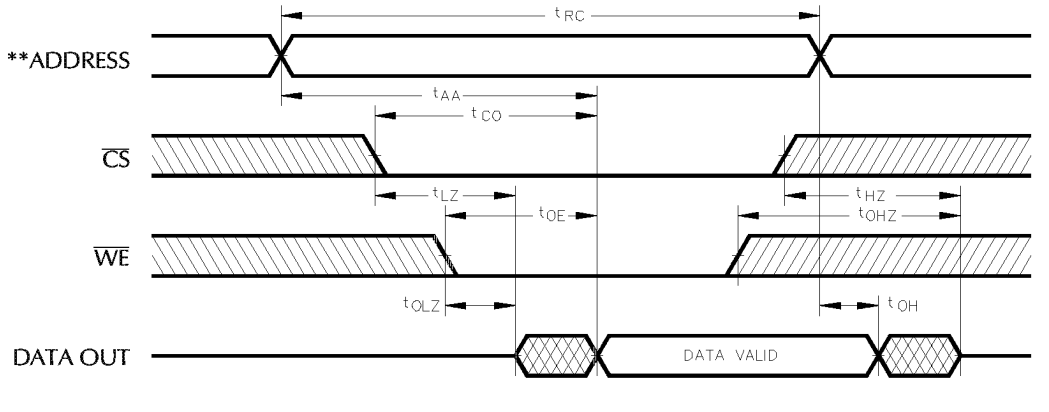
ROM OPERATION - READ CYCLE: $\overline{CS}2$ = RAMCSB = V_{IH}							
No.	Symbol	Parameter	V_{CC} = 1.8V Worse Case		V_{CC} = 3.0±0.3V Worse Case		Unit
			Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	500		300		ns
2	t_{AA}	Address Access Time		500		300	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		500		300	ns
4	t_{OE}	Output Enable to Output Valid		250		150	ns
5	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [5]	25		10		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z	25		10		ns
7	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]	0	30	0	20	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z * [4]	0	30	0	20	ns
9	t_{OH}	Output Hold from Address Change	8		7		ns

* Valid for both Read and Write Cycles.

ROM READ CYCLE 1: Address Controlled. $\overline{CS}2$/RAMSCB is High.



ROM READ CYCLE 2: $\overline{CS}$ & OE Controlled. $\overline{CS}2$/RAMSCB is High.

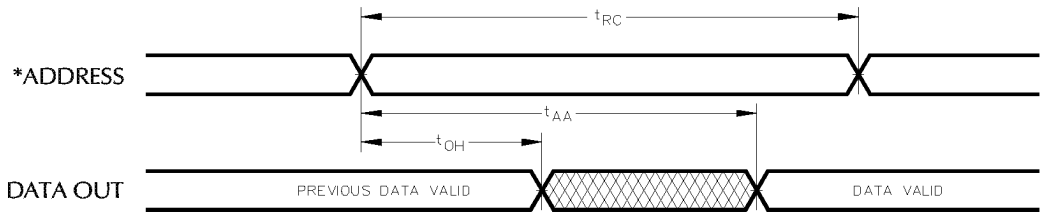


** Address valid prior to or coincident with $\overline{CS}1$ transition LOW.

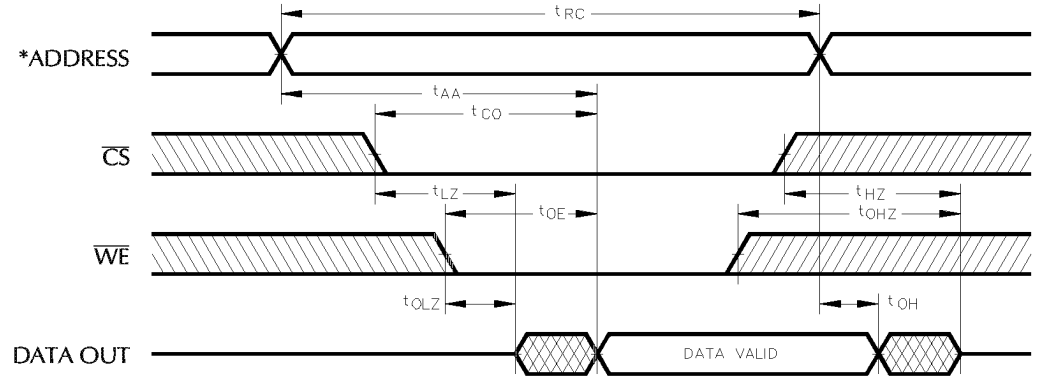
SRAM OPERATION - READ CYCLE: $\overline{CS}1$ = ROMCSB = V_{IH}							
No.	Symbol	Parameter	V_{CC} = 1.8V Worse Case		V_{CC} = 3.0±0.3V Worse Case		Unit
			Min.	Max.	Min.	Max.	
10	t_{RC}	Read Cycle Time	500		250		ns
11	t_{AA}	Address Access Time		500		250	ns
12	t_{CO}	$\overline{CE}$ to Output Valid		500		300	ns
13	t_{OE}	Output Enable to Output Valid		250		150	ns
14	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [5]	25		10		ns
15	t_{OLZ}	Output Enable to Output in LOW-Z	25		10		ns
16	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]	0	30	0	20	ns
17	t_{OHZ}	Output Enable to Output in HIGH-Z * [4]	0	30	0	20	ns
18	t_{OH}	Output Hold from Address Change	15		5		ns

* Valid for both Read and Write Cycles.

SRAM READ CYCLE 1: Address Controlled. $\overline{WE}$ is High.



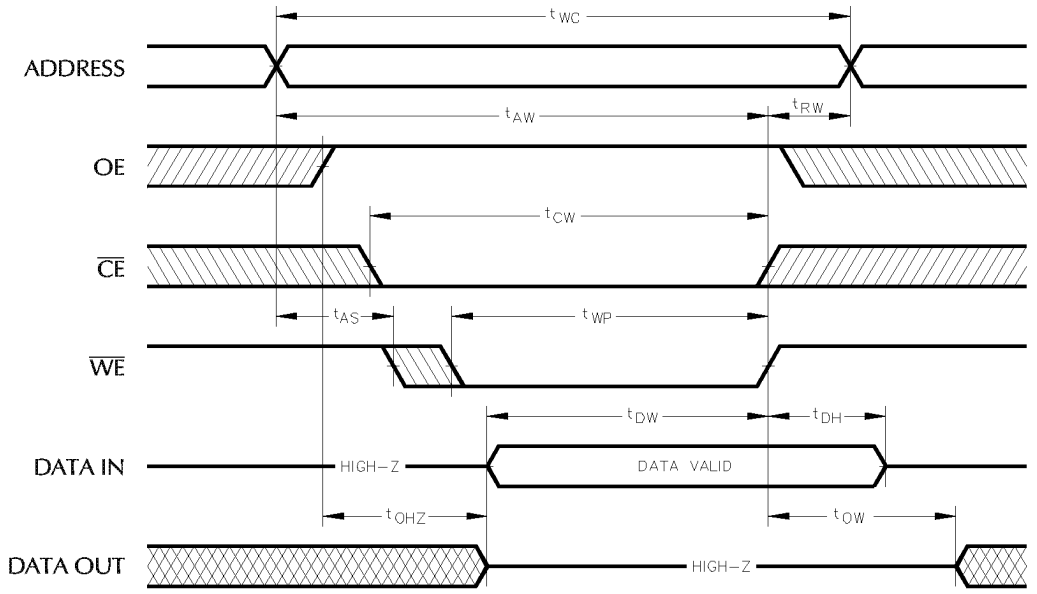
SRAM READ CYCLE 2: $\overline{WE}$ = V_{IH}.



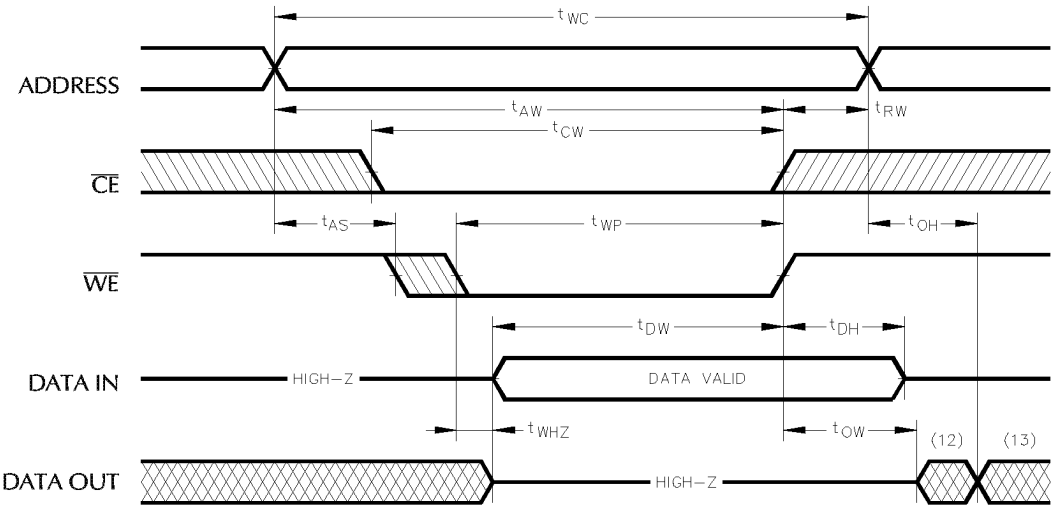
** Address valid prior to or coincident with $\overline{CS}2$ transition LOW.

OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE							
No.	Symbol	Parameter	V_{CC} = 1.8V		V_{CC} = 3.0±0.3V		Unit
			Min.	Max.	Min.	Max.	
19	t_{WC}	Write Cycle Time	500		250		ns
20	t_{AW}	Address Valid to End of Write	375		200		ns
21	t_{CW}	Chip Enable to End of Write	365		200		ns
22	t_{AS}	Address Set-Up Time	0		0		ns
23	t_{WP}	Write Pulse Width	375		200		ns
24	t_{WR}	Write Recovery Time	0		0		ns
25	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]	-	80	0	40	ns
26	t_{DW}	Data to Write Time Overlap	200		125		ns
27	t_{DH}	Data Hold from Write Time	0		0		ns
28	t_{OW}	Output Active from End of Write	15		5		ns

WRITE CYCLE: $\overline{OE}$ is Clock. $\overline{CS1}$ = ROMCSB = V_{IH}. [6, 11]



WRITE CYCLE 2: $\overline{OE}$ is fixed. $\overline{CS1}$ = ROMCSB = V_{IH}. [7, 11]

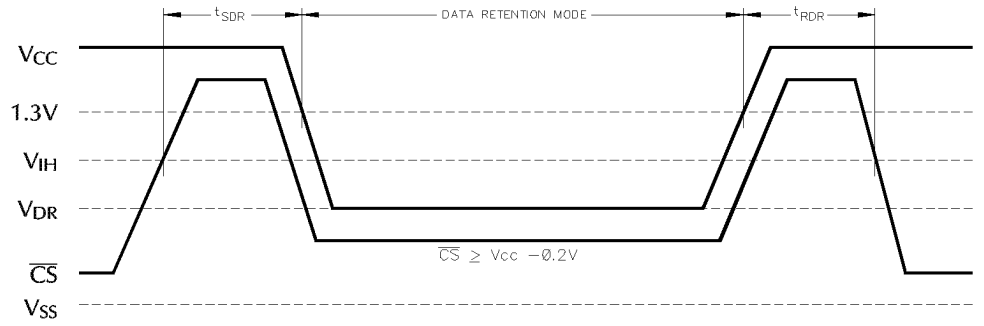


NOTES:

1. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
5. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
6. A write occurs during the overlap (t_{WP}) of a low $\overline{CS2}$ and low. A write begins at the latest transition among $\overline{CS2}$ going low and going low: A write end at the earliest transition among $\overline{CS2}$ going high and going high, t_{WP} is measured from the beginning of write to the end of write.
7. t_{CW} is measured from the later of $\overline{CS2}$ going low to end of write.
8. t_{AS} is measured from the address valid to the beginning of write.
9. t_{WR} is measured from the end of write to the address change.
10. If OE, WE are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
11. If 2 goes low simultaneously with going low or after going low, the outputs remain high impedance state.
12. D_{OUT} is the same phase of the latest written data in this write cycle.
13. D_{OUT} is the read data of new address

DATA RETENTION CHARACTERISTICS (T_A = -20 to +70°C)				
Symbol	Parameter	Min.	Max	Unit
V_{DR}	VCC for Data Retention	1.8	3.0	V
I_{DR}	Data Retention Current		3.0	µA
t_{SDR}	Data Retention Set-Up Time	0		ns
t_{RDR}	Recovery Time	5		ms

DATA RETENTION: $\overline{CS}$ Controlled.



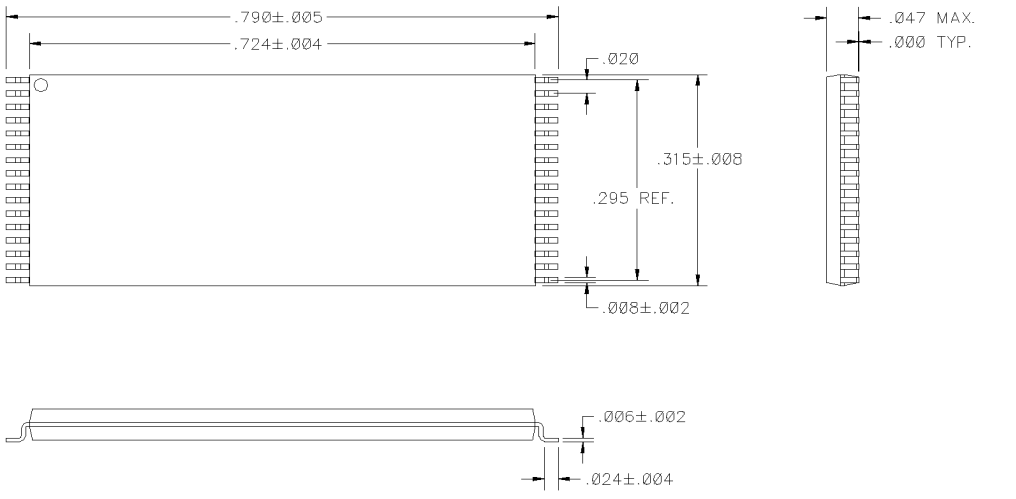
WAVEFORM KEY

ORDERING INFORMATION

DP (PREFIX) 50CM232 (PART TYPE)

- SRAM/ROM COMBO MEMORY
- DENSE-PAC

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove , California 92841-1431
(714) 898-0007 (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772 ◆ http://www.dense-pac.com