1 Megabyte Sync/Sync Burst, Small Outline DIMM

FEATURES

- 2x64kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Sequential Burst MODE
- Clock Controlled Registered Bank Enables (E1\, E2)
- Clock Controlled Byte Write Mode Enable (BWE\)
- Clock Controlled Byte Write Enables (BW1\ - BW8\)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW\)
- Aysnchronous Output Enable (G\)
- Internally self-timed Write
- Gold Lead Finish
- 3.3V ±10% Operation
- Access Speed(s): TKHQV=8.5, 9, 10, 12ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- *Multiple Vcc and Gnd*

The EDI2AG27265VxxD1 is a Synchronous/Synchronous Burst SRAM, 72 position 30 DIMM(144 contacts) Module, organized as 2x64Kx72. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS aysnchronous device architectures.

Synchronous Only operations are performed via strapping ADSC\ Low, and ADSP\ / ADV\ High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

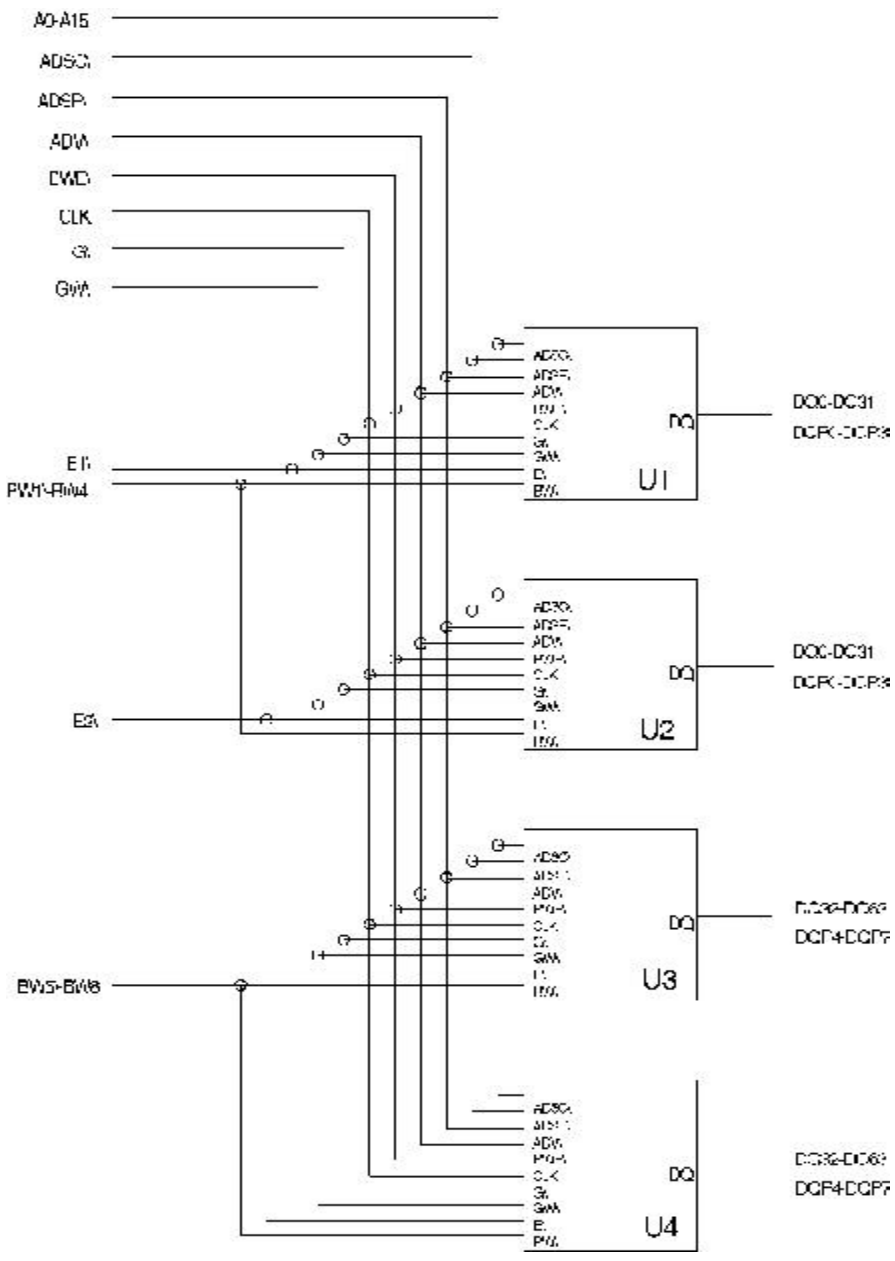
PIN NAMES

DQ0-DQ63	Input/Output Bus
DQP0-DQP7	Parity Bits
A0-A15	Address Bus
E1\, E2	Synchronous Bank Enables
BWE\	Byte Write Mode Enable
BW1\-BW8\	Byte Write Enables
Clk	Array Clock
GW\	Synchronous Global write Enable
G\	Asynchronous Output Enable
Vcc	3.3V Power Supply
Vss	Gnd

PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	VSS	37	DC0	73	VSS	109	DQ41
2	VSS	38	DC7	74	VSS	110	DQ40
3	A0	39	DC1	75	BW4	111	DQ42
4	PRU	40	DC9	76	DCP8	112	DQ45
5	PRU	41	DC2	77	VCC	113	DQ43
6	A1	42	DC3	78	VCC	114	DQ44
7	A2	43	DC3	79	DQ24	115	VSS
8	A15	44	DC4	80	DQ31	116	VSS
9	A14	45	VSS	81	DQ25	117	BW7
10	A3	46	VSS	82	DQ30	118	DCP9
11	A4	47	BW2	83	DQ28	119	VCC
12	A13	48	DCP1	84	DQ29	120	VCC
13	A12	49	VCC	85	DQ27	121	DC48
14	A5	50	VCC	86	DQ26	122	DQ55
15	A6	51	DC8	87	VSS	123	DQ49
16	A11	52	DC15	88	VSS	124	DQ54
17	A10	53	DC9	89	BW5	125	DQ50
18	A7	54	DC14	90	DQ14	126	DQ53
19	A8	55	DQ10	91	VCC	127	DQ51
20	A9	56	DQ13	92	VCC	128	DQ52
21	VCC	57	DC11	93	DQ22	129	VSS
22	VCC	58	DC12	94	DQ23	130	VSS
23	GW	59	VSS	95	DQ20	131	BW6
24	PRU	60	VSS	96	DQ21	132	DCP7
25	GW	61	BW3	97	DQ19	133	VCC
26	ADV	62	DCP2	98	DQ17	134	VCC
27	ADSP	63	VCC	99	DQ16	135	DQ35
28	ADSC	64	VCC	100	DQ18	136	DQ33
29	E1	65	DC16	101	VSS	137	DQ37
30	CLK	66	DQ39	102	VSS	138	DQ32
31	E2	67	DC17	103	BW8	139	DQ38
32	BW1	68	DQ32	104	DCP5	140	DQ31
33	BW0	69	DC18	105	VCC	141	DQ29
34	DCP0	70	DC21	106	VCC	142	DQ30
35	VCC	71	DC19	107	DQ40	143	VSS
36	VCC	72	DC20	108	DQ47	144	VSS

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
3, 6, 7, 10, 11 14, 15, 18, 19, 20 17, 16, 13, 12, 98	A0-A17	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.
33, 47, 61 75, 89, 103 117,13	BW1\, BW2\, BW3\, BW4\, BW5\, BW6\, BW7\, BW8\	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW0/ controls DQ0-7 and DQP0, BW1\ controls DQ8-15 and DQP1. BW2\ controls DQ16-23 and DQP2. BW3\ controls DQ24-31 and DQP3. BW4\ controls DQ32-39 and DQP4. BW5\ controls DQ40-47 and DQP5. BW6\ controls DQ48-55 and DQP6. BW7\ controls DQ56-64 and DQP7.
32	BWE\	Input Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
25	GW\	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE\ and BWx\ lines and must meet the setup and hold times around the rising edge of CLK.
30	CLK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
29, 31,	E1\, E2\ E3\, E4\	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP\.
23	G\	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
26	ADV\	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
27	ADSP\ Synchronous	Input	Address Status Processor: This active LOW input, along with EL\ and EH\ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
28	ADSC\ Synchronous	Input	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eight byte is DQ56-64.
38, 48, 62 76, 90, 104 118,132	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4\ is parity bit for DQ32-39. DQP5 is parity bit for DQ40-47. DQP6\ is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7.In order to use the device Configured as a128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor.
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground

SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1\	E2\	ADSP\	ADSC\	ADV\	GW\	G\	CLK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	X	H	H	L	X	L-H	D	Current

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1\	E2\	GW\	G\	ZZ	CLK	DQ
Synchronous Write-Bank 1	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	L	L	↑	

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
Vin	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.14	3.3	3.6	V
Supply Voltage	VSS	0.0	0.0	0.0	V
Input High	VIH	1.1	3.0	VCC+0.3	V
Input Low	VIL	-0.3	0.0	0.3	V
Input Leakage	ILi	-2	1	2	µA
Output Leakage	ILo	-2	1	2	µA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	SYM	Typ	8.5	5	10	Max 12	Units
Power Supply Current	Icc1	1.35	1.2	1.1	1.1	1.0	A
Power Supply Current Device Selected,No Operation	Icc	.700	.550	.800	.750	.700	A
CMOS Standby	Icc3	200	300	300	300	300	mA
Clock Running-Deselect	IccK	500	750	750	750	750	mA

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input and Output Timing Ref.	1.25V
Output Test equivalencies	

AC TEST LOAD

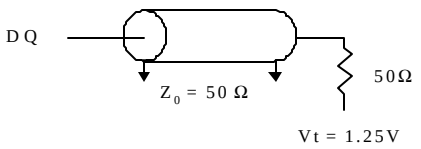


Fig. 1 Output Load Equivalent

BURST ADDRESS TABLE (MODE=NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A..A00	A..A01	A..A10	A..A11
A..A01	A..A00	A..A11	A..A10
A..A10	A..A11	A..A00	A..A01
A..A11	A..A10	A..A01	A..A00

BURST ADDRESS TABLE (MODE=GND)

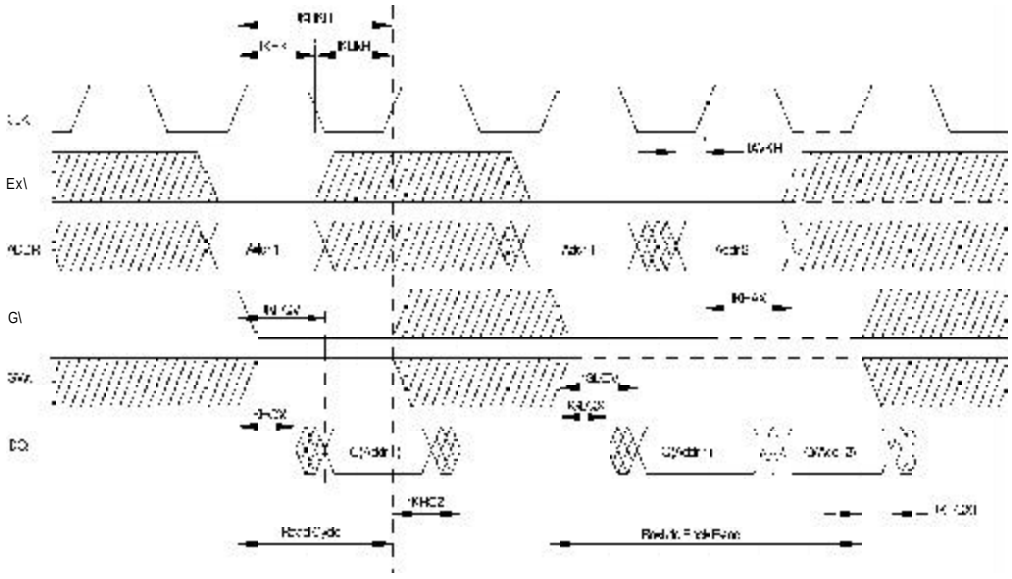
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A..A00	A..A01	A..A10	A..A11
A..A01	A..A10	A..A11	A..A00
A..A10	A..A11	A..A00	A..A01
A..A11	A..A00	A..A01	A..A10

READ CYCLE TIMING PARAMETERS

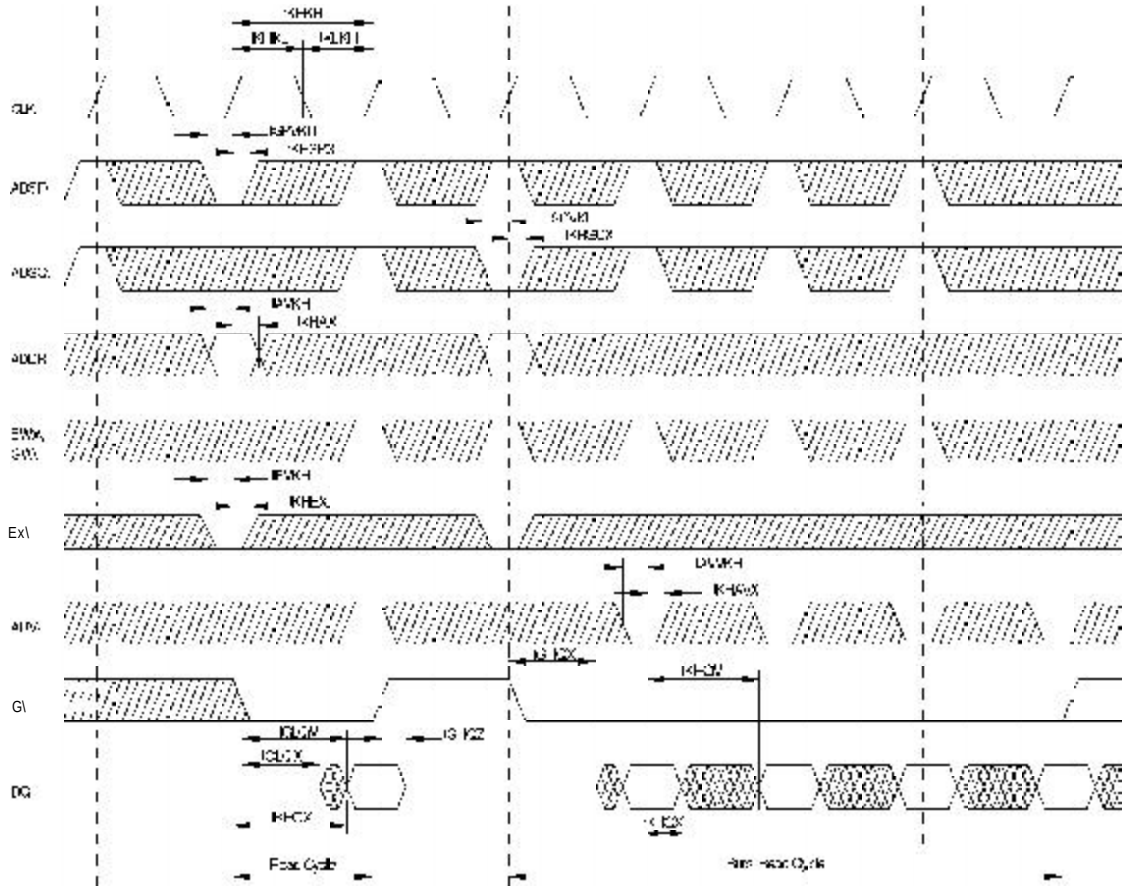
		8.5ns		9ns		10ns		12ns		
Description	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Cycle Time	tKhKh	*	*	10		10		15		ns
Clock High Time	tKHKL	*	*	4		5		5		ns
Clock Low Time	tKLKH	*	*	9		5		5		ns
Clock to Output Valid	tKHQV	*	*		9		10		12	ns
Clock to Output Invalid	tKHQX1	*	*	3		3		3		ns
Clock to Output Low-Z	tKHQX	*	*	2		2		2		ns
Output Enable to Output Valid	tGLQV	*	*		4		4		5	ns
Output Enable to Output Low-Z	tGLQX	*	*	0		0		0		ns
Output Enable to Output High-Z	tGHQZ	*	*		9		9		5	ns
Address Setup	tAVKH	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	tEVKH	*	*	2.5		2.5		2.5		ns
Address Hold	tKHAX	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	tKHEX	*	*	1.0		1.0		1.0		ns

*TBD

SYNCHRONOUS ONLY READ CYCLE



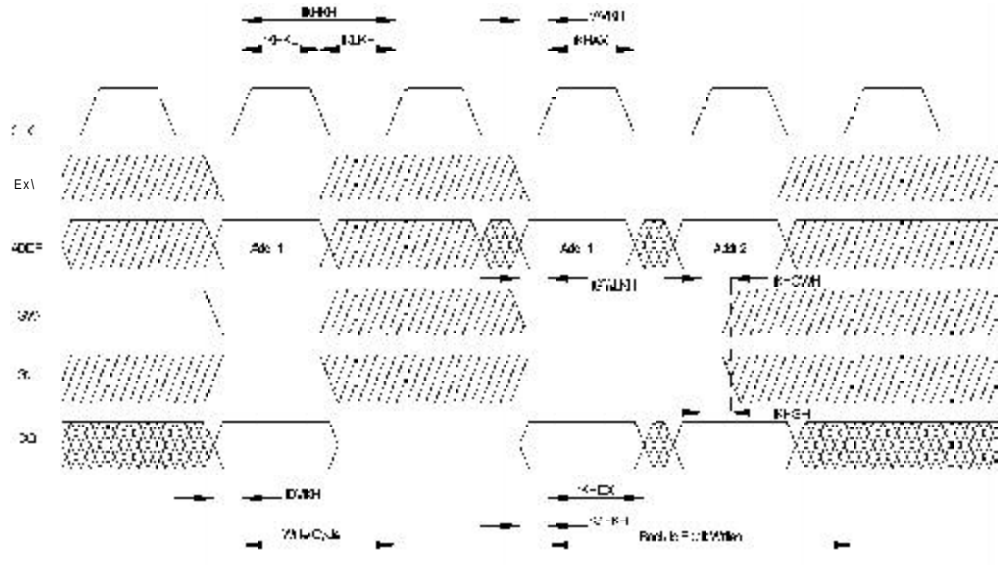
SYNC-BURST READ CYCLE



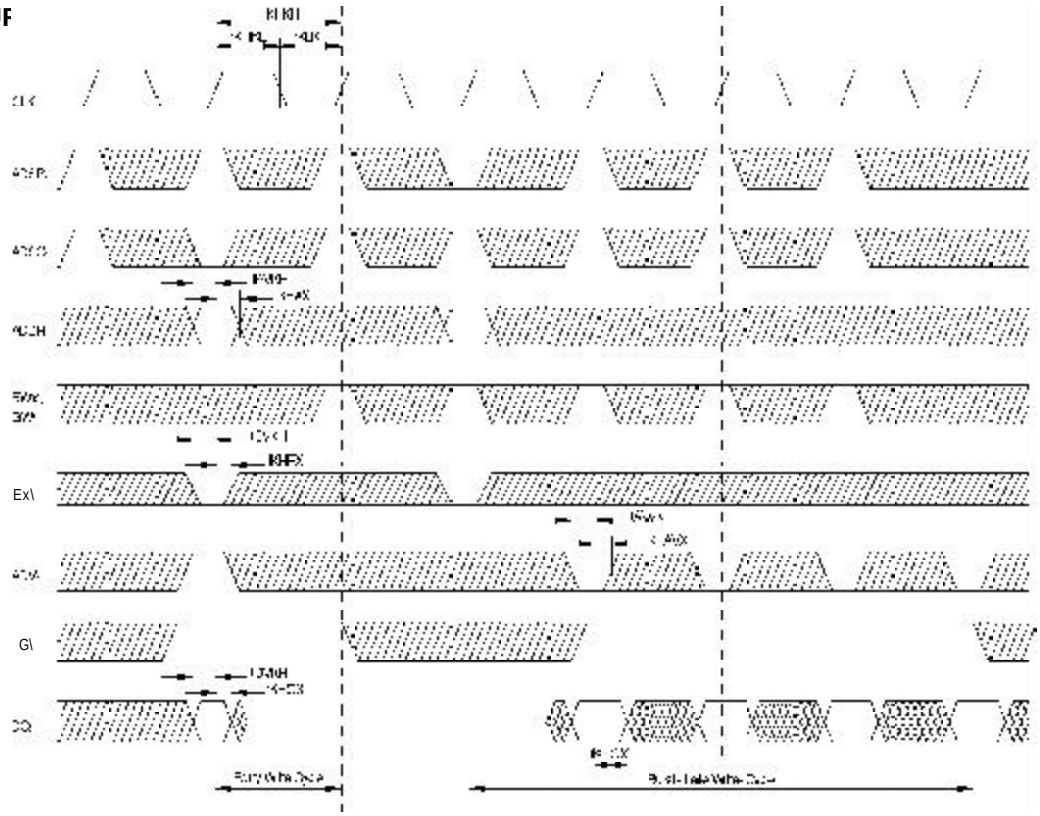
WRITE CYCLE TIMING PARAMETERS

		8.5ns		9ns		10ns		12ns		
Description	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Cycle Time	tKHKH			10		12		15		ns
Clock High Time	tKHKL			4		5		5		ns
Clock Low Time	tKLKH			4		5		5		ns
Address Setup	tAVKH			2.5		2.5		2.5		ns
Address Hold	tKHAX			1.0		1.0		1.0		ns
Bank Enable Setup	tEVKH			2.5		2.5		2.5		ns
Bank Enable Hold	tKHEX			1.0		1.0		1.0		ns
Global Write Enable Setup	tWVKH			2.5		2.5		2.5		ns
Global Write Enable Hold	tKHWX			1.0		1.0		1.0		ns
Data Setup	tDVKH			2.5		2.5		2.5		ns
Data Hold	tKHDX			1.0		1.0		1.0		ns

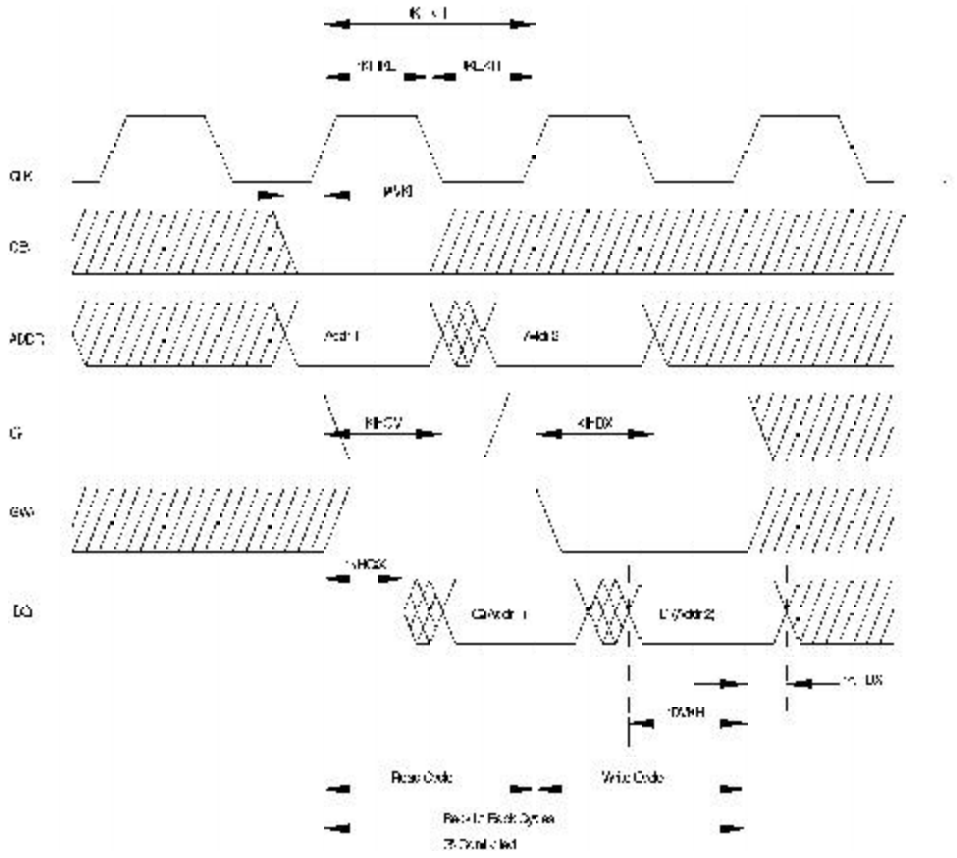
SYNC (NON-BURST) WRITE CYCLE



SYNCBUF



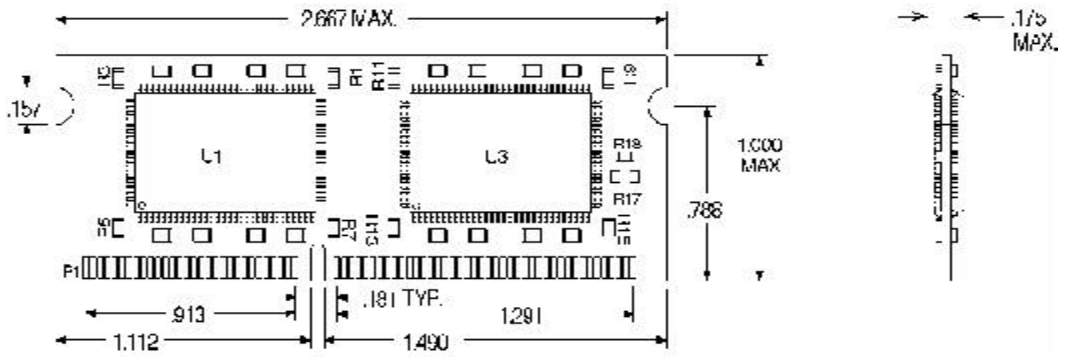
SYNC (NON-BURST) READ/WRITE CYCLE



PACKAGE DESCRIPTION

Package No. 409

144 Lead
SO-DIMM



Ordering Information

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2AG27265V85D1*	2x64Kx72	3.3	8.5	144 SO-DIMM
EDI2AG27265V9D1*	2x64Kx72	3.3	9	144 SO-DIMM
EDI2AG27265V10D1	2x64Kx72	3.3	10	144 SO-DIMM
EDI2AG27265V12D1	2x64Kx72	3.3	12	144 SO-DIMM

**Consult Factory for Availability*