Ordering number : ENN8013

SANYO Semiconductors

DATA SHEET

CMOS IC

LC723341E — ETR Controller

Overview

The LC723341E is a single-chip microcontroller/electronic tuner that also integrates a 250 MHz PLL circuit and a 1/4-duty 1/2-bias LCD driver on the same chip.

Functions

- Program memory (ROM): 4096 × 16 bits (8 KB)
- Data memory (RAM): 256 × 4 bits
- Cycle time: 1.33 µs (all one-word instructions) at 4.5 MHz
- Stack: 8 levels
- LCD driver: 48 to 80 segments (1/4-duty 1/2-bias drive)
- Interrupts: External interrupts: 2 systems
  Timer interrupts: 2 systems (1, 5, 10 or 50 ms)
- A/D converter: Four input channels (6-bit successive approximation conversion)
- Dedicated input ports: 8 ports (of which 4 can be switched for use as A/D converter inputs)
- Dedicated output ports: 10 ports (of which 6 are open-drain ports and 4 can be switched between CMOS and open-drain specifications)
- I/O ports: 19 ports (of which 8 can be switched for use as segment ports)
- PLL: Reference frequencies: 3, 3.125, 5, 6.25, 12.5 and 25 kHz
  Supports dead zone control (4 types) and features a built-in unlock detection circuit.
- Input frequency (input sensitivity): FM band - 10 to 250 MHz
  AM band- 0.5 to 40 MHz
- Input sensitivity: FM band - 35 mV rms (Above 130 MHz: 50 mV rms)
  AM band - 35 mV rms
- IF counting: HCTR input - 0.4 to 12 MHz (35 mV rms)
- External reset input: The program counter starts from location 0 during CPU and PLL operation
- Reset: Built-in voltage detection reset circuit
- Halt mode: The controller's operating clock is temporarily slowed to reduce current drain.
- Backup mode: The crystal oscillator is stopped.
- Static power on function: Backup mode is cleared using the PF port.
- Beep tone: Frequencies of 0.75, 1.25, 1.5, 2.08. 2.5, 3.125, and 6.25 kHz
- Memory retention voltage: 0.9 V or higher
- VDD: PLL 4.5 to 5.5 V
  CPU 3.5 to 5.5 V
- Package: QIP64E (0.8 mm pitch)

SANYO Electric Co., Ltd. Semiconductor Company
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Specifications

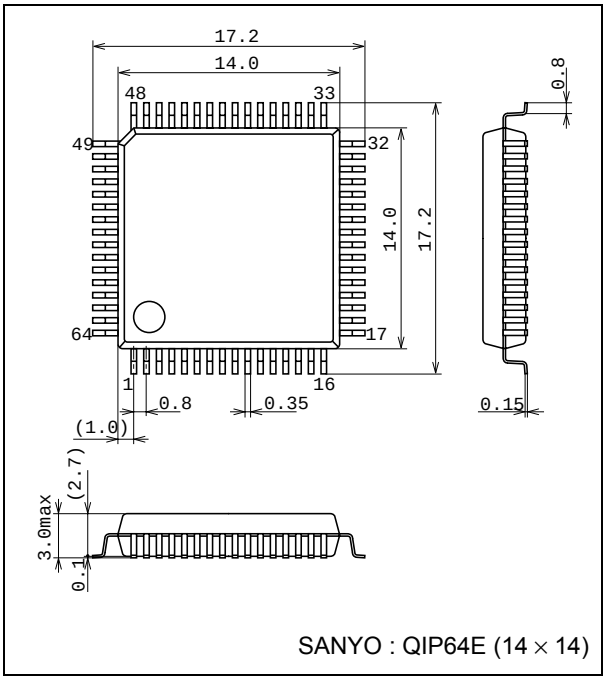
Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	V_{IN}	All input pins	–0.3 to VDD to +0.3	V
Output voltage	$V_{OUT}1$	PE2, PL0 to PL3	–0.3 to +15	V
	$V_{OUT}2$	All output pins except $V_{OUT}1$	–0.3 to VDD + 0.3	V
Output current	$I_{OUT}1$	PC, PD, PE3, PG, PH, PK, EO	0 to 3	mA
	$I_{OUT}2$	PB	0 to 1	mA
	$I_{OUT}3$	PE2, PL0 to PL3	0 to 2	mA
	$I_{OUT}4$	S1 to S20	0 to 1	μA
	$I_{OUT}5$	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –20 to +70°C	300	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–45 to +125	°C

Package Dimensions

unit: mm

3159A



SANYO : QIP64E (14 × 14)

Allowable Operating Ranges at Ta = -20 to +70°C, V_{DD} = 2.6 to 5.5V

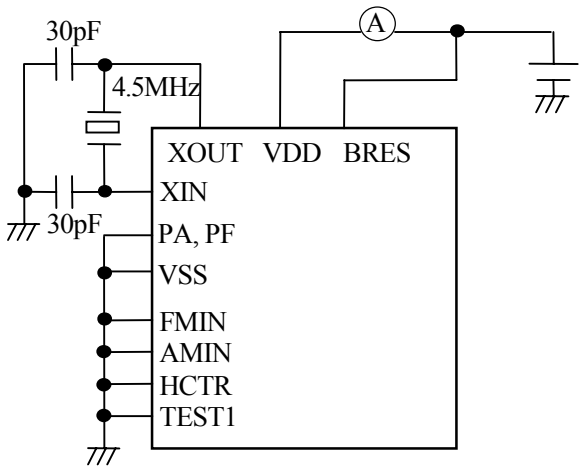
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	PLL operating voltage	4.5		5.5	V
	$V_{DD}2$	Memory retention voltage	0.9		5.5	
	$V_{DD}3$	CPU operating voltage	2.6		5.5	
High-level input voltage	$V_{IH}1$	Input ports other than $V_{IH}2$, $V_{IH}3$, AMIN, FMIN, HCTR, and XIN	$0.7V_{DD}$		V_{DD}	V
	$V_{IH}2$	BRES	$0.8V_{DD}$		V_{DD}	V
	$V_{IH}3$	The PF port	$0.6V_{DD}$		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Input ports other than $V_{IL}2$, $V_{IL}3$, AMIN, FMIN, HCTR, and XIN	0		$0.3V_{DD}$	V
	$V_{IL}2$	BRES	0		$0.2V_{DD}$	V
	$V_{IL}3$	The PF port	0		$0.2V_{DD}$	V
Input amplitude	$V_{IN}1$	XIN	0.5		1.5	Vrms
	$V_{IN}2$	FMIN: $F_{IN}2$, AMIN	0.035		0.35	Vrms
	$V_{IN}3$	FMIN: $F_{IN}3$	0.05		0.35	Vrms
	$V_{IN}4$	HCTR	0.035		0.35	Vrms
Input voltage range	$V_{IN}5$	ADI0, ADI1, ADI2, ADI3	0		V_{DD}	V
Input frequency	$F_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$F_{IN}2$	FMIN: $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$F_{IN}3$	FMIN: $V_{IN}3$, $V_{DD}1$	130		250	MHz
	$F_{IN}4$	AMIN(H): $V_{IN}2$, $V_{DD}1$	2		40	MHz
	$F_{IN}5$	AMIN(L): $V_{IN}2$, $V_{DD}1$	0.5		10	MHz
	$F_{IN}6$	HCTR: $V_{IN}4$, $V_{DD}1$	0.4		15	MHz

Electrical Characteristics under the Allowable Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	$I_{IH}1$	XIN: $V_I = V_{DD} = 5.0V$	2.0	5.0	15	µA
	$I_{IH}2$	FMIN, AMIN, HCTR: $V_I = V_{DD} = 5.0V$	4.0	10	30	µA
	$I_{IH}3$	Ports PA (pull-down resistors disabled), PC, PD, PF, PG, PH, and PK. BRES: $V_I = V_{DD} = 5.0$ V.			3	µA
Low-level input current	$I_{IL}1$	XIN: $V_I = V_{DD} = V_{SS}$	–2.0	–5.0	–15	µA
	$I_{IL}2$	FMIN, AMIN, HCTR: $V_I = V_{DD} = V_{SS}$	–4.0	–10	–30	µA
	$I_{IL}3$	Ports PA (pull-down resistors disabled), PC, PD, PF, PG, PH, and PK. BRES: $V_I = V_{DD} = V_{SS}$.			–3	µA
Input floating voltage	V_{IF}	PA. Pull-down resistors enabled			$0.05V_{DD}$	V
Pull-down resistance	$R_{PD}1$	PA pull-down resistors. $V_{DD} = 5.0$ V	75	100	200	kΩ
	$R_{PD}2$	TEST1 resistance		10		kΩ
Hysteresis	V_H	BRES	$0.1V_{DD}$			V
High-level output voltage	$V_{OH}1$	PB: IO = 1mA	V_{DD}–2.0	V_{DD}–1.0		V
	$V_{OH}2$	PC, PD, PE3, PG, PH, PK: I_O = 1mA	V_{DD}–1.0			V
	$V_{OH}3$	EO: I_O = 500µA	V_{DD}–1.0			V
	$V_{OH}4$	XOUT: I_O = 200µA	V_{DD}–1.0			V
	$V_{OH}5$	S1 to S20: I_O = 100µA	V_{DD}–1.0			V
	$V_{OH}6$	COM1, COM2, COM3, COM4: I_O = 5µA	V_{DD}–0.75	V_{DD}–0.5		V
Low-level output voltage	$V_{OL}1$	PB: I_O = –50µA		1.0	2.0	V
	$V_{OL}2$	PC, PD, PE3, PG, PH, PK: I_O = –1mA			1.0	V
	$V_{OL}3$	EO: I_O = –500µA			1.0	V
	$V_{OL}4$	XOUT: I_O = –200µA			1.0	V
	$V_{OL}5$	S1 to S20: I_O = –100µA			1.0	V
	$V_{OL}6$	COM1, COM2, COM3, COM4: I_O = –5µA		0.5	0.75	V
	$V_{OL}7$	PE2, PL0 to PL3: IO = 5mA			2.0	V
Output off leakage current	$I_{OFF}1$	The PB, PC, PD, PE3, PG, PH, PK, and EO ports	–3		+3	µA
	$I_{OFF}2$	PE2, PL0 to PL3	–100		+100	nA
Output mid-level voltage	V_M	COM1, COM2, COM3, COM4: $V_{DD} = 5.0V$	2.0	2.5	3.0	V
A/D conversion error		ADI0, ADI1, ADI2, ADI3	–1/2		+1/2	LSB
Power down detection voltage	V_{DET}		2.7	3.0	3.3	V
Current drain	$I_{DD}1$	$V_{DD}1$: $F_{IN}2$ 130MHz Ta = 25°C		15	20	mA
	$I_{DD}2$	$V_{DD}3$: Halt mode, Ta = 25°C *1		0.6		mA
	$I_{DD}3$	V_{DD} = 5.5 V, oscillator stopped, Ta = 25°C *2			5	µA
	$I_{DD}4$	V_{DD} = 2.5 V, oscillator stopped, Ta = 25°C *2			1	µA

Note: The halt mode current is used to execute 20 instruction steps every 125 ms.

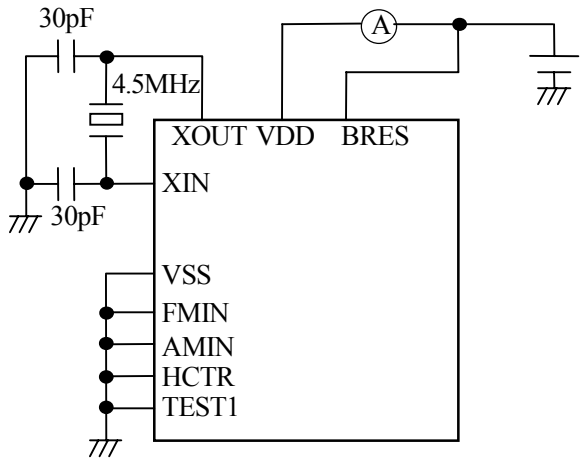
*1 Halt and PLL stop mode current measurement conditions



With all ports other than those mentioned above left open.
With output mode selected for PC and PD.
With segment mode selected for S13 to S20.

Set up halt mode with a software instruction.
The state where CPU operation is stopped without stopping the crystal oscillator.

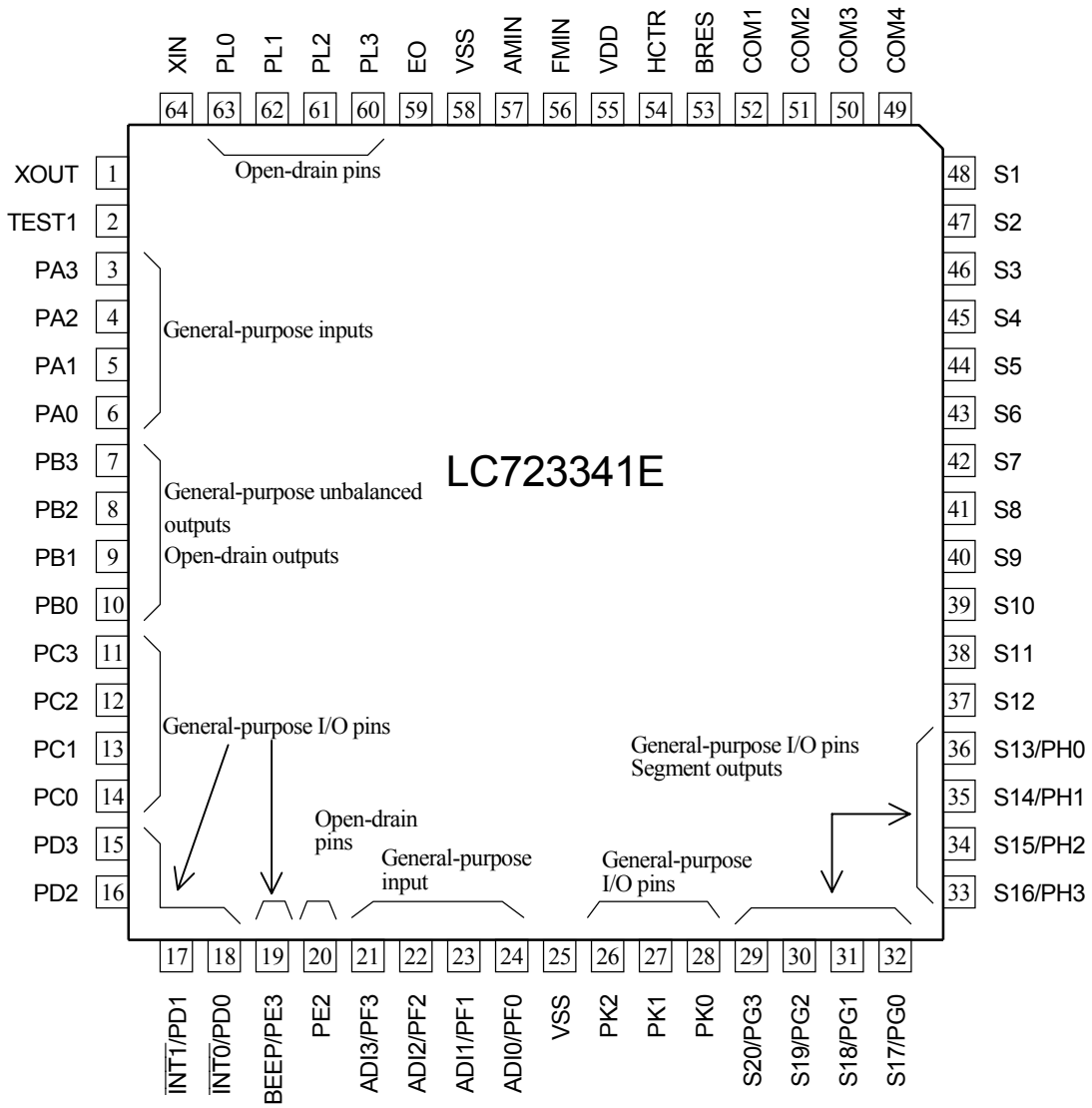
*2 Backup mode current measurement conditions



With all ports other than those mentioned above left open.
With output mode selected for PC and PD.
With segment mode selected for S13 to S20.

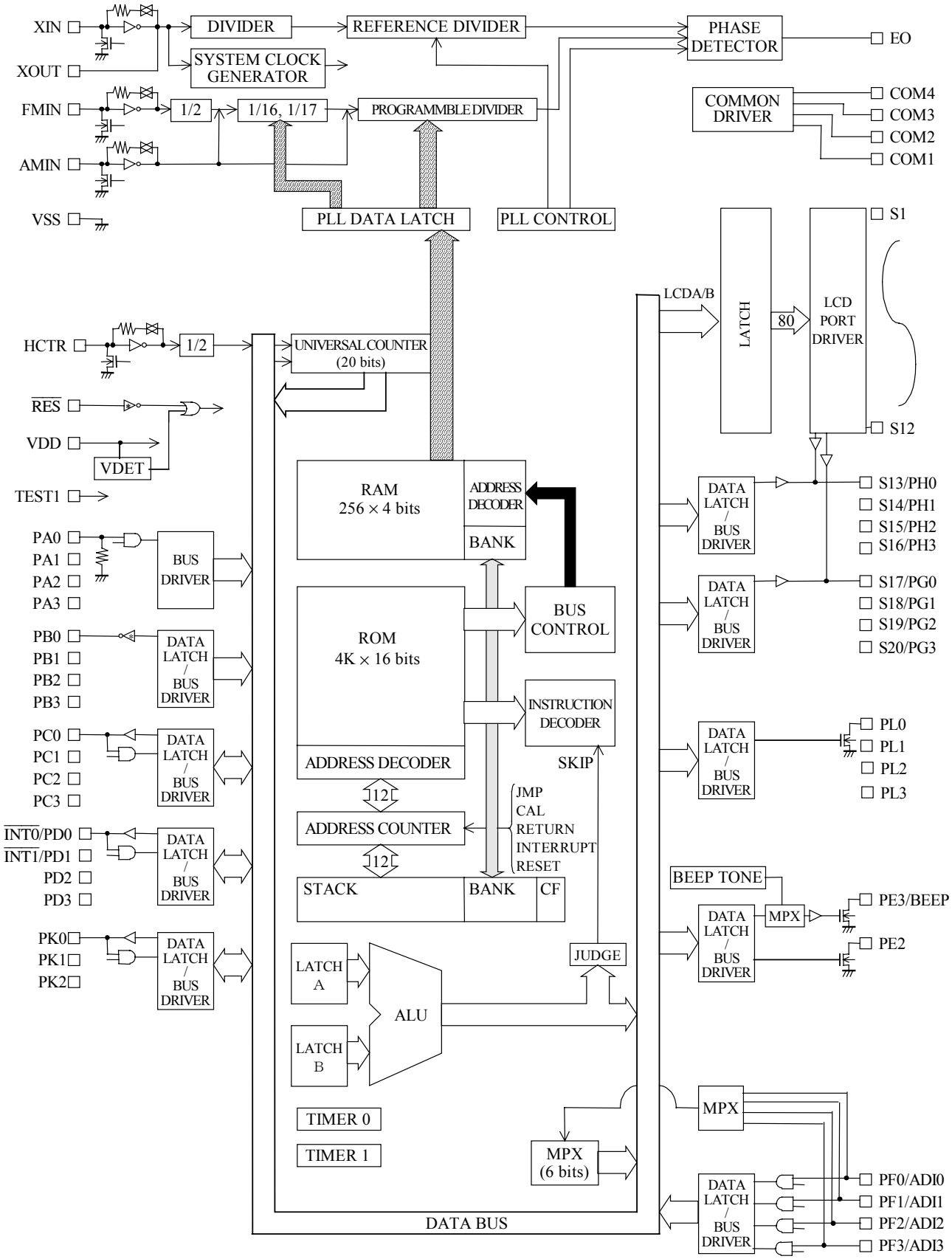
Set up backup mode with a software instruction.
The state where the crystal oscillator is stopped.

Pin Assignment

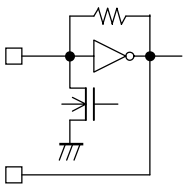
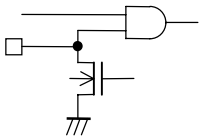
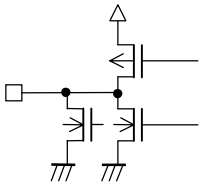
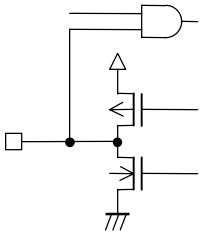
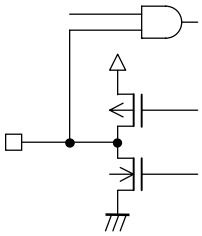


Top view

Block Diagram



Pin Functions

Pin No.	Symbol	I/O	Description	Equivalent circuit
64 1	XIN XOUT	I O	4.5 MHz crystal oscillator circuit connections	
2	TEST1	I	IC test pin This pin must be connected to ground during normal operation.	—
6 5 4 3	PA0 PA1 PA2 PA3	I	These input ports are used as the key return ports and are designed with a low threshold voltage. When a key matrix is formed with the PB port, multiple key presses with up to 3 keys can be detected. The four pull-down resistors are enabled/disabled together with an IOS instruction (PWn = 2, b1). The pull-down resistors cannot be controlled individually. In backup mode, this port goes to the input disabled state, and the pull-down resistors will be in the disabled state after a reset.	Input with built-in pull-down resistor 
10 9 8 7	PB0 PB1 PB2 PB3	O	These output ports are used as the key source ports and can be set up to be either unbalanced outputs or open-drain outputs. The output type is set with an IOS instruction (PWn = 2, b0, b2, b3). When used set to the unbalanced output circuit type, diodes to prevent short circuits due to multiple key presses are not required. If used set to the open-drain output circuit type, pull-up resistors between VDD and the port pins are required. In backup mode, this port goes to the output high-impedance state. After a reset, this port will be in the output high-impedance state, and will remain in that state until an output instruction (an OUT, SPB, or RPB instruction) is executed. *: Note that the output impedance requires care if these pins are used for any purpose other than as key source outputs.	Unbalanced CMOS push-pull or n-channel open-drain output 
15 14 13 12	PC0 PC1 PC2 PC3	I/O	General-purpose I/O ports. *1 The IOS instruction (PWN = 4) is used to switch between the general-purpose input and output port functions. The I/O direction can be set in 1-bit units. (0: input, 1: output) In backup mode, this port goes to the input disabled high-impedance state. After a reset, the general-purpose input port function will be selected.	CMOS push-pull circuit 
18 17 16 15	PD0/$\overline{\text{INT0}}$ PD1/$\overline{\text{INT1}}$ PD2 PD3	I/O	General-purpose I/O ports. *1 The IOS instruction (PWN = 5, b0, b1) is used to switch between the general-purpose input and output port functions. The I/O direction can be set in 1-bit units. (0: input, 1: output) Two of these port pins can be used as external interrupt inputs. In that case, the I/O direction must be set to input, and rising or falling edge detection must be selected with an IOS instruction (PWN = 3, b0, b1). In backup mode, this port goes to the input disabled high-impedance state. After a reset, the general-purpose input port function will be selected.	CMOS push-pull circuit 

Note: ∗1 When ports that can be switched between input and output are used as output ports, the output data must be established in advance with an OUT, SPB, or RPB instruction before the port is set to output mode with an IOS instruction.

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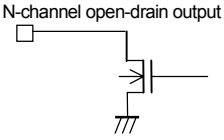
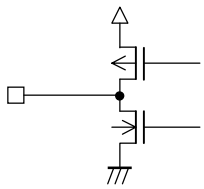
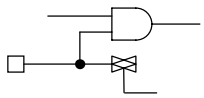
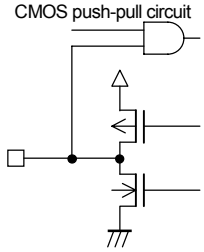
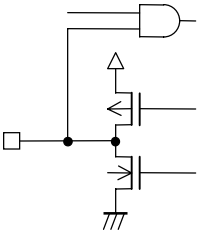
Pin No.	Symbol	I/O	Description	Equivalent circuit
20	PE2	O	PE2 is an open-drain output port. A pull-up resistor between this port and VDD is required. In backup mode, PE2 goes to the high-impedance state. After a reset, it remains at the low level until an output instruction is executed.	N-channel open-drain output 
18	PE3/BEEP	O	General-purpose output or beep tone output shared-function port. The BEEP instruction is used to switch between the general-purpose output and beep tone output functions. To use this port as a general-purpose output port, execute a BEEP instruction with b3 = 0 to set up the general-purpose output function. If b3 = 1, the beep tone output function will be selected. Bits b0, b1, and b2 select the beep tone frequency. The LC723341E provides seven beep tone frequencies. *: When the PE3 port is set to the beep tone function, executing an output instruction only switches the state of the internal output latch and has no effect on the beep tone output. In backup mode, this port goes to the high-impedance state. This state is maintained until either an output instruction or a BEEP instruction is executed. After a reset, the general-purpose output port function will be selected.	CMOS push-pull output 
24 23 22 21	PF0/ADI0 PF1/ADI1 PF2/ADI2 PF3/ADI3	I	General-purpose input or A/D converter input shared-function ports. The IOS instruction (PWn = FH, b0 to b3) is used to switch between the general-purpose input and A/D converter input functions. The function can be switched in 1-bit units. (0: general-purpose input, 1: A/D converter input) When the A/D converter input function is selected, the pin to be A/D converted is selected with the IOS instruction (PWn = 1). The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read out the data. *: Since CMOS input is disabled, the data read out will always be zero if an input instruction is executed for a port pin set to analog input mode. Execute an IOS instruction (PWn = 0, b0 to b3) to set the port that clears backup mode. In backup mode, this port goes to input disabled high-impedance state. After a reset, the general-purpose input port function will be selected. The conversion time for the 6-bit successive approximation A/D converter is 0.64 ms. The A/D converter full-scale voltage is 63/96 of VDD.	CMOS input or analog input 
28 27 26	PK0 PK1 PK2	I/O	These are general-purpose I/O ports. *1 The IOS instruction (PWN = A) is used to switch between the general-purpose input and output port functions. The I/O direction can be set in 1-bit units. (0: input, 1: output) In backup mode, this port goes to the input disabled high-impedance state. After a reset, the general-purpose input port function will be selected.	CMOS push-pull circuit 
32 31 30 29 36 35 34 33	S17/PG0 S18/PG1 S19/PG2 S20/PG3 S13/PH0 S14/PH1 S15/PH2 S16/PH3	I/O	LCD driver segment output or general-purpose I/O shared-function ports. *1 The IOS instruction is used to switch between the segment output and general-purpose I/O functions and for I/O direction switching for the general-purpose port function. • When used as segment output ports PG port ... IOS instruction (PWn = B, b0 to b3) 0: Segment output PH port ... IOS instruction (PWn = C, b0 to b3) 0: General-purpose I/O These pins can be switched in 1-bit units. • When used as general-purpose I/O ports PG port ... IOS instruction (PWn = 6, b0 to b3) 0: Input PH port ... IOS instruction (PWn = 7, b0 to b3) 1: Output The I/O directions of these pins can be set in 1-bit units. In backup mode, when used as general-purpose output ports, the pins go to the input disabled high-impedance state. When used as segment outputs, these pins will be held fixed at the low level. After a reset, the segment output function will be selected.	CMOS push-pull circuit 

Note: *1 When ports that can be switched between input and output are used as output ports, the output data must be established in advance with an OUT, SPB, or RPB instruction before the port is set to output mode with an IOS instruction.

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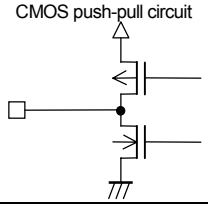
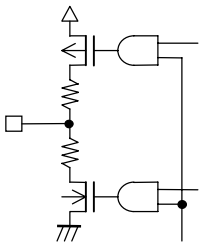
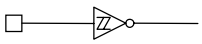
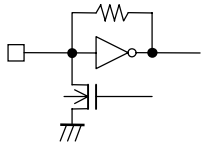
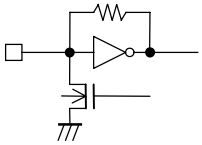
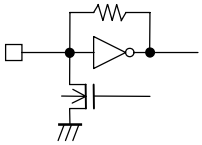
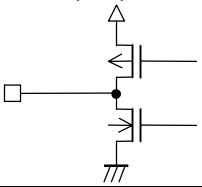
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Equivalent circuit</th></tr>
<tr><td>48-37</td><td>S1-S12</td><td>O</td><td>LCD driver segment output pins.
This driver implements 1/4-duty 1/2-bias drive.
The frame frequency is 75 Hz.
In backup mode, after a reset, and after an LCD off instruction has been executed, these pins will be held fixed at the low level.</td><td>CMOS push-pull circuit
  </td></tr>
<tr><td>62
61
60
59</td><td>COM1
COM2
COM3
COM4</td><td>O</td><td>LCD driver common output pins.
This driver implements 1/4-duty 1/2-bias drive.
The frame frequency is 75 Hz.
In backup mode, after a reset, and after an LCD off instruction has been executed, these pins will be held fixed at the low level.</td><td>  </td></tr>
<tr><td>69</td><td>BRES</td><td></td><td>System reset pin.
If this pin is held low for at least one machine cycle during CPU operation or in halt mode, the system will be reset and execution will continue with the program counter set to location 0.</td><td>  </td></tr>
<tr><td>54</td><td>HCTR</td><td>I</td><td>Dedicated universal counter input port.
• For frequency measurement, select frequency measurement mode with the UCD instruction (b3 = 0, b2 = 0) and start the counter with the UCC instruction.
<table>
<tr><th>UCS b3, b2</th><th>Measurement time</th><th>Measurement mode</th></tr>
<tr><td>0 0</td><td>HCTR</td><td>Frequency</td></tr>
<tr><td>0 1</td><td>—</td><td>—</td></tr>
<tr><td>1 0</td><td>—</td><td>—</td></tr>
</table>
<table>
<tr><th>UCS b1, b0</th><th>Measurement time</th></tr>
<tr><td>0 0</td><td>1 ms</td></tr>
<tr><td>0 1</td><td>4 ms</td></tr>
<tr><td>1 0</td><td>8 ms</td></tr>
<tr><td>1 1</td><td>32 ms</td></tr>
</table>
The CNTEND flag will be set when the count completes. In this mode, the input operates as an AC amplifier. Thus the input must be capacitance coupled. Input is disabled in backup mode, in halt mode, during a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>56</td><td>FMIN</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected using the PLL instruction CW1 field.
<table>
<tr><th>CW1 b1, b0</th><th>Band</th></tr>
<tr><td>0 0</td><td>10 to 250 MHz</td></tr>
</table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, during a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>57</td><td>AMIN</td><td>I</td><td>AM VCO (local oscillator) input.
This pin is selected and the bandwidth set using the PLL instruction CW1 field.
<table>
<tr><th>CW1 b1, b0</th><th>Band</th></tr>
<tr><td>1 0</td><td>2 to 40 MHz (SW)</td></tr>
<tr><td>1 1</td><td>0.5 to 10 MHz (MW,LW)</td></tr>
</table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, during a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>59</td><td>EO</td><td>O</td><td>This is the main charge pump output. When the frequency of the local oscillator divided by N is higher than the reference frequency, a high level is output, and when it is lower, a low level is output. This pin goes to the high-impedance state when the frequencies match.
This pin goes to the output high-impedance state in backup mode, in halt mode, during a reset, and in PLL stop mode.</td><td>CMOS push-pull circuit
  </td></tr>
</table>

Continued on next page.

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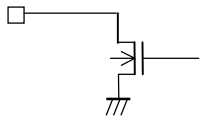
Pin No.	Symbol	I/O	Description	Equivalent circuit
63 62 61 60	PL0 PL1 PL2 PL3	O	Open-drain output port. Pull-up resistors must be inserted between these port pins and VDD. These pins go to the high-impedance state in backup mode. After a reset, the output remains at the low level until an output instruction is executed.	N-channel open-drain output 
25 58 55	VSS VSS VDD	—	Power supply connections. Connect the VSS pins to the minus side (ground) of the power supply. Connect the VDD pin to the plus side.	—