NEC Electronics Inc.

NEC

ADVANCED PRODUCT INFORMATION USER'S MANUAL

June 1985

μPD7761/62, MC4760

Speech Recognition LSI Set

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CHAPTER 1 SPEECH RECOGNITION SYSTEM

The MC-4760, uPD7761, and uPD7762 are a three-chip set that offers all the necessary functions for performing speech recognition. You can implement a speech recognition system with a minimum amount of hardware using this set of devices. The analog interface (MC-4760), analysis and matching processor (uPD7761), and system control processor (uPD7762), provide the basis for a variety of speech recognition applications. You can interface the LSI set with a pattern registration memory and a host system to create a high-performance speech recognition system. No other interface is required if you use the special serial interface. You control the functions of the LSI set with simple commands issued from the host computer.

You can classify speech recognition according to speaker dependence or independence, and the continuity of speech recognized. Speaker-dependent recognition requires training the system to recognize speech patterns for specific speakers. Recognition then consists of pattern-matching to a previously established vocabulary unique to the individual speaker. Speaker-independent recognition uses composite patterns that represent many different speakers.

The continuity of the speech can be classified as isolated-word or connected-word speech. Isolated-word recognition requires that a spoken utterance have a finite time duration. Speech is recognized as an entity at the end of the input and before the next input to the system. Connected-word speech recognition, in NEC's definition, supports speech entered without pauses between words.

The three-chip system described in this manual functions as an isolated-word speaker-dependent speech recognition system.

1.1 Features

- Isolated word speech recognition by the time-compressed dynamic programming (DP) matching method.
- Speaker-dependent isolated-word speech recognition system
- Word registration capacity: 128 words (with a 16K-byte basic memory) to 512 words (with a 64K-byte memory)
- Word length: 0.2 seconds - 2.0 seconds max.
- Grouping (syntax control): 128 groups max.
- Recognition response time: 0.5s on average

- Recognition accuracy: more than 98%
- Directly-connectable microphone
- Host interfaces:
  - Parallel interface using uPD8255A-5
  - RS-232C interface using uPD8251A
  - Serial Interface using uPD7762G serial port
- Available memory configuration:
  - 16K bytes (basic configuration)
  - 32K bytes
  - 48K bytes
  - 64K bytes (maximum)
- Simple command configuration using 12 types of commands

1.2 System Function

Three NEC chips, the MC-4760, uPD7761, and the uPD7762 integrate the functions necessary for speech recognition. Figure 1.1 shows a functional configuration diagram of these devices.

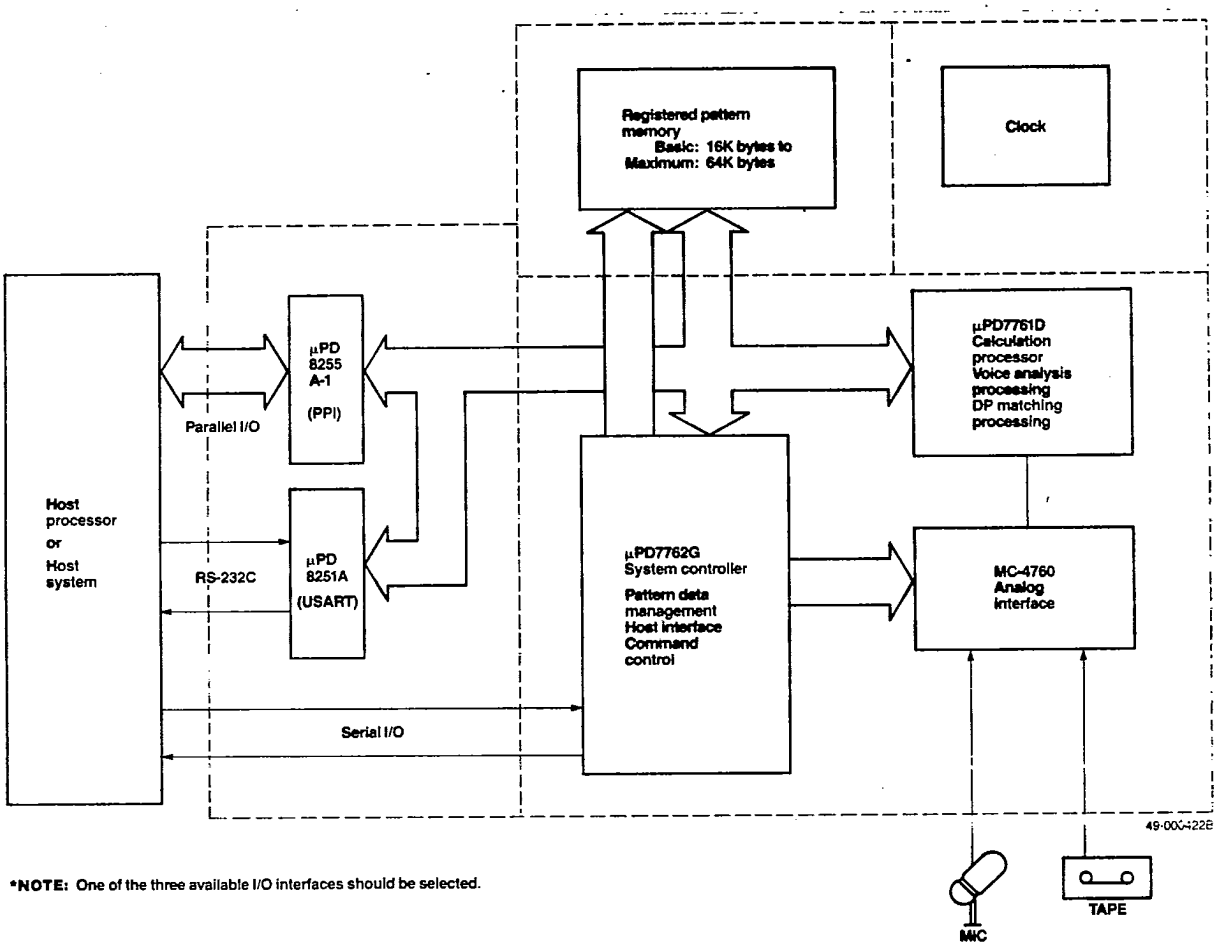
The MC-4760 analog interface accepts the speech input to the system. The uPD7762 functions as the system-level control processor. The uPD7761 operates as a dedicated arithmetic processor and performs analysis and matching calculations. The analysis process determines the energy content of the input speech data within specific frequency bands. The matching recognition process performs pattern matching calculations of the analyzed input speech against the predefined, or "registered" speech patterns.

The speech recognition chip can recognize single word inputs from a 128-word vocabulary by using a compressed dynamic programming (DP) method for pattern matching. The average response time is 0.5 seconds, with an accuracy of better than 98%. You may also use up to four resident vocabularies of 128 words each, allowing 512 words to be registered into the system. You can expand the active vocabulary storage (or "pattern memory") in increments of 16K bytes (128 spoken words) to a maximum of 64K bytes (512 spoken words). The current bank is selected by external command.

1.3 System Configuration

Figure 1.1 shows the basic configuration of a speech recognition system using the speech recognition LSI set (MC-4760, uPD7761D, and uPD7762G). The system consists of the speech recognition LSI set and registered pattern memory, system clock, and system interface blocks.

Figure 1.1 System Configuration



*NOTE: One of the three available I/O interfaces should be selected.

1.3.1 Analog Interface

The MC-4760 is a hybrid IC used as the analog interface. Its internal 8-bit A/D converter converts the analog speech signal input from the microphone to digital speech. It also contains a programmable attenuator (controlled from the uPD7762G) that calibrates the level of the analog speech signal input, as shown in Figure 1.2.

Two speech input terminals, MIC IN and LINE IN, allow you to connect a microphone directly to the MIC IN terminal. It is recommended that you use a close-talking type microphone that does not pick up surrounding noise, but almost any dynamic microphone will work. Impedance should be 200 ohms to 1 kohm (600 ohms, standard).

The G ADJ pin allows you to adjust the level of the input speech. The resistance connected between this pin and ground sets the optimum input level (see Figure 1.3).

The MC-4760 is discussed in detail in Chapter 5.

Figure 1.2 MC-4760 Block Diagram

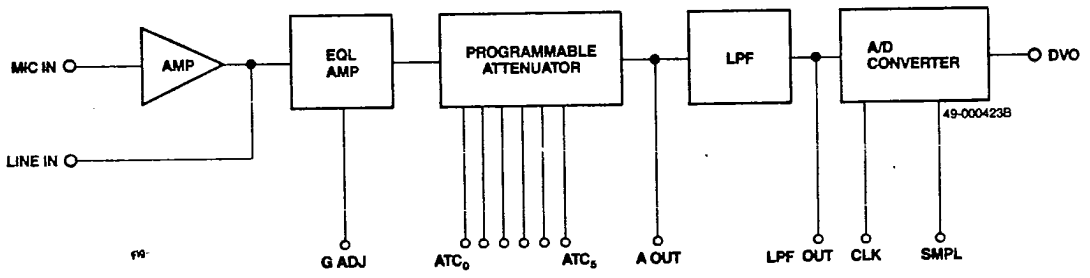


Figure 1.3 Speech Input

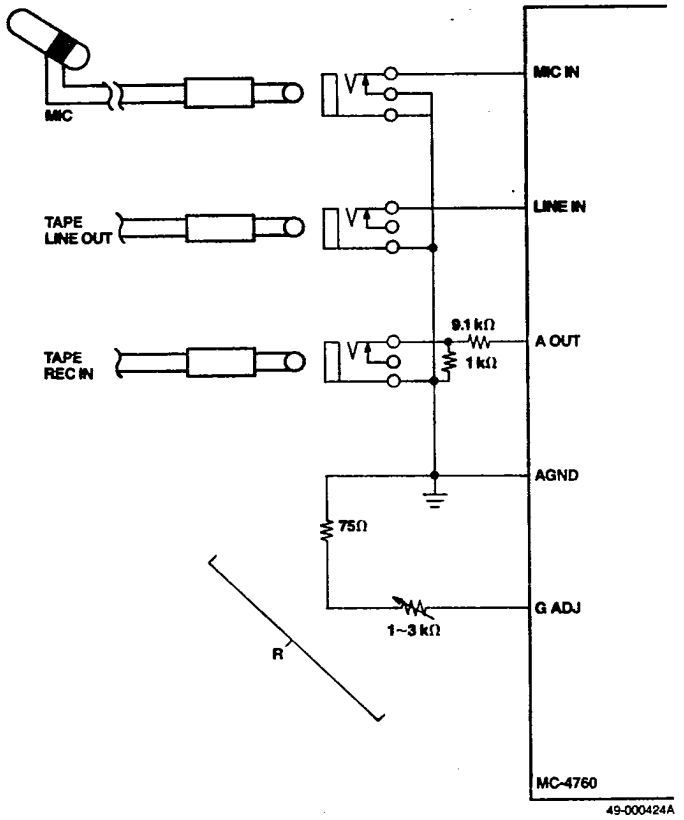


Table 1.1 Relation Between G ADJ Resistance and Input Sensitivity

R (Ω)	Equalizer Gain (V/V)	MIC IN (mV p-p)	LINE IN (V p-p)	Measuring Conditions:
Open	1.07	47.0	4.7	f = 1kHz
1100	3.16	16.0	1.6	V_{LPF0} = 5.0V p-p
510	5.58	9.0	.90	ATC_0-ATC_5 = All high
240	10.66	4.7	.47	level (gain = 1)
120	20.25	2.5	.25	
75*	31.0	1.6	.16	

* Note: Do not use a resistance of less than 75 ohms between G ADJ and ground.

1.3.2 Calculation Processor

The uPD7761D is an LSI used exclusively for calculations such as speech analysis and DP matching. To perform speech analysis, the speech pattern is extracted from the output of the MC-4760 (digital speech data) using an 8-channel digital filter. An 8-bit data bus connects the uPD7761D to the uPD7762G. This bus transfers speech analysis data, pattern data required for DP matching, and the result of the matching between the uPD7761D and the uPD7762G.

The uPD7761D is discussed in detail in Chapter 6.

1.3.3 System Control LSI

The uPD7762G receives commands from the host system and controls the speech recognition system according to those commands. Its functions include controlling the MC-4760 and uPD7761D, managing the registered pattern memory, and interfacing with the host computer.

The uPD7762G is discussed in detail in Chapter 7.

1.3.4 Other System Blocks

The Registered Pattern Memory stores the speech patterns extracted by the uPD7761D during training. It acts as a dictionary of registered word patterns. The memory is a configuration of banks of 16K bytes each. You may use up to four banks (64K bytes) of memory.

The System Clock section supplies the operating clocks of the speech recognition system.

The System Interface is the interface between the host system and the speech recognition system. Parallel, RS-232C, and Serial interfaces are available.

CHAPTER 2 SPEECH RECOGNITION SYSTEM CONFIGURATION EXAMPLE

This chapter describes an example of how to connect the speech recognition LSI set. Figure 2.1 shows this circuit example.

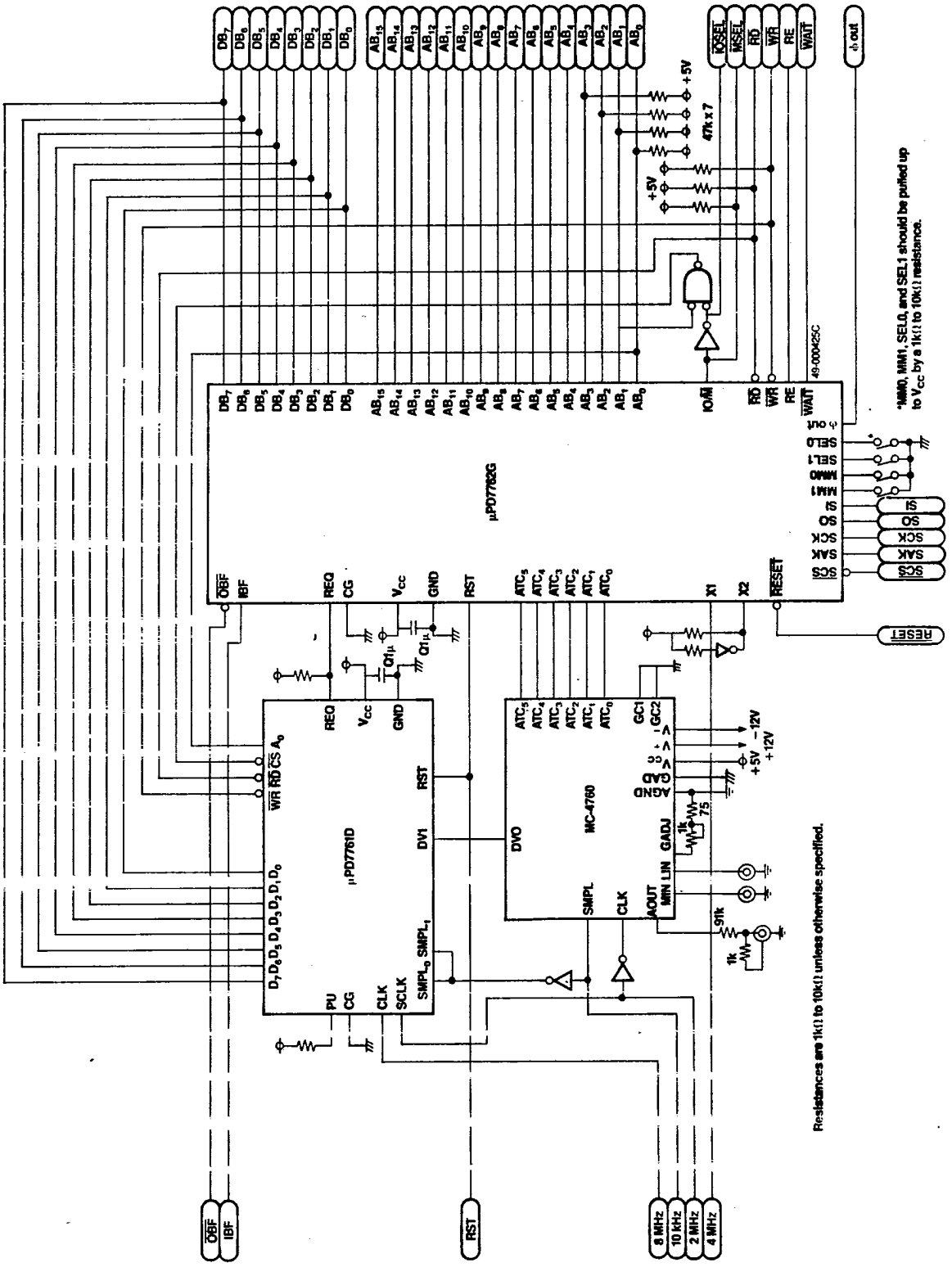
Since the MC-4760 is a hybrid IC designed to be used as an analog interface, you must carefully shield it against noise pulses in the digital lines. It is recommended that you use a single-point ground for each of separate analog and digital grounds (ground planes, if you use a PC board).

2.1 Power-on/Reset

The uPD7762G initializes the speech recognition system when power is applied. At initialization:

- level flags are reset for all memory banks set by the MM0 and MM1 pins of the uPD7762G (you must set the level flags by executing the LEVEL ADJUST command),
- the current bank is set to bank 0,
- all system interfaces are initialized (at this time, even if one or more interfaces are not connected, no error occurs),
- the ATC (attenuation control) values for the MC-4760, including GC1 and GC2 as the two LSBs, are initialized at 20H (input level is divided by 8.),
- and the uPD7761D is reset.

Figure 2.1 Circuit Example for the Speech Recognition LSI Set



2.2 Registered Pattern Memory

The registered pattern memory is a configuration of 16K-byte banks. You can use up to 64K bytes (see Figure 2.2). The state of the MM0 and MM1 pins of the uPD7762G specify the memory capacity as shown in Table 2.1.

Figure 2.2 Memory Bank Configuration

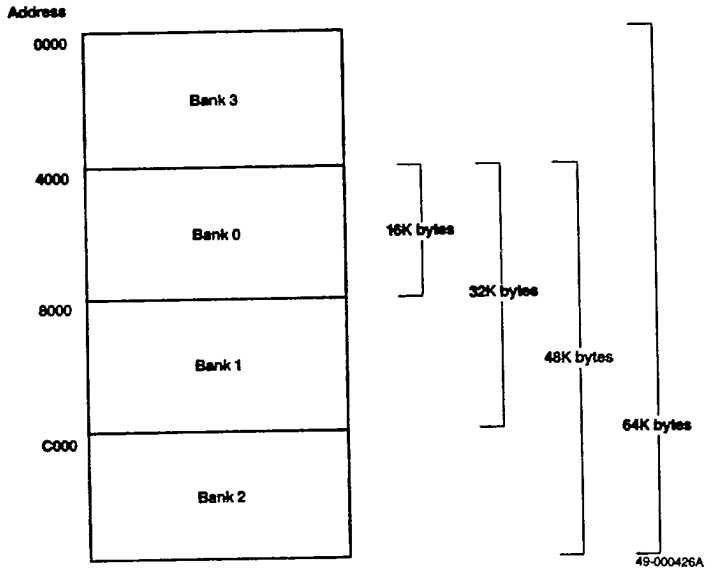


Table 2.1 Setting Memory Capacity

MM0	MM1	Memory size
L	L	64K bytes
L	H	16K bytes
H	L	32K bytes
H	H	48K bytes

H: High Level
L: Low level

2.2.1 Read Cycle

Figure 2.3 shows the timing for the memory read signal output from the uPD7762G. Note that a wait cycle is included in the read cycle timing. This is because when you input a 4MHz clock as the operating clock of the uPD7762G, the access time is only 350ns. Thus, to use a slow dynamic RAM (access time greater than 350ns), the read operation must include a wait cycle. Inserting a wait cycle extends the access time to 850ns, allowing you to use almost any dynamic RAM.

Figure 2.4 shows an example of this type of $\overline{\text{WAIT}}$ signal generating circuit.

Figure 2.3 uPD7762 Memory Read Timing

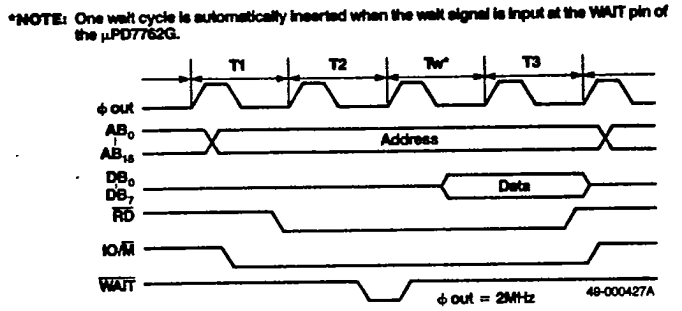
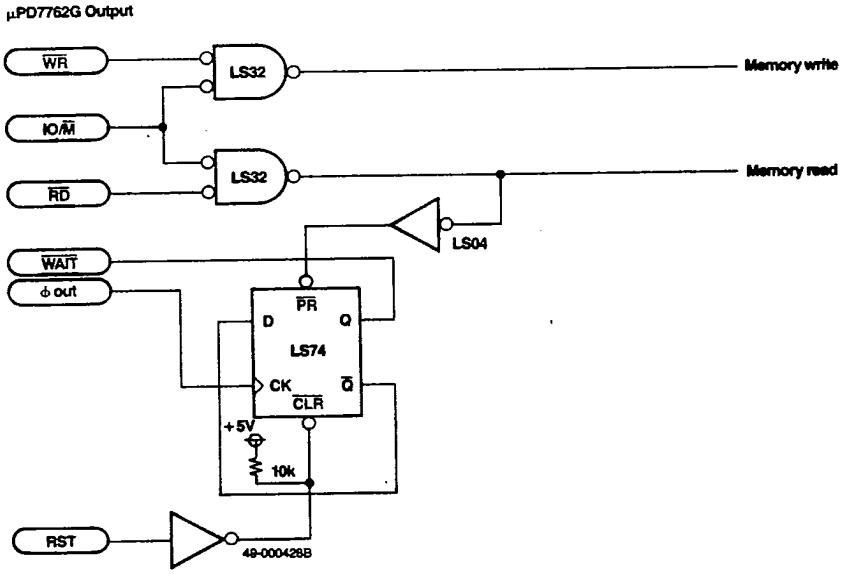


Figure 2.4 Generating One Wait Signal During Memory Read

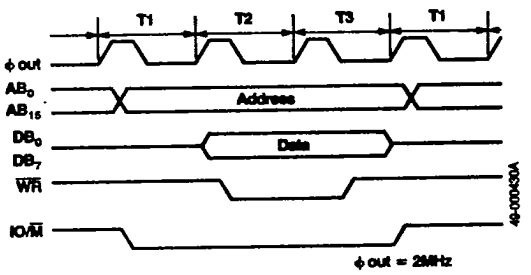


The uPD7762G senses the $\overline{\text{WAIT}}$ signal during the T2 State. If the signal is low, it inserts a wait cycle (TW). At the end of TW, it senses the $\overline{\text{WAIT}}$ pin; if it is low, another wait cycle is inserted. TW repeats as long as the $\overline{\text{WAIT}}$ signal is low.

2.2.2 Write Cycle

Figure 2.5 shows the timing of the memory write signal output from the uPD7762G. The write cycle differs from the read cycle in that no wait cycle is required. This is because when you use a 4MHz clock, a $\overline{\text{WR}}$ signal width of 600ns is assured and a normal RAM latches the data at the trailing edge of the $\overline{\text{WR}}$ signal.

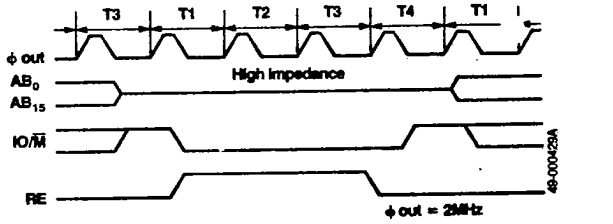
Figure 2.5 uPD7762G Memory Write Timing



2.2.3 Refresh Cycle

The Refresh Enable pin on the uPD7762G allows you to use a dynamic RAM for registered pattern memory. Figure 2.6 shows the timing for the RE pin. When the uPD7762G is not performing memory access, the RE pin outputs a high-level signal; the IO/$\overline{M}$ pin simultaneously outputs a low-level signal. At this time, the address bus of uPD7762G is held at high impedance.

Figure 2.6 uPD7762G RE (Refresh Enable) Timing



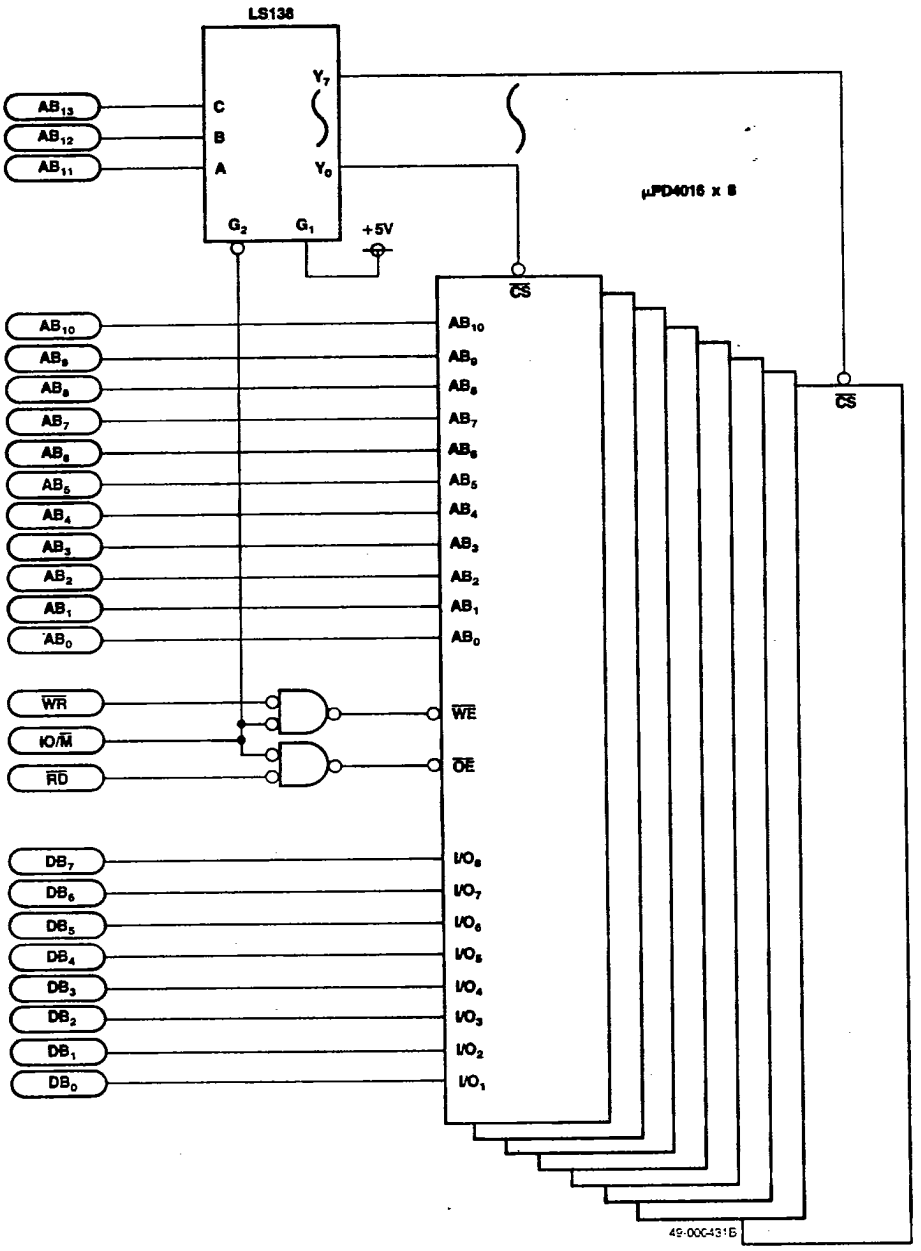
NOTE: The refresh cycle, unlike the read and write cycles, requires four machine cycles.

2.2.4 Static RAM

If you use uPD4016 static RAMs, the wait cycle described above is not required, obviating the need for the circuit shown in Figure 2.4.

Pull up the $\overline{WAIT}$ pin of the uPD7762G by a resistance of about 10kohm. Figure 2.7 shows an example of a circuit for registered pattern memory using uPD4016s.

Figure 2.7 Memory Configuration Using Static RAMs



2.3 System Clocks

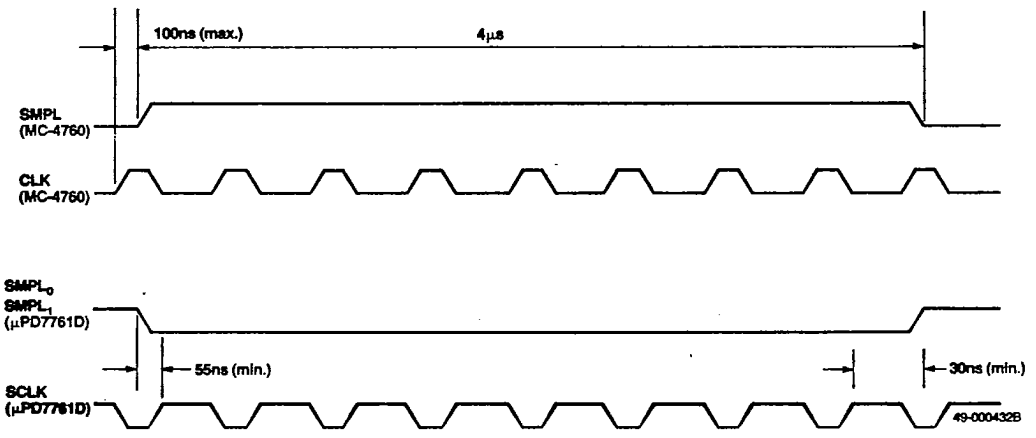
Table 2.2 shows the system clocks required by the speech recognition system.

Table 2.2 Clock Signals Supplied to the Speech Recognition Set

Device	Description	Frequency	Supply Terminal	Pin No.	Notes
uPD7761D	Operation Clock	8MHz	CLK	15	
uPD7762G	Operation Clock	4MHz	X1	31	
uPD7761D	Digital speech data serial input	2MHz	SCLK	18	
MC-4760	A/D operation	2MHz	CLK	3	Inverse phase of 7761's SCLK
MC-4760	A/D sampling clock	10kHz	SMPL	4	
uPD7761D	Sampling sync clock	10kHz	SMPL0 SMPL1	19 17	Inverse phase of 4760's SMPL

When you send digital speech data between the uPD7761D and the MC-4760, you must synchronize the 2MHz clock and the 10kHz clock (see Figure 2.8).

Figure 2.8 Clock Input Timing for uPD7761D and MC-4760

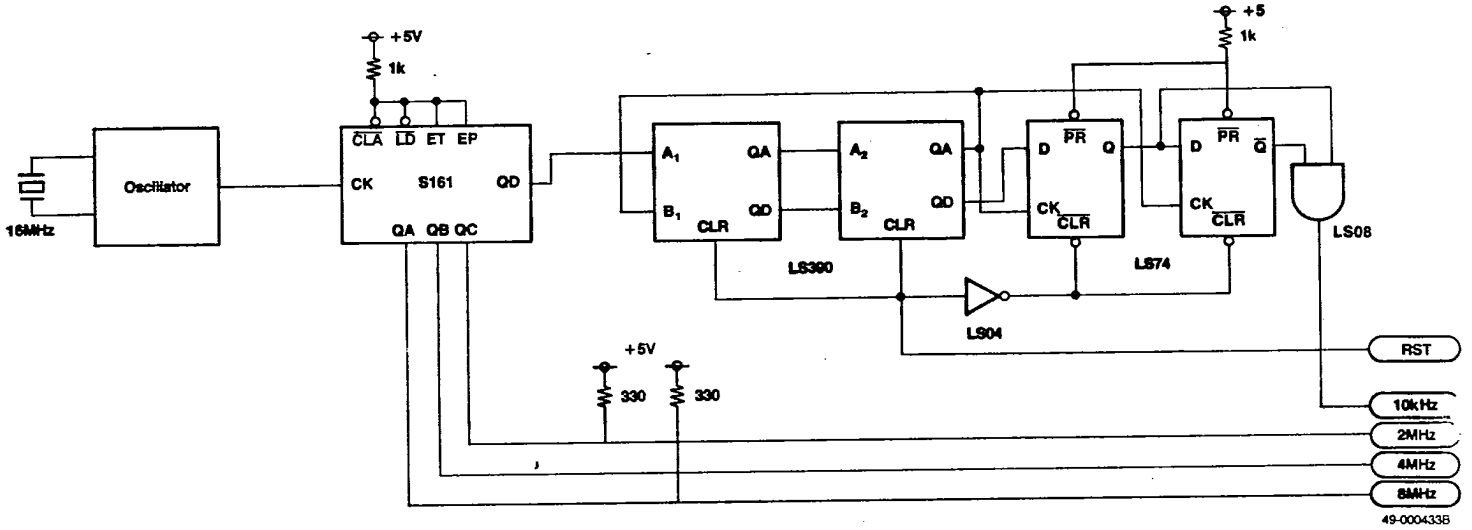


The 10KHz clock has an asymmetrical duty ratio of 1:24 (where 1 = high level). This clock is supplied to the MC-4760 and the inverse phase to the uPD7761D. (The duty ratio for all other clocks is 1:1.)

When reset (RST) is input to the uPD7761D, the 10KHz clock must also be cleared.

Circuits that generate each of these clocks are shown in Figure 2.9.

Figure 2.9 Clock Generating Circuits



2.4 System Interface

You can use three different types of system interfaces with the speech recognition LSI set. These interfaces allow you to perform data communication with the host system in 8-bit units. The uPD7762G manages the host interface. Parallel (uPD8255A-5), RS-232C (uPD8251A), and Serial (serial port of the uPD7762G) interfaces are supported.

Table 2.3 Interface Selection

SEL0	SEL1	Interface
L	L	uPD8255A-5 Parallel
L	H	uPD7762G Serial
H	L	Illegal
H	H	uPD8251A RS-232C

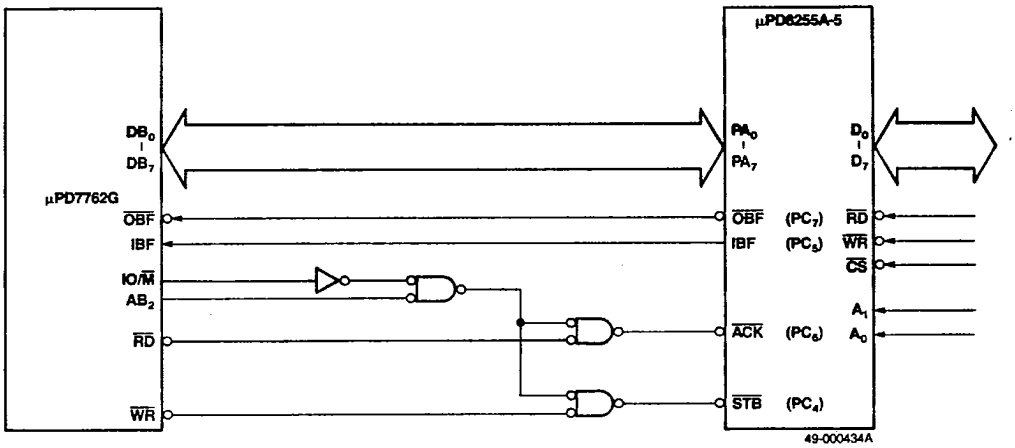
H: High level
L: Low level

2.4.1 Parallel Interface (uPD8255A-5)

The host system performs 8-bit parallel data communication via the uPD7762G and the uPD8255A-5. The uPD8255A-5 has three 8-bit ports referred to as ports A, B, and C. Bits 4 to 7 of port C with all port A bits are called group A, and bits 0 to 3 of port C with all port B bits are called group B. You can use the port C bits in these configurations to output control signals or to input status signals.

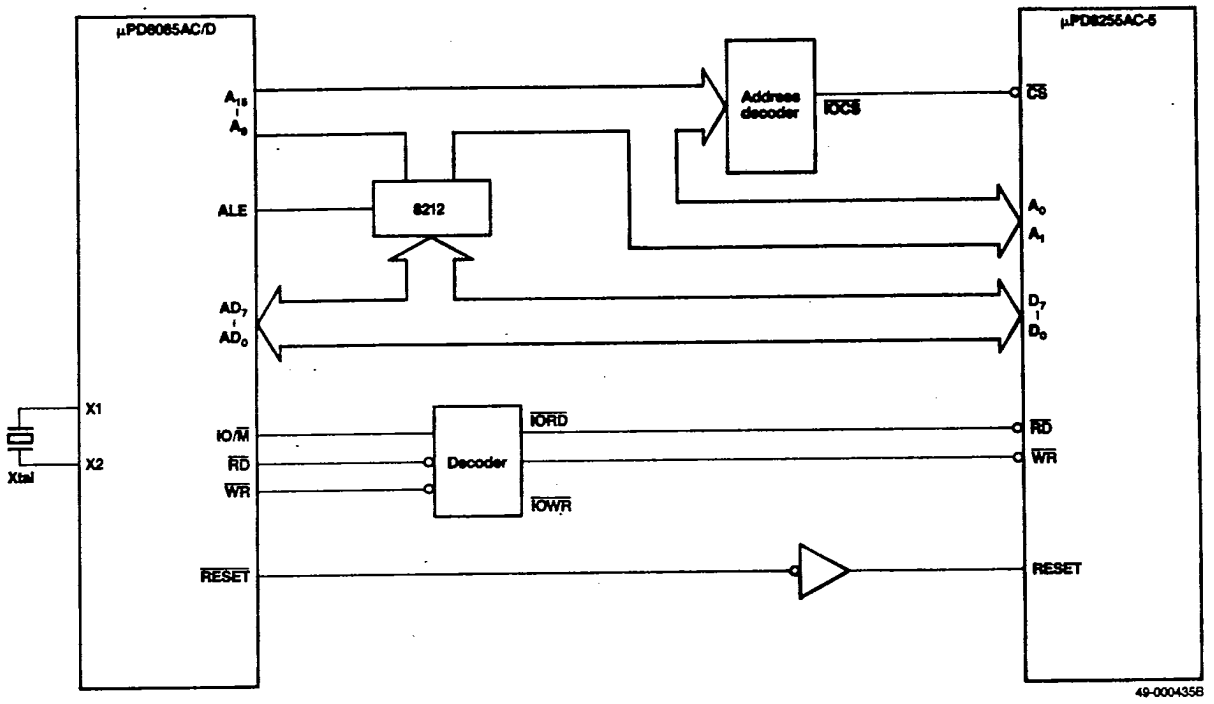
The uPD8255A-5 is supported as a peripheral device of the host. Therefore, set the bits of group A in mode 2. You can set the bits of group B in any mode. Figure 2.10 shows how to connect the uPD8255A-5 and the uPD7762G.

Figure 2.10 Parallel Interface



uPD7762G outputs IO/$\overline{M}$, AB_2 (active low) and $\overline{RD}$/$\overline{WR}$ generate the input signals for uPD8255A-5 pins ACK and STB. Also, the outputs of uPD8244A-5 pins $\overline{OBF}$ and IBF are input without change to uPD7762G pins $\overline{OBF}$ and IBF. Figure 2.11 shows a circuit example using a uPD8085A as the host.

Figure 2.11 Connecting uPD8085AC/D(-2) and PPI (uPD8255AC-5)

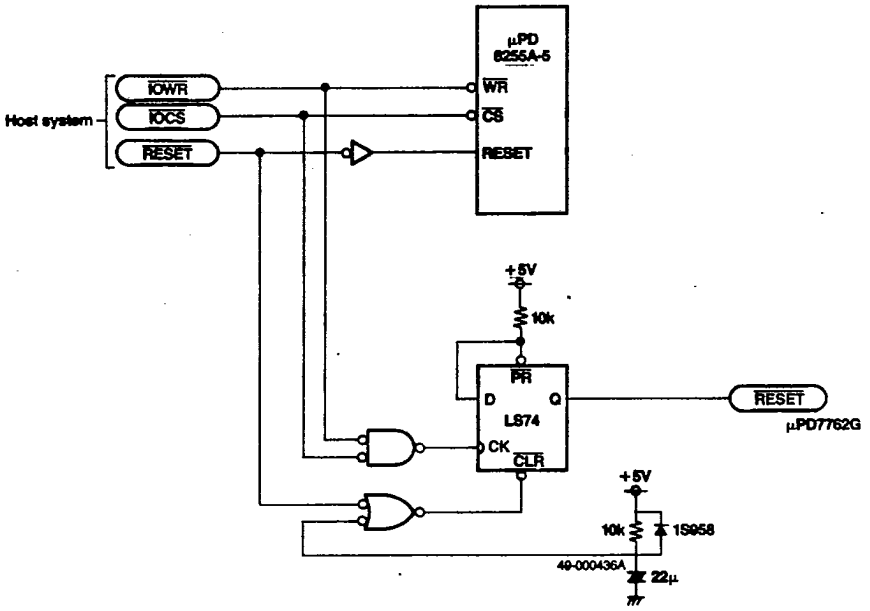


The $\overline{\text{RESET}}$ signal sent to the uPD7762G must be held at the active (low) level until the host system sets the mode for the uPD8255A-5. This is not necessary when you use the serial or RS-232C interface for the host interface.

Figure 2.12 shows a circuit example that performs this reset operation. In this circuit, the $\overline{\text{RESET}}$ signal to the uPD7762 rises after the initial write (of the mode setting code) has been received from the host system.

Note that there is a delay of approximately 80usec between the time you reset uPD7762 and the completion of mode setting for the external interface (at 4MHz). This delay time does not include initializing the management tables. The uPD7762 actually begins accepting commands after about 1.3 msec.

Figure 2.12 Reset Signal Synchronization Circuit



2.4.2 RS-232C Interface (uPD8251A)

When you use a uPD8251A (USART) as the host interface, the host system communicates with the uPD7762G in 8-bit units using the RS-232C communication standard. The uPD8251A is supported as a peripheral device of the uPD7762G. You must therefore provide another uPD8251A on the host side. Figure 2.13 shows the connection of a uPD7762G and uPD8251A.

The AB_3 and $IO/\overline{M}$ signals of the uPD7762G generate the $\overline{CS}$ signal of the uPD8251A. The AB_0 signal of the uPD7762G is used as the C/D signal of the uPD8251A. The uPD7762G sets the uPD8251A in the mode shown below. The mode and the setting at the host side must conform.

The uPD7762 issues a software reset to the uPD8251A before configuring it to the following specifications. Because some 8251As will not work if a software reset is issued immediately after a hardware reset, you should permanently ground the 8251A's RESET pin (hold it inactive) as shown in Figure 2.13.

uPD8251A operation mode specification:
(mode setting data = 0CFH)
Clock rate: baud rate x 64
(maximum baud rate = 4800 when CLK = 2MHz)
Word length: 8 bits
Parity: disabled (no parity)
Stop bits: 2 bits
Communication mode: asynchronous

Figure 2.13 Connecting the uPD8251A

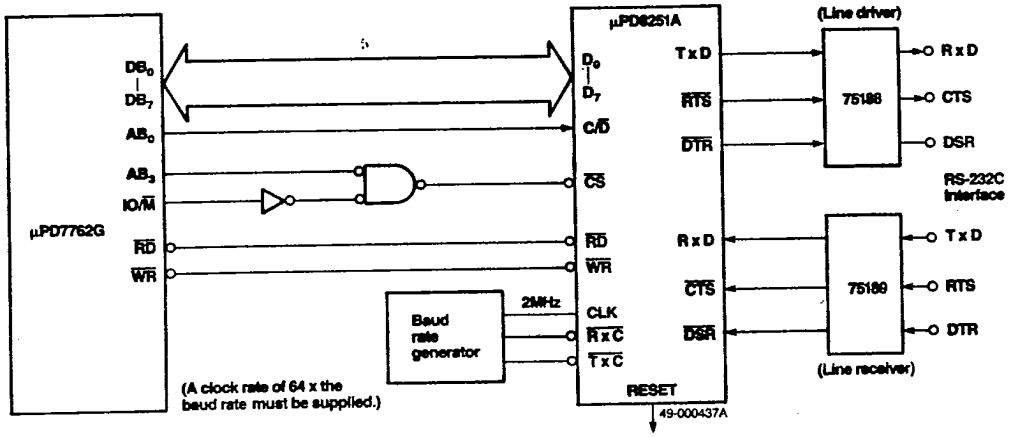
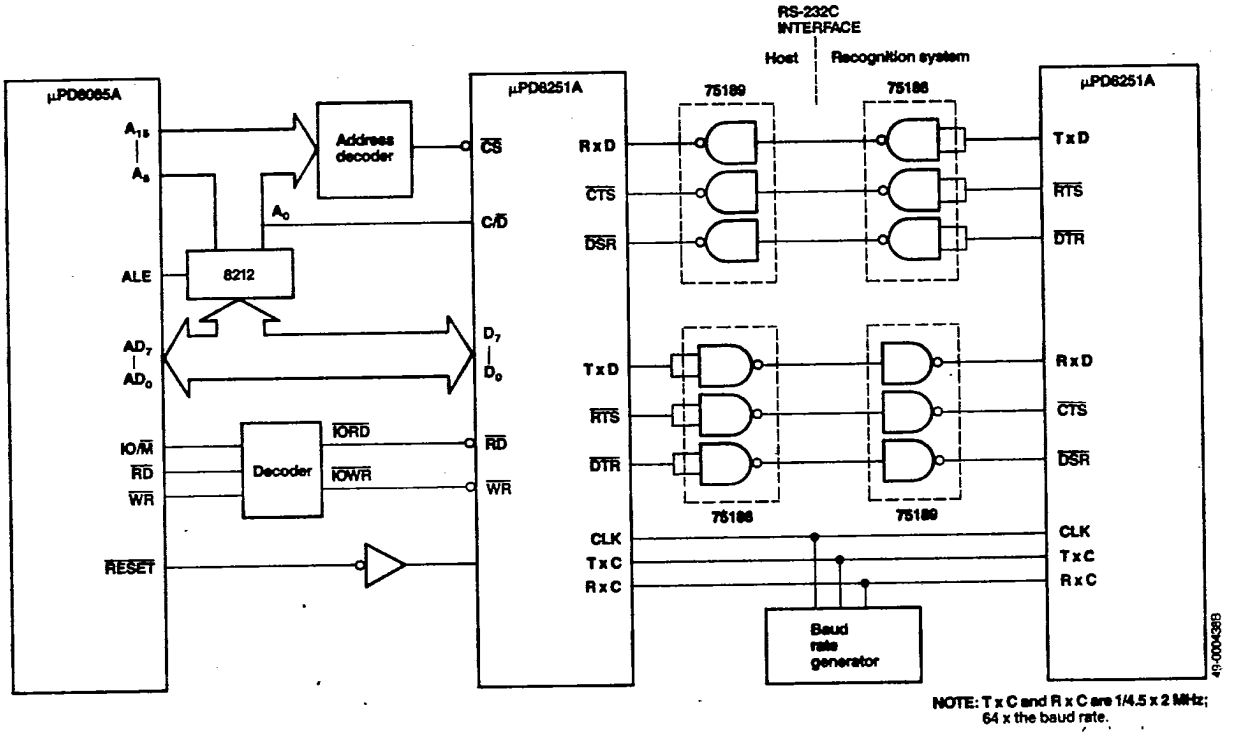


Figure 2.14 Connecting the uPD8085A and the uPD8251A

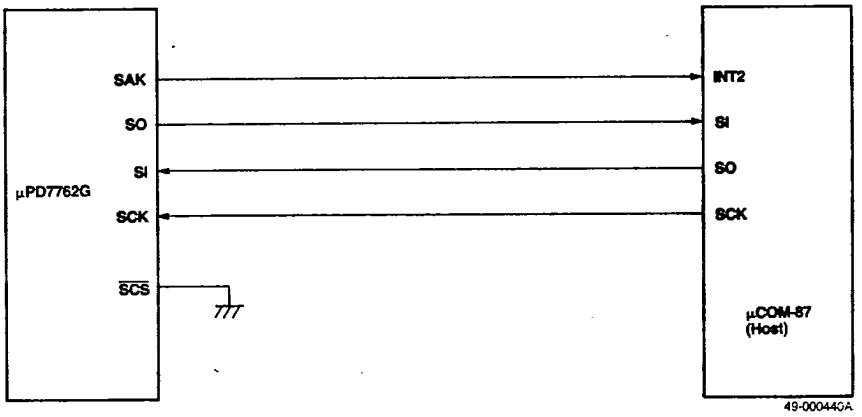


2.4.3 Serial Interface (uPD7762G Serial Port)

The uPD7762G has a serial I/O port that allows 8-bit data communication with a host system that has a port with the same timing. The serial I/O clock SCK is supplied from the host. In this mode, when the end of I/O operation is detected, the uPD7762G issues a low level SAK signal as confirmation.

When all the 8-bit data has been input or output from the serial register of the uPD7762G, the SAK signal goes low. Likewise, when internal data is fetched from the serial register of the uPD7762G or when data is rewritten to this register, the SAK signal goes high. The host system performs data I/O after confirming that the SAK signal has risen from low to high level. Figure 2.15 shows a connection example for the serial interface.

Figure 2.15 Connecting the uPD7762G Serial Port



Figures 2.16 and 2.17 show serial communication timing and the changing levels of SAK.

Figure 2.16 uPD7762G Serial Input (Host --> 7762)

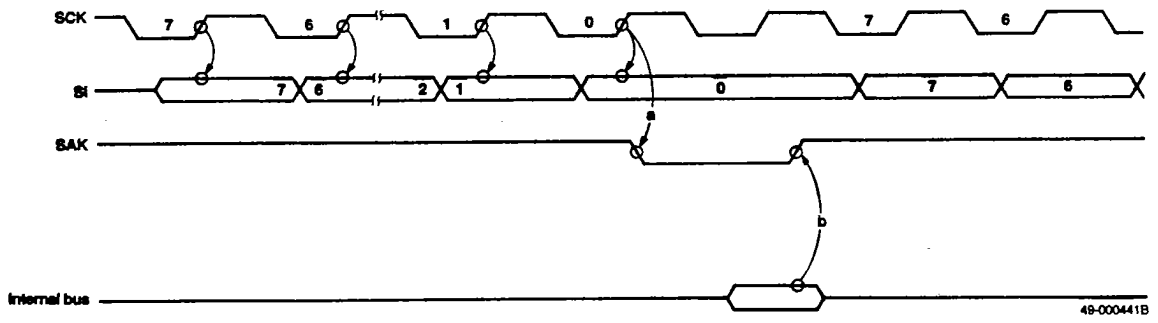
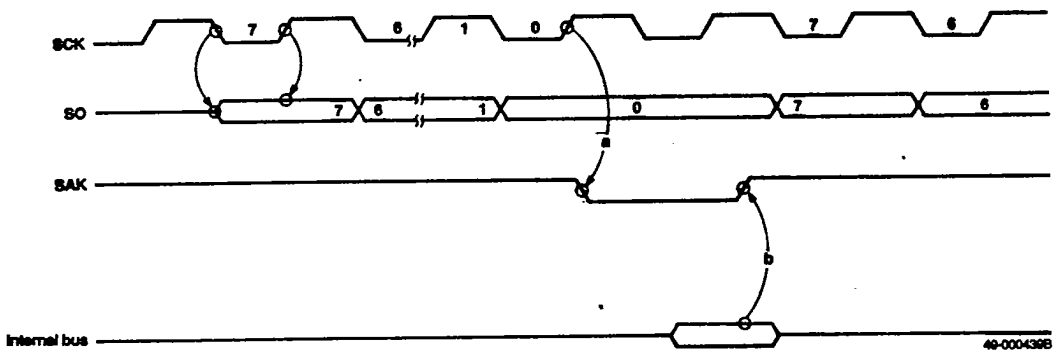
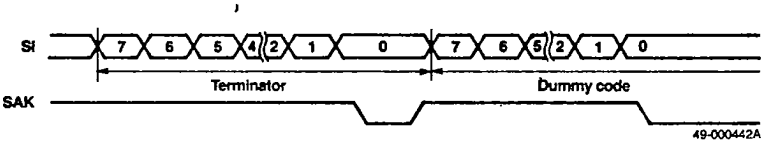


Figure 2.17 uPD7762G Serial Output (7762 --> Host)



When inputting commands from the host to the uPD7762, the host must send 00H as dummy data after it has sent the command terminator to the uPD7762G (see Chapter 3). This dummy data brings the SAK signal to low level (see Figure 2.18). If this operation is not performed as part of the command send, a subsequent output operation of the uPD7762G may send spurious data. No dummy data is sent during the output operation of the uPD7762G.

Figure 2.18 Dummy Code for Serial Input (7762 <-- Host)



CHAPTER 3 COMMANDS

The host system sends commands to the speech recognition system to control its operation. Commands consist of the command code (8-bit binary code), the required parameters, and the terminator code (0FFH).

3.1 Command Format

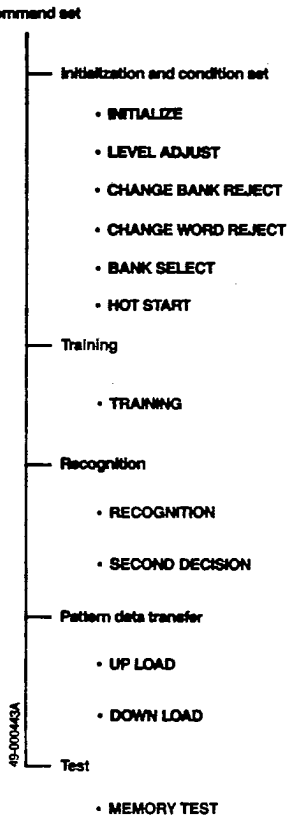
The uPD7762G has 12 commands as shown in Table 3.1. These commands can further be divided into four separate categories (Figure 3.1). In each of the formats shown in Table 3.1, 0FFH is the terminator and arguments in brackets are optional.

As noted before, after you reset the uPD7762 there is a delay of about 80usec until the mode is set for the external interface (at 4MHz operation). This delay does not include initialization of the management tables. The uPD7762 actually begins accepting commands about 1.3msec after reset.

Table 3.1 uPD7762G Commands

Command Name	Command Format
INITIALIZE	00H, 0FFH
LEVEL ADJUST	01H, [bank][bank][bank][bank], 0FFH
TRAINING	02H, registration number, [syntax number, word reject value], 0FFH
RECOGNITION	03H, [syntax number][...][syntax number], 0FFH
SECOND DECISION	04H, 0FFH
HOT START	05H, 0FFH
DOWN LOAD	06H, NUMBER OF PATTERNS, 0FFH
UP LOAD	07H, 0FFH (used as a pair with DOWN LOAD command)
CHANGE BANK REJECT	08H, bank reject value, 0FFH
MEMORY TEST	09H, 0FFH
BANK SELECT	0AH, bank, 0FFH
CHANGE WORD REJECT	0CH, registration number, word reject value, 0FFH

Figure 3.1 Organization of Commands



3.2 Commands

This section describes each of the commands available for the uPD7762. Arguments in brackets are optional. The following abbreviations are used in the command descriptions:

B Bank Number
D Distance Value
R Registration Number
Rv Reject Value
S Syntax Number

Each command results in a Status Output Code. A status result of 00H indicates the command was executed without error. Any other status result indicates an error. The status result codes possible for each command are shown in the command descriptions. Table 3.2 lists the Status Result codes.

Table 3.2 Status Output Codes

Code	Code Name	Description
00H	Acknowledge	Normal completion
01H	Level Over	Input speech level too high
02H	Level Under	Input speech level too low
03H	Time Over	Speech input longer than two seconds
04H	No Adjust	ATC values for the current bank have not been adjusted
05H	No Syntax	Specified syntax number does not exist
06H	No Pattern	Registered pattern does not exist
07H	No Data	The matching result (Distance Value) is greater than the bank reject value; matching pattern does not exist
08H	No Bank	Specified bank does not exist
09H	Invalid Command	Command format error
0AH	Reject Error	The matching result (Distance Value) is greater than the word reject value but less than the bank reject value
0BH	Too Short	Speech is too short
0CH	Memory I/O Error	Memory test error or hardware I/O error

3.2.1 Initialization and Condition Commands

BANK SELECT
Format: 0AH, B, 0FFH
Legal Values: 00H ≤ B ≤ 03H
Bytes: 3
Function: Selects the specified memory bank.
Action: Changes the ATC values of the MC-4760.
Status Result: 00H, 08H, or 09H

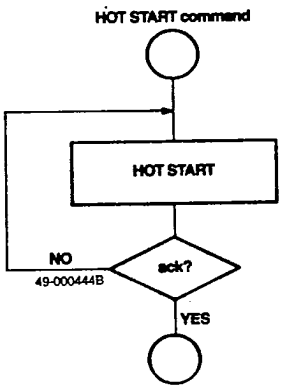
CHANGE BANK REJECT
Format: 08H, Rv, 0FFH
Legal Values: 00H ≤ Rv ≤ 0FEH
Bytes: 3
Function: Changes the reject value of the current memory bank. A value greater than the word reject value is normally set.
Status Result: 00H or 09H

CHANGE WORD REJECT
Format: 0CH, R, Rv, 0FFH
Legal Values: 01H ≤ R ≤ 80H
00H ≤ Rv ≤ 0FEH
Bytes: 4
Function: Changes the reject value for words that have already been registered.
Status Result: 00H or 09H. 09H is output if you specify a registration number above 80H.

HOT START

Format:	05H, 0FFH
Bytes:	2
Function:	Initializes the voice registration system while maintaining the registration patterns in memory. Use this command when the system interface has been changed or when the system stops because of error.
Actions:	Initializes the host interface. Resets the uPD7762.
Status Result:	00H or 09H

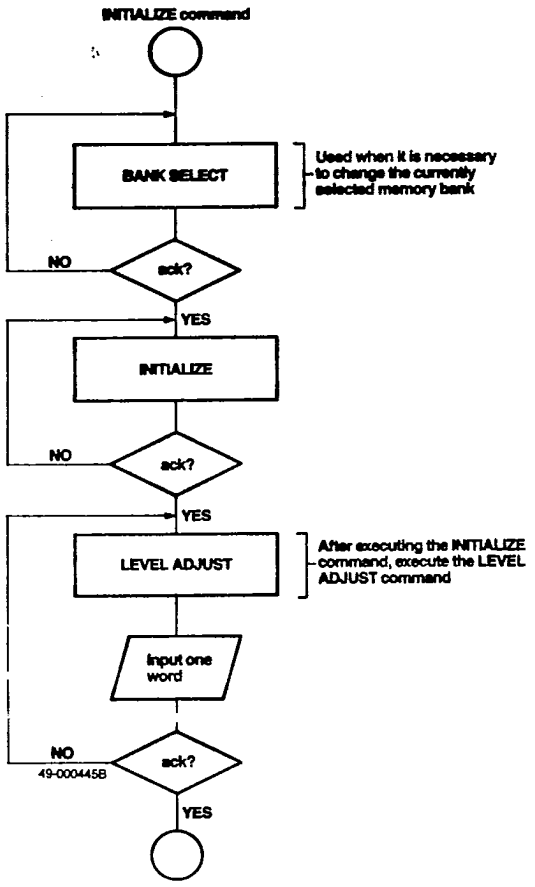
Figure 3.2 HOT START Command



INITIALIZE

Format:	00H, 0FFH
Bytes:	2
Function:	Initializes the speech recognition system while maintaining the current state of the system interface.
Actions:	Reset the uPD7761D, initialize the reject value for the current bank of the registered pattern memory (bank reject value = 0AH, word reject value = 0FEH), and initialize the ATC values for the MC-4760.
Status Result:	00H or 09H

Figure 3.3 INITIALIZE Command



LEVEL ADJUST

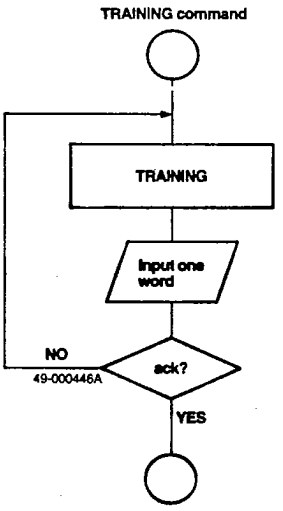
Format:	01H, [B], [B], [B], [B], 0FFH
Legal Values:	00H ≤ B ≤ 03H
Bytes:	2 - 6
Function:	Calibrates the ATC values of the MC-4760. You must issue this command after power is ON or after the INITIALIZE command has been executed.
Actions:	A speech signal is input and the ATC values are adjusted to obtain an appropriate input level. Resets the level flags of the specified memory banks. If you do not specify a bank, level flags are set for bank 0 and any other banks selected by MM0 and MM1.
Status Result:	00H, 01H, 02H, 08H, or 09H

3.2.2 Training Commands

TRAINING

Format:	02H, R, [S, Rv], 0FFH If you omit one of the two optional parameters, you should omit both.
Legal Values:	01H ≤ R ≤ 80H 00H ≤ S ≤ 80H (if omitted, 0) 00H ≤ Rv ≤ 0FEH (if omitted, 0FEH) If you specify a syntax number and reject value, these are set in the registration number table. If omitted, 0 and 0FEH are respectively assumed for the syntax number and reject value.
Bytes:	3 - 5
Function:	Performs registration of speech patterns. You must issue the LEVEL ADJUST command to calibrate the ATC values of the MC-4760 before executing this command. Once this calibration has been performed, you need not perform it again unless the system is initialized.
Actions:	Analyzes input speech data, converts it to a speech pattern, and registers the pattern with the registration number.
Status Result:	00H, 03H, 04H, 05H, 09H, or 0BH

Figure 3.4 TRAINING Command

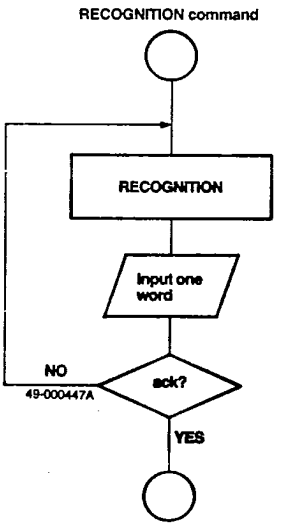


3.2.3 Recognition Commands

RECOGNITION

Format:	03H, [S],...[S], 0FFH You may specify up to 30 syntax numbers; if omitted, all syntax numbers are assumed. Syntax Group 0 is always assumed. See section 3.3 for a discussion of syntax groups.
Legal Values:	00H ≤ S ≤ 80H
Bytes:	2 - 32
Function:	Inputs speech data, compares it with the registered speech patterns, and outputs the result.
Actions:	Analyzes input speech data and converts it to a speech pattern. Performs matching calculation of the input pattern against all registered patterns with the specified syntax number(s) within the currently selected memory bank. Outputs the result of the matching calculation as the registration number of the pattern with the smallest distance from the input word, the distance value, and the status codes (00H or 0AH). These values are output one byte at a time to the host system. All registered patterns are matched if you do not specify a syntax number.
Status Result:	00H (followed by R and D), 03H, 04H, 05H, 06H, 07H, 09H, 0AH (followed by R and D), or 0BH

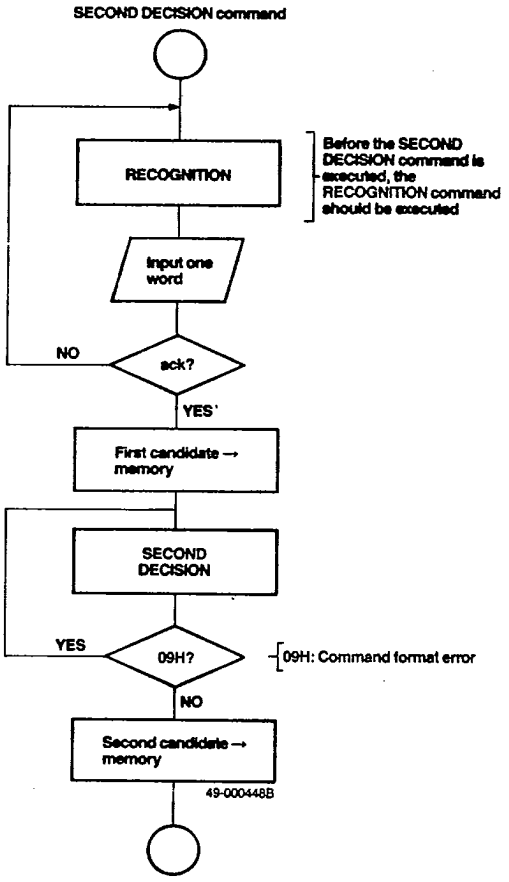
Figure 3.5 RECOGNITION Command



SECOND DECISION

Format:	**04H, 0FFH**
Bytes:	**2**
Function:	**After the recognition result is output, the registration number and distance value of the registered pattern with the next smallest distance are output to the host system following the status code (00H or 0AH). This command is valid only after the RECOGNITION command is executed.**
Status Result:	**00H (followed by R and D), 07H, 09H or 0AH (followed by R and D).**

Figure 3.6 SECOND DECISION Command



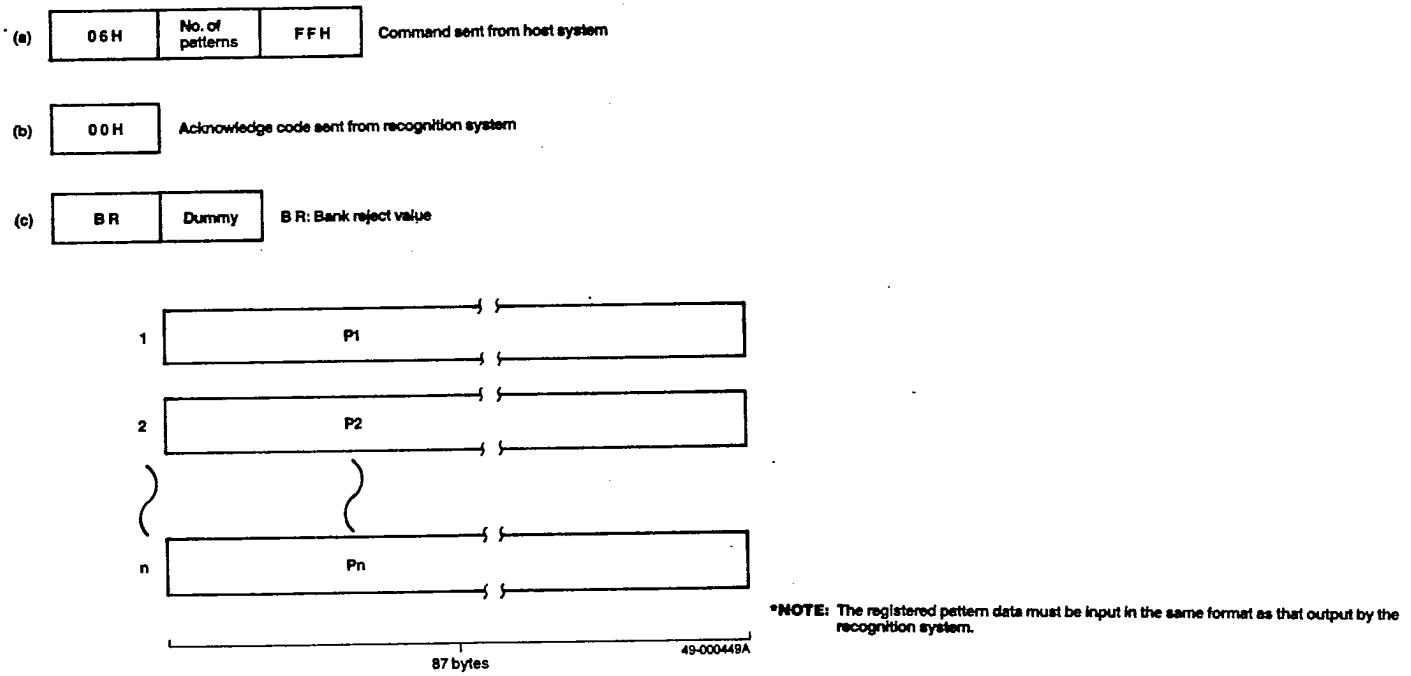
3.2.4 Pattern Data Transfer Commands

Use the UP LOAD and DOWN LOAD commands to transfer registered patterns between the recognition system and the host system.

DOWN LOAD moves patterns from the host system to the recognition system.
When you send a DOWN LOAD command from the host system, the recognition system responds with 00H (acknowledge).

The host system sends the bank reject value and terminator (1 byte each), followed by the pattern data (87 bytes per word). Assuming n as the number of patterns, (2 + 87 x n) bytes is the number of bytes sent from the host.

Figure 3.7 DOWN LOAD Command and Data Format

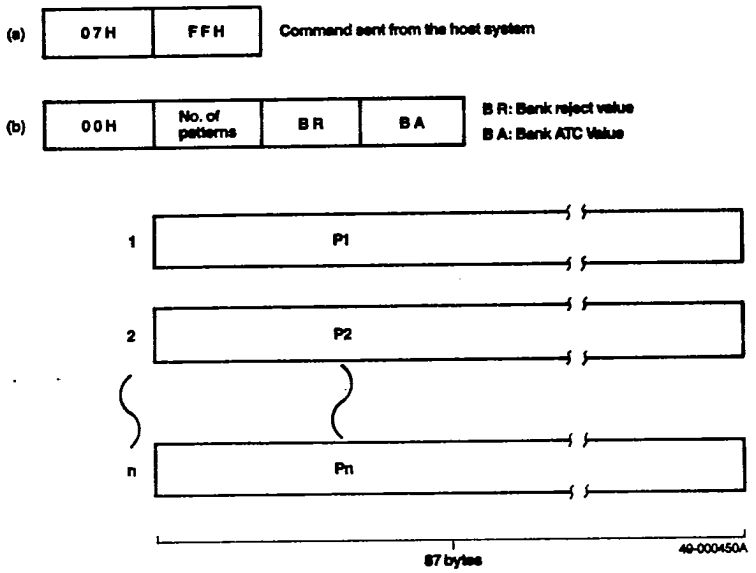


UP LOAD moves patterns from the recognition system to the host system.
When you send an UP LOAD command from the host system, the recognition system responds with 00H (acknowledge) and outputs the number of patterns, reject value, and bank ATC value. This data transfer is performed in byte units.

The recognition system outputs the registered pattern data (87 bytes per word) in the order of registration number, syntax number, word reject value, and pattern data.

Assuming n as the number of patterns, (3 + 87 x n) bytes is the number of bytes of data sent from the recognition system.

Figure 3.8 UP LOAD Command and Data Format

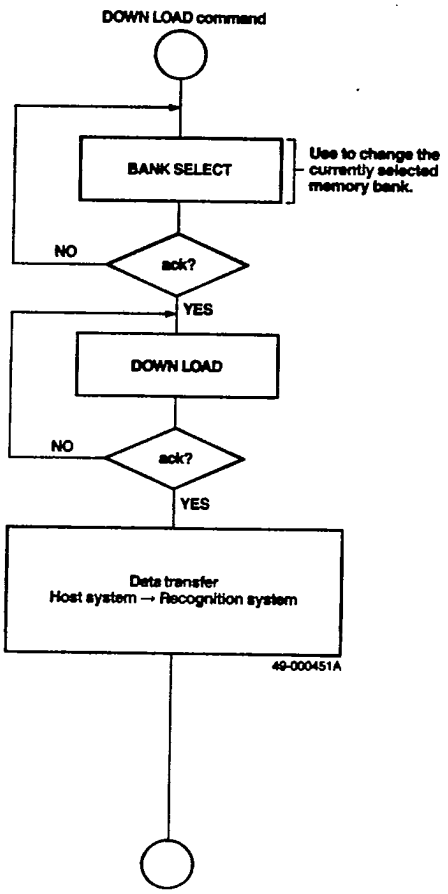


The registered pattern data must be input in the same format as that output by the recognition system.

DOWN LOAD

Format:	06H, Number of Patterns, 0FFH, Pattern List
Legal Values:	01H ≤ Number of Patterns ≤ 80H
Bytes:	3
Function:	Loads the registered patterns from the host system into the current memory bank. Number of patterns indicates the number of patterns to be sent from the host. It is not the registration number. If the number of patterns you specify as the second byte of this command is greater than the number of patterns actually sent, the next data sent (next command, etc.) is read as pattern data.
Status Result:	00H or 09H.

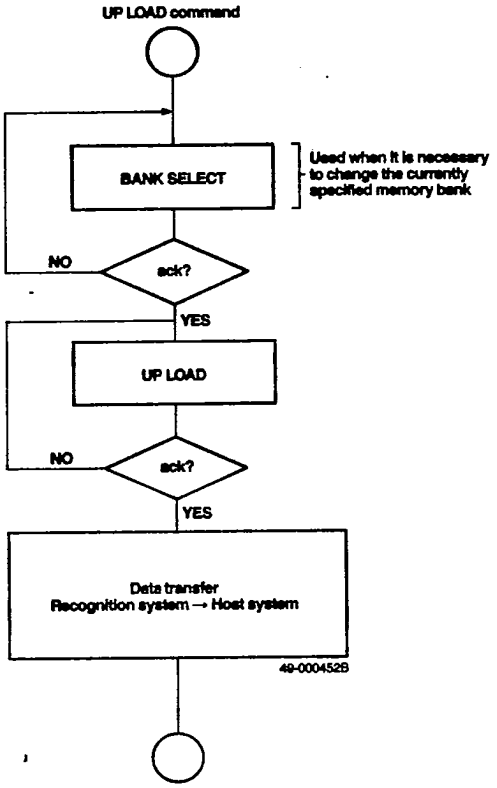
Figure 3.9 DOWN LOAD Command



UP LOAD

Format:	07H, 0FFH
Bytes:	2
Function:	Outputs the registered patterns in the current memory bank to the host system. This command is paired with the DOWN LOAD command to save and load registered patterns.
Status Result:	00H, 06H, or 09H

Figure 3.10 UP LOAD Command



3.2.5 Test Commands

MEMORY TEST

Format:	09H, 0FFH
Bytes:	2
Function:	Performs a read/write test of all memory banks set by the MM0 and MM1 pins of the uPD7762G. CAUTION: Since this command performs a read/write test of the memory, all registered patterns are destroyed.
Status Result:	00H, 09H, or 0CH

3.3 Syntax Groups

Set syntax groups by specifying a syntax number for words when registering the speech patterns. Specifying a syntax number when performing recognition reduces the number of words against which the input speech must be matched. You can also partition the registered vocabulary.

For example, given the following words:

Tokyo	Los Angeles
Hong Kong	Paris
Singapore	London
New York	Munich

the words are divided into three syntax groups: Asia (1), North America (2), and Europe (3).

Specifying the syntax group when performing recognition uses only those registered words with the specified syntax number as the object for matching calculation and recognition. To recognize an Asian place-name, specify syntax number 1 and recognition is performed by comparing the input word against registered words "Hong Kong," "Tokyo," and "Singapore." Table 3.3 lists the words with their registration numbers and syntax groups.

Table 3.3 Syntax Group Example

Word	Registration Number	Syntax Group
Hong Kong	1	1
Singapore	2	1
Tokyo	3	1
New York	4	2
Los Angeles	5	2
London	6	3
Paris	7	3
Munich	8	3

3.3.1 Using Syntax Group 0

As discussed in the descriptions of the Training and Recognition commands, if you do not specify a syntax group number, the command assumes a default value. The Training command defaults to Syntax Group 0. This means that a registered pattern is in syntax group 0 if you specified group 0 or if you did not specify a group.

The Recognition command defaults to ALL syntax groups. If you give this command without specifying a syntax group, EVERY registered pattern in the current bank is compared to the input speech regardless of its syntax group number. If you specify one or more syntax numbers in the command, syntax group 0 is always assumed to be in the list, even if you do not specify it explicitly. You can specify syntax group 0 alone, in which case it is the only group searched.

3.3.2 Examples of Syntax Group Use

Given that registered patterns exist in syntax groups 0, 1, 2, and 3, if you issue the Recognition command with:

Syntax Number 3, input speech is compared with patterns in groups 0 and 3.

Syntax Number 0, input speech is compared with patterns in group 0 only.

Syntax Number 4, input speech is compared with patterns in group 0.
The 05H error does NOT occur because the system found patterns in at least one of the syntax groups it searched, even though group 0 was only implicitly specified.

Syntax Numbers 1, 2, and 3 OR 0, 1, 2, and 3, OR no syntax numbers, input speech is compared with patterns in ALL syntax groups (0, 1, 2, and 3).

Given that registered patterns exist in syntax groups 1, 2, and 3 (none in group 0), if you issue the Recognition command with:

Syntax Number 3, input speech is compared with patterns in group 3 only.

Syntax Numbers 0 or 4, or both, the 05H error (no syntax) is produced.

3.4 Reject Values

Recognition is carried out based on a distance value obtained by comparing the input speech pattern with registered speech patterns. You can set the maximum permissible distance value (valid range) for recognition when you register the standard patterns. Recognition then occurs when the distance between the patterns is within the range specified by the reject value. The result is output as the registration number and distance value of the word with the smallest distance value from the input speech pattern.

If the distance between all patterns is greater than the reject value, the result is invalid and output as an error code. There are two reject values: the bank reject value, set for each memory bank, and the word reject value, set for each registered word. When both reject values are specified, recognition is performed based on the smaller of the two values. When you expect a large distance value, set a large reject value for the word. This improves the recognition rate.

Table 3.4 Sample Reject Values

Word	Bank	Word Reject Value	Bank Reject Value	Effective Reject Value
a	0	06	07	06
b	0	08	07	07
c	0	09	07	07
d	1	06	09	06
e	1	08	09	08
f	1	0A	09	09

CHAPTER 4 OPERATION EXAMPLES

This chapter provides program examples for data handlers and command operations of the host system. Although program details may vary depending on the host system, you can use the same method for any system.

4.1 Standard Operation

The LEVEL ADJUST, TRAINING, and RECOGNITION commands are essential for speech recognition operation. The other commands improve the effectiveness of the recognition system.

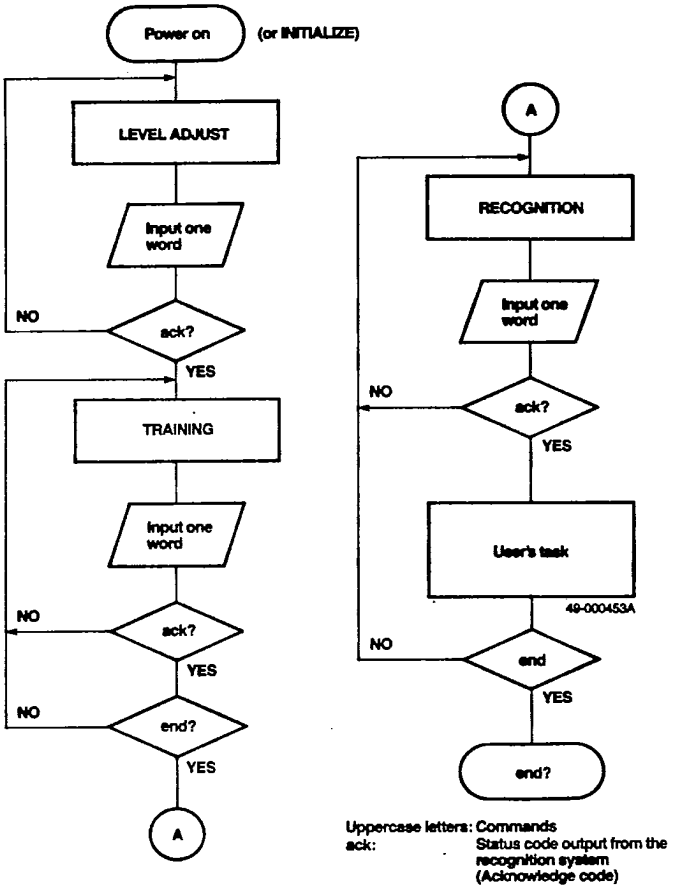
Figure 4.1 shows the flowcharts for each of these commands. You must use the LEVEL ADJUST command after power up or initialization (INITIALIZE) to set the speech signal input level of the recognition system to the speech level of the user.

You must repeat the LEVEL ADJUST command until 00H (acknowledge) is returned as the status. The chip set adjusts the level itself. If it returns 01H or 02H (level over or under), do not change the input signal level. Instead, repeat the command and the speech input until the chip set correctly adjusts the level.

You need only adjust the level once until the system is either reset or initialized again. Registration of the standard patterns is performed next.

You can register up to 128 words in each memory bank. You do not have to assign registration numbers in order. Registration of the required words is the final preparation for system operation. Thereafter, you can use the recognition system as an input device to the host system, using the registration number output as the result of the recognition to specify the type of processing to be performed (see Figure 4.1).

Figure 4.1 Standard Operation Example



4.2 Data Handler

Use the data handler described here when commands are being sent to the recognition system. The following is an example of this type of data handler adjusting the speech level. The host is a uPD8085A. All routines given below are described in 8085A assembly language.

A different host would require essentially the same procedure.

```
0000  3E01          LEVEL:   MVI     A,01H     ;Command code
0002  CD1600                 CALL    DOUT      ;Call handler
                                               (out)
0005  3E00                   MVI     A,00H     ;Select Bank 0
0007  CD1600                 CALL    DOUT      ;Call handler
                                               (out)
000A  3EFF                   MVI     A,0FFH    ;Terminator
000C  CD1600                 CALL    DOUT      ;Call handler
                                               (out)
000F  CD1800                 CALL    DINP      ;Call handler
                                               (in)
0012  C20000                 JNZ     LEVEL     ;If ACC=0 then
                                               next
                      :
0015  C9              NEXT:  RET
                      :
```

4.2.1 uPD8255A-5 (Parallel)

Mount a uPD8255A-5 as a peripheral device of the host system. The host performs initialization and other operations.

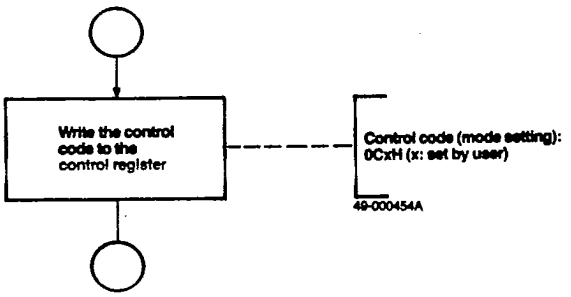
The following is a program example for initialization, data output, and data input. These handlers check the state (OBF, IBF) of port C of the uPD8255A-5 by to perform data transfer with bidirectional handlers.

Address assignments in the uPD8255 are as follows: 80H is port A, 81H is port B, 82H is port C and 83H is the control address. Figure 4.2 shows the initialization procedure, Figure 4.3 shows the data output procedure, and Figure 4.4 shows the data input procedure.

Initialization (I/O Condition: none)

```
0000  3EC2          INIT:    MVI     A,0C2H    ;0C2H = Mode 2
0002  D383                   OUT     83H       ;83H = Control
0004  C9                     RET               ;Return
```

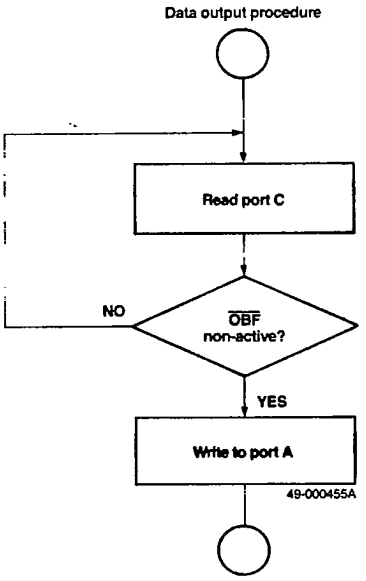
Figure 4.2 uPD8255 Initialization Procedure



Data Output (I/O Condition: Input: ACC = Output Data; Output: none)

```
0005  F5          DOUT:   PUSH    PSW       ;Save
                                              accumulator
0006  DB82                IN      82H       ;82H = Port C
0008  E680                ANI     80H       ;80H = Mask
                                              data
000A  CA0600              JZ      DOUT + 1  ;OBF Status
                                              check
000D  F1                  POP     PSW       ;Restore
                                              accumulator
000E  D380                OUT     80H       ;80H = Port A
0010  C9                  RET               ;Return
```

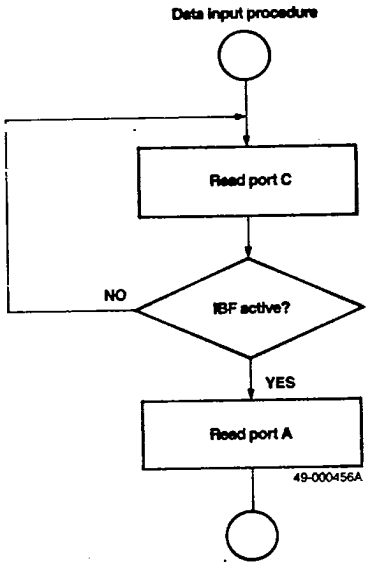
Figure 4.3 uPD8255 Data Output Procedure



Data Input (I/O Condition: Input: none; Output: ACC = Return Code)

```
0011  DB82          DINP:   IN      82H     ;82H = Port C
0013  E620                  ANI     20H     ;20H = Mask data
0015  CA1100                JZ      DINP    ;IBF Status check
0018  DB80                  IN      80H     ;80H = Port A
001A  C9                    RET             ;Return
```

Figure 4.4 uPD8255 Data Input Procedure



4.2.2 uPD8251A (RS-232C)

Place uPD8251As in the host and recognition systems. Data transfer is performed between these interfaces.

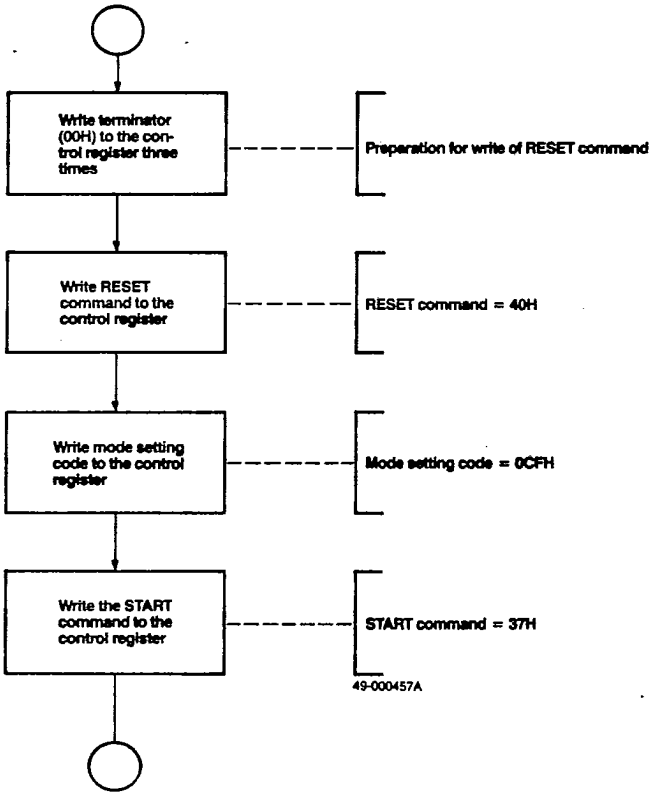
The following is a program example for initialization, data output, and data input. These handlers check the uPD8251A status data by software.

Address assignments in the uPD8251A are as follows: 80H is the data register address, 81H is the command/mode address, and 82H is the status address. Figure 4.5 shows the initialization procedure, Figure 4.6 shows the input procedure example, and Figure 4.7 shows the output procedure.

Initialization (I/O Condition: none)

```
0000  AF        INIT:   XRA     A       ;Clear
                                        accumulator
0001  D381                OUT     81H     ;Dummy
0003  D381                OUT     81H     ;
0005  D381                OUT     81H     ;
0007  3E40                MVI     A,40H   ;Reset USART
0009  D381                OUT     81H     ;CMO Output
000B  3ECF                MVI     A,0CFH  ;Mode select
000D  D381                OUT     81H     ;Mode set
000F  3E37                MVI     A,37H   ;Start command
0011  D381                OUT     81H     ;CMO Output
0013  C9                  RET             ;Return
```

Figure 4.5 uPD8251A Initialization Procedure

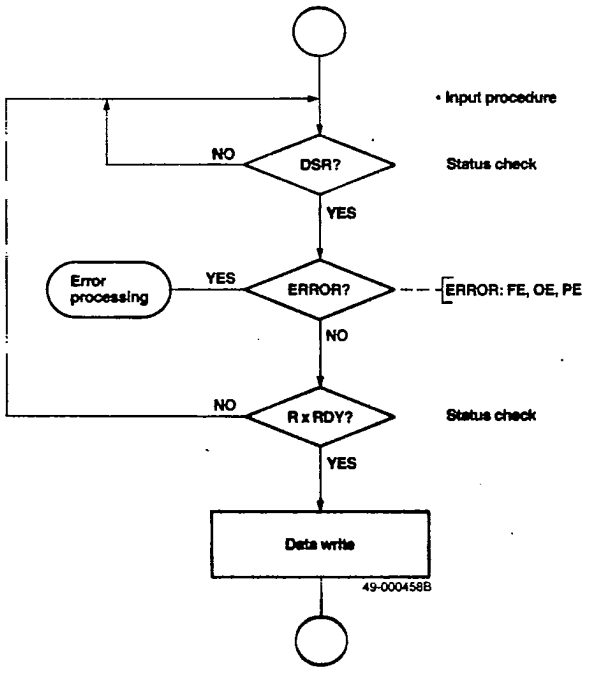


NOTE: In this flowchart, use is assumed of μPD8251As at both the host system and the recognition system.

Data Input (I/O Condition: Input: ACC = Output data; Output: none)

```
0014  F5          DOUT:   PUSH    PSW       ;Save
                                              accumulator
0015  DB81                IN      81H       ;Status input
0017  F5                  PUSH    PSW       ;Save status
0018  E680                ANI     80H       ;80H = DSR
                                              Mask
001A  C22100              JNZ     DOUT1     ;DSR check
001D  F1                  POP     PSW       ;Restore
                                              status
001E  F21500              JP      DOUT+1    ;
                ;
0021  F1          DOUT1:  POP     PSW       ;Restore
                                              status
0022  E601                ANI     01H       ;01H = TxRDY
                                              mask
0024  CA1500              JZ      DOUT+1    ;TxRDY check
0027  F1                  POP     PSW       ;Restore
                                              accumulator
0028  D380                OUT     80H       ;Data output
002A  C9                  RET               ;Return
```

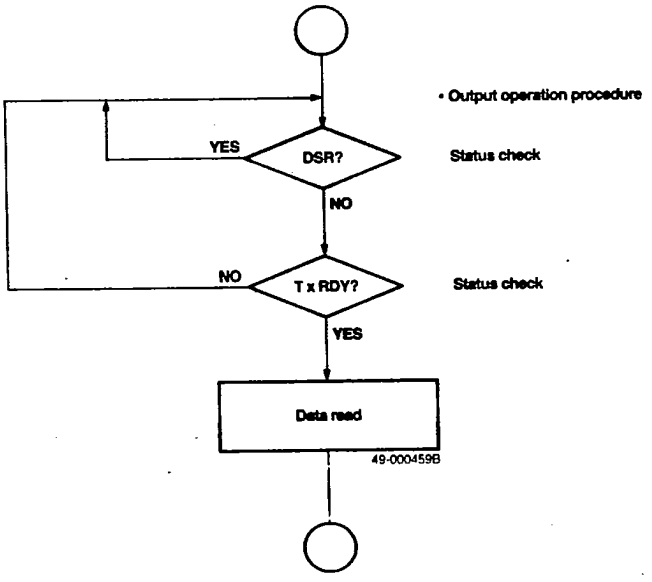
Figure 4.6 uPD8251A Input Procedure



Data Output (I/O Condition: Input: none; Output: ACC = Return data)

```
002B  DB81        DINP:   IN      81H     ;Input status
002D  F5                  PUSH    PSW     ;Save status
002E  E680                ANI     80H     ;80H = DSR mask
0030  C23700              JNZ     DINP1   ;DSR check
0033  F1                  POP     PSW     ;Restore status
0034  F22B00              JP      DINP    ;
                ;
0037  F1          DINP1:  POP     PSW     ;Restore status
0038  F5                  PUSH    PSW     ;Resave status
0039  E638                ANI     38H     ;38H = Error mask
003B  C24700              JNZ     IOERR   ;Error check
003E  F1                  POP     PSW     ;Restore status
003F  E602                ANI     02H     ;02H = RxRDY mask
0041  CA2B00              JZ      DINP    ;RxRDY check
0044  DB80                IN      80H     ;Input return code
0046  C9                  RET             ;Return
                ;
0047  00          IOERR:  NOP
```

Figure 4.7 uPD8251A Output Procedure



CHAPTER 5 USING THE MC4760 ANALOG INTERFACE

The MC-4760 is an integrated speech input circuit that performs conditioning and digital sampling of speech band signals. It is a 24-pin hybrid component that supplies all the functions for interfacing an external speech source to the speech recognition system. The component can support a microphone or a tape source as an input device, eliminating the need for external interfacing circuitry.

Figure 1.2 in Chapter 1 is the MC-4760 block diagram. A preamplifier front end interfaces speech from the microphone input to the device. A built-in variable gain amplifier (which equalizes the input) amplifies the input speech signal. Set the gain of the amplifier by connecting it to an external resistor. A digitally-controlled attenuator (which compensates for variations in the signal level due to microphone positioning and input voice level fluctuations) further adjusts the gain of the input speech signal. The uPD7762 control processor sets the attenuator gain in response to the LEVEL SET command. The gain is not continuously varied.

The input is then low-pass filtered by an antialiasing filter and input to a built-in A/D converter. The A/D converter samples the speech signal at a 10kHz rate and produces 8-bit converted samples by a logarithmic transfer function. The speech data samples are serially output to the uPD7761 analysis and matching processor, MSB first, at a serial bit rate of 2MHz. Design details for the microphone preamplifier, equalization amplifier, and attenuator control are described below.

5.1 Microphone Preamplifier

The input amplifier that interfaces the speech signal from a microphone source has the following specifications:

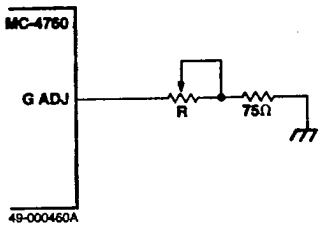
Gain:	40dB (100 v/v)
Input impedance:	1 kohm
Band pass:	100Hz to 10kHZ

Recognition accuracy varies with the noise environment and the microphone used. The system is intended for use with normal (dynamic) microphones with an impedance of 200 ohms to 1 kohm (including the standard 600 ohms). You may use an omni-directional microphone in quiet environments, but you should use a directional, noise-cancelling microphone for better results.

5.2 Equalization Amplifier

The equalization amplifier is a variable gain amplifier; set the gain by connecting an external resistor. You should set the amplifier so that the input signal level is within the dynamic range of the device. If you use a variable resistance, you should connect a 75 ohm resistance as shown in Figure 5.1. Note that you should connect the external gain setting resistance to analog ground (GNDA).

Figure 5.1 External Resistance Connection for G ADJ



The gain of the equalization amplifier is determined by the formula

$$G = 20 \log \frac{[18.49/R] + 8.6}{10} + 1.9$$

Where G = gain (dB), and R = resistance (k ohms). R must be at least 75 ohms.

5.3 Attenuator Control

The MC-4760 has an internal attenuator, digitally controlled by an 8-bit input port. The attenuator input terminals (ATC_0 to ATC_5) are TTL-level digital inputs. The LEVEL SET command from the host system sets ATC_0-ATC_5. The uPD7762 controls these inputs via its corresponding 6-bit attenuator control output port. The two low-order inputs, GC2 and GC_1, are tied to ground. Figure 5.2 shows these connections. Table 5.1 shows the relationship of the attenuator control input values to the output voltage. Note that the resolution of the attenuator step increments is: $(2^{-6})V_{REF}=(V_{REF}/64)$, where V_{REF} is the voltage being input to the attenuator.

Figure 5.2 Attenuator Control Terminal Connections

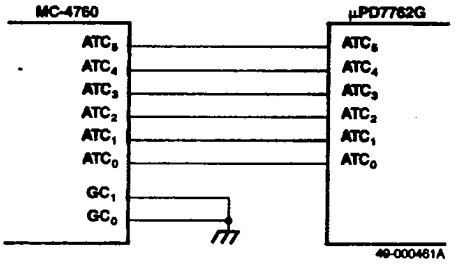


Table 5.1 Attenuator Control Values and Output Voltage

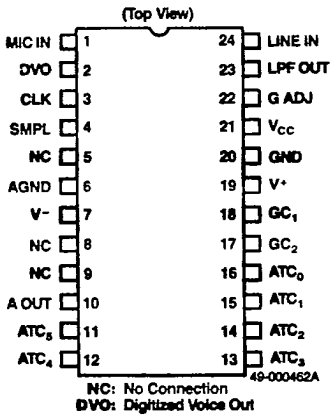
Attenuation	ATC_5	ATC_4	ATC_3	ATC_2	ATC_1	ATC_0	GC_1	GC_2
Divide by 1 (252/256)	1	1	1	1	1	1	0	0
Divide by 2 (128/256)	1	0	0	0	0	0	0	0
Divide by 4 (64/256)	0	1	0	0	0	0	0	0
Divide by 8 (32/256)	0	0	1	0	0	0	0	0
Divide by 16 (16/256)	0	0	0	1	0	0	0	0
Divide by 32 (8/256)	0	0	0	0	1	0	0	0
Divide by 64 (4/256)	0	0	0	0	0	1	0	0
No signal (0/256)	0	0	0	0	0	0	0	0

Note that the GC_1 and GC_2 inputs are normally grounded. They are actually the two LSBs of the digital attenuator. Divide by 8 is the default value set by the uPD7762 immediately after reset.

5.4 MC-4760 Pin Identification

This section describes the pins of the MC-4760. Figure 5.3 shows the MC-4760 pin configuration.

Figure 5.3 MC-4760 Pin Configuration



Pin Description

No.	Symbol	Name	Function	Description
1	MIC IN	Microphone	Input	Microphone input. Interfaces the microphone signal to an internal preamplifier. Max input level is ±6mV p-p based on a sine wave input with the equalization amplifier at 20dB gain and an attenuation control value of 7FH. Input impedance is 1 kohm.
2	DVO	Digitized Speech Output	Output 3-state	Serial output for 8-bit digitized speech samples. Output from the internal A/D converter.
3	CLK	Clock	Input	Input for the operation clock for the internal A/D converter. 2 MHz frequency.
4	SMPL	Sampling Clock	Input	Input for the sampling clock for the A/D converter. Allows serial speech sample data to be shifted out on DVO. Clock frequency is 10 KHz. It is a non-inverted version of the uPD7761 SMPL0 and SMPL1 clock.
5, 8,9	N.C.	No Connection	Open	No connection, leave open
6	GNDA	Analog Ground	Ground	Analog ground return. No internal connection to GNDD.
7	V-	-12V Power Supply	Power	-12V ± 5% referenced to GNDA

No.	Symbol	Name	Function	Description
10	A OUT	Attenuator Output	Output	Analog output for the input speech data after it goes through the pre-amp, equalization amplifier and attenuator, but not the low pass filter. You may use it to record the input speech data. Minimum load impedance of 10 kohm is required.
11-16	ATC_5 - ATC_0	Attenuator Control	Input	TTL-level input terminals for digital control of the attenuator.
17,18	GC_1,GC_2	Ground	Input	Connect to digital ground (GNDD).
19	V+	+12V Power Supply	Power	+12V±5% referenced to GNDA
20	GNDD	Digital Ground	Ground	Digital ground return for V_{CC} supply. Not connected to GNDA internally.
21	V_{CC}	+5V Power Supply	Power	+5V ± 5% referenced to GNDD.
22	G ADJ	Gain Adjust	Input	Connect external gain setting resistance for the equalization amplifier. A minimum resistance of 75 ohm is required.
23	LPF OUT	Lowpass Filter Output	Output	Use to observe the analog speech signal before conversion. Do not connect a load to this terminal.

No.	Symbol	Name	Function	Description
24	LINE IN	Line Input	Input	Tape input. Input impedance is 10 kohm. Max input level is ±0.6V p-p based on a sine wave input with the equalization amplifier at 20dB gain and an attenuation control value of 7FH.

CHAPTER 6 USING THE uPD7761D ANALYSIS AND MATCHING PROCESSOR

The uPD7761 is a dedicated high-speed arithmetic processor for analysis and matching calculations. It analyzes the input speech signal by extracting the spectral power content, and performs pattern matching calculations via the dynamic programming algorithm. A control word passed from the uPD7762 specifies the choice of analysis or pattern matching.

The uPD7761 internal architecture is designed for real-time, speech-band analysis. The component operates internally as a 16-bit device. It communicates with the MC-4760 via a dedicated serial port.

The uPD7761 accepts digitized speech data samples from the MC-4760 analog interface. It communicates with the uPD7762 via an 8-bit parallel data port. It is treated as a dedicated peripheral of the uPD7762 control processor.

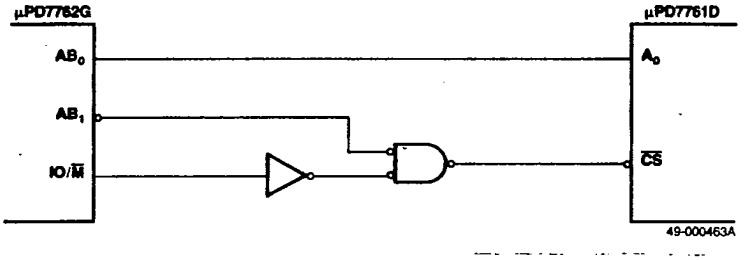
6.1 uPD7761 Operation

The uPD7762 control processor directly controls the operation of the uPD7761 analysis and matching processor. At the beginning of operation, the $\overline{\text{RESET}}$ output terminal of the uPD7762 sends an active high level reset signal to the RST input terminal of the uPD7761. The reset level must last for at least four clock-cycle times of the uPD7761 (500ns total at 8MHz clock).

The uPD7761 is then initialized and enters an internal Wait state at the end of the RST input. The uPD7761 stays in the Wait state until the uPD7762 control processor inputs a mode control word through the parallel data port. The mode control word is written into the uPD7761 as two bytes. Once a mode control word is received, the uPD7761 executes the analysis process or the pattern matching operation, depending on the mode control word. At the end of processing, a code is output to indicate which operation was performed, followed by output of data.

Connect the I/O addresses of the uPD7761 and uPD7762 as shown in Figure 6.1.

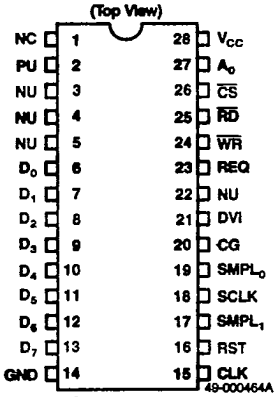
Figure 6.1 I/O Addresses for uPD7761 to uPD7762



6.2 uPD7761D Pin Identification

This section describes the pins of the uPD7761D. Figure 6.2 shows the uPD7761D pin configuration.

Figure 6.2 uPD7761D Pin Configuration



Pin Description

No.	Symbol	Name	Function	Description
1	N.C.	No Connection	Open	No connection, leave open.
2,20	C.G.	Contact Ground	Input	Connect to ground (GND) for proper device operation.
3,4, 5,22	N.U.	Not Used	Open	Leave open.
6-13	D_0-D_7	Data bus	Input/ Output 3-state	8-bit bidirectional data bus for transfer of data, status and mode codes with the uPD7762.
14	GND	Ground	Ground	0V Ground
15	CLK	Clock	Input	Input for single phase operation clock. Maximum clock frequency is 8MHz.
16	RST	Reset	Input	Resets the uPD7761 when a high-level signal is input for 4 clock cycles (500ns total) or greater.
17,19	SMPL1, SMPL0	Sampling Clock	Input	Input for sampling clock. Allows serial speech samples to be shifted into the uPD7761 from the MC-4760 A/D converter. Active low. Clock frequency 10KHz with a 1:24 duty cycle.
18	SCLK	Serial Clock	Input	Serial shift clock frequency of 2MHz. Digitized speech samples are shifted into the DVI input on the rising edge of SCLK.

No.	Symbol	Name	Function	Description
21	DVI	Digitized Speech Input	Input	Input for 8-bit speech data samples from the MC-4760 A/D converter. Connect this terminal to the MC-4760 DVO output.
23	REQ	Request for Data Transfer	Output	Output to the uPD7762 to request a data transfer from the uPD7761. Connect it to the uPD7762 REQ input terminal.
24	$\overline{WR}$	Write	Input	Allows the contents of the data bus to be written to the internal data register.
25	$\overline{RD}$	Read	Input	Allows the internal data or status register to be read onto the external data bus.
26	$\overline{CS}$	Chip Select	Input	Active low enables data transfer through the data port (D_0-D_7).
27	A_0	Address Select	Input	Selects R/W access of the data register or read access of the status register. A_0=0 selects DR (read/write), A_0=1 selects SR (read only).
28	V_{CC}	+5V Supply	Power	+5V ± 5% referenced to GND.

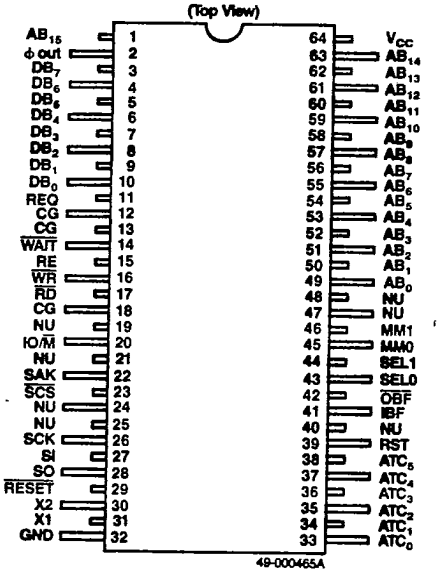
CHAPTER 7 USING THE UPD7762G CONTROL PROCESSOR

The uPD7762 is the system-level control processor for the speech recognition chip set. It controls the chip set, executes commands, and interfaces with the host system. Functions related to the recognition process include speech detection, input level control, speech pattern compression, memory management, recognition result judgment, and status and error reporting. The uPD7762 control processor provides a variety of options allowing you to tailor it to suit many diverse applications.

7.1 uPD7762 Pin Identification

This section describes the pins of the uPD7762. Figure 7.1 shows the uPD7762 pin configuration.

Figure 7.1 uPD7762 Pin Configuration



Pin Descriptions

No.	Symbol	Name	Function	Description
1 49-63	AB_{15} AB_0-AB_{14}	Address Bus	Output 3-state	16-Bit address bus for addressing external memory and I/O devices. AB_0 is the least significant bit.
2	ø out		Output	Prescaled output clock at one half the frequency input at X1.
3-10	DB_0-DB_7	Data Bus	Input/ Output 3-state	8-bit bidirectional data bus that transfers data between the processor and external memory and I/O devices. DB_0 is the least significant bit.
11	REQ	Request Data Transfer	Input	Edge-sensitive data transfer request for the uPD7761. Connect to the corresponding uPD7761 REQ output pin (23).
12,13	C.G.	Contact Ground	Input	Connect to ground (GND).
14	$\overline{WAIT}$	Wait Request	Input	Extends the read/write cycle timing when using slow external memory. The uPD7762 checks the wait request at the end of the T_2 cycle. If wait request is active (low), a wait state (T_W) is inserted in the read/write cycle. The device stays in the wait state until $\overline{WAIT}$ goes high.
15	RE	Refresh Enable	Output	Internal uPD7762 memory cannot be accessed while RE is active high.

No.	Symbol	Name	Function	Description
16	$\overline{WR}$	Write	Output 3-state	Allows data to be written to external memory or I/O devices.
17	$\overline{RD}$	Read	Output 3-state	Allows data to be read from external memory or I/O devices.
18,19 24,25 40,47 48	N.U.	Not Used	Open	
20	IO/$\overline{M}$	I/O Memory	Output	Indicates if external read ($\overline{RD}$) and write ($\overline{WR}$) operations are for memory or I/O devices. Outputs low level during memory access, and high level during I/O access.
21	TO		Output	Internal use only.
22	SAK	Serial Acknowledge	Output	Goes low after 8 clock cycles of $\overline{SCK}$, signaling the end of a byte transfer into or out of the uPD7762 serial port. The signal goes high when the uPD7762 reads the serial register internally on an input operation, or loads the serial register during an output operation.
23	SCS	Serial Chip Select	Input	A low level enables the serial clock and allows serial data transfer through the SO and SI ports. A high level inhibits $\overline{SCK}$ and goes to the high impedance state.

No.	Symbol	Name	Function	Description
26	$\overline{SCK}$	Serial Clock	Input	Externally supplied serial shift clock. Max. frequency of 1MHZ. The data bit on the SI input is loaded into the serial register at the rising edge. The serial register contents are clocked out to the SO output from MSB to LSB at the falling edge.
27	SI	Serial Input	Input	Shifts serial data into the serial register (MSB first) through the SI port. Data is clocked on the rising edge of $\overline{SCK}$.
28	SO	Serial Output	Output 3-state	Shifts serial data from the serial register (MSB first) through the SO port. Data is clocked on the falling edge of $\overline{SCK}$.
29	$\overline{RESET}$	Reset	Input	The uPD7762 is reset when a low level signal is input for at least 4us. During reset, the address bus, data bus, and $\overline{RD}$ and $\overline{WR}$ signals go to the high impedance state.
30,31	X_2, X_1	Crystal	Input	Connect an external crystal to the internal clock generation circuitry. When you use an externally generated clock, input it through the X1 pin.
32	GND	Ground	Ground	0V ground.

No.	Symbol	Name	Function	Description
33-38	ATC_0 - ATC_5	Attenuator Control	Output	Latched output port that controls the MC-4760 digitally controlled attenuator.
39	RST	Reset	Output	Output terminal used to reset the uPD7761 and the clock generation logic that produces the SMPL, SMPL0, and SMPL1 sampling clocks.
41	IBF	Input Buffer Full	Input	Use with the 8255 interface option. Goes high when the uPD7762 outputs data to the 8255. The 8255 generates IBF in response to STB from the uPD7762.
42	$\overline{OBF}$	Output Buffer Full	Input	Use with the 8255 interface option. The 8255 sets it low to tell the uPD7762 that the host wrote a byte of data to the 8255. In mode 2, the uPD7762 generates an ACK to the 8255 to acquire the data byte.
43,44	SEL0, SEL1	Interface Select	Input	Selects the interface for host communication.

SEL0	SEL1	Interface
0	0	8255 parallel
0	1	uPD7762 serial
1	1	8251 RS-232C

No.	Symbol	Name	Function	Description
45,46	MM0,MM1	Memory Mode	Input	Specifies the size of the available pattern memory.

MM0	MM1	Memory area
0	0	64K Bytes
0	1	16K
1	0	32K
1	1	48K

64	V_{CC}	+5V Supply	Power	+5V± 10% referenced to GND.

APPENDIX A APPLICATION CIRCUIT EXAMPLES

This appendix shows two circuit examples you can use with the Speech Recognition LSI set.

Figure A.1 Speech Recognition LSI Set Circuit Example

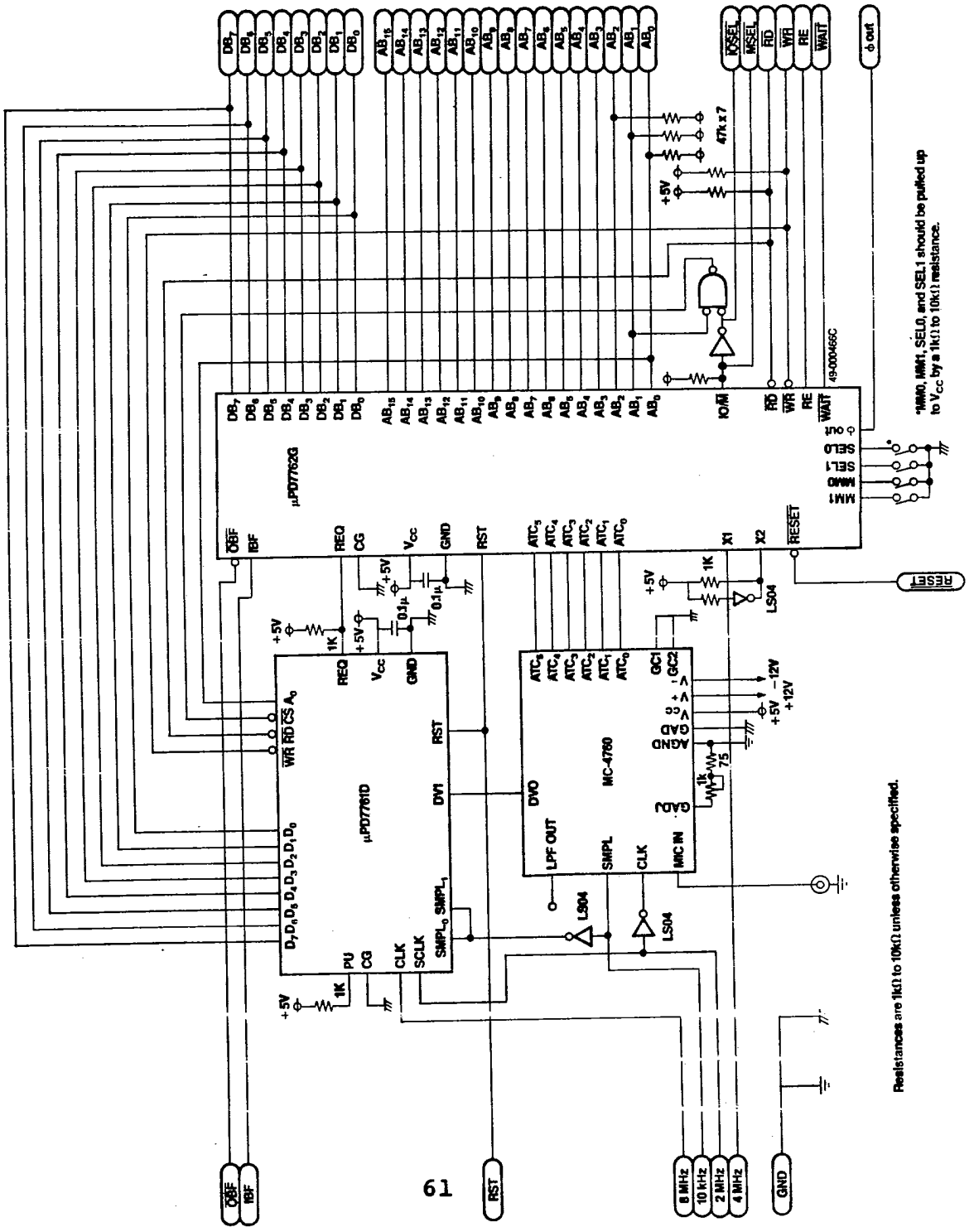


Figure A.2 Parallel Interface Circuit