

# STSJ100NH3LL

## N-CHANNEL 30V - 0.0027 Ω - 100A PowerSO-8™ STripFET™ III POWER MOSFET FOR DC-DC CONVERSION

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	ID
STSJ100NH3LL	30 V	<0.0035 Ω	100 A

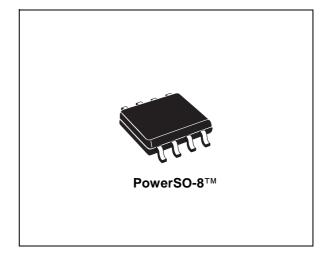
- TYPICAL R<sub>DS</sub>(on) = 0.0027 Ω @ 10V
- OPTIMAL R<sub>DS</sub>(on) x Qg TRADE-OFF @ 4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

#### DESCRIPTION

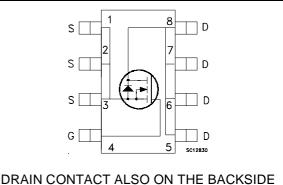
The STSJ100NH3LL utilizes the latest advanced design rules of ST's proprietary STripFET<sup>TM</sup> technology. This process compled to unique metallization techniques realizes the most advanced low voltage MOSFET in SO-8 ever produced. The exposed slug reduces the R<sub>thj-c</sub> improving the current capability.

#### **APPLICATIONS**

 SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PC<sub>S</sub>



#### INTERNAL SCHEMATIC DIAGRAM



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS}$ = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	± 18	V
ID	Drain Current (continuous) at T <sub>C</sub> = 25°C	100	A
ID	Drain Current (continuous) at $T_C = 25^{\circ}C$ (#)	22	A
ID	Drain Current (continuous) at T <sub>C</sub> = 100°C	62.5	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	400	A
P <sub>tot</sub>	Total Dissipation at $T_C = 25^{\circ}C$ Total Dissipation at $T_C = 25^{\circ}C$ (#)	70 3	W W

(•) Pulse width limited by safe operating area.

November 2002

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

## STSJ100NH3LL

#### THERMAL DATA

(#) When Mounted on FR-4 board with 1 inch<sup>2</sup> pad, 2 oz of Cu and t  $\leq$  10 sec.

## **ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25 °C unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
IDSS	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating $V_{DS}$ = Max Rating T <sub>C</sub> = 125°C			1 10	μΑ μΑ
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 18 V			±100	nA

#### ON (\*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 50 A I <sub>D</sub> = 50 A		0.0027 0.0035	0.0035 0.005	$\Omega \ \Omega$

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> =10 V I <sub>D</sub> = 12 A		30		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		4450 655 50		pF pF pF

#### ELECTRICAL CHARACTERISTICS (continued)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time			18 50		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}$ =15V I <sub>D</sub> =100A V <sub>GS</sub> =4.5V (see test circuit, Figure 2)		32 12.5 10	43	nC nC nC

#### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time			75 8		ns ns

#### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (●)	Source-drain Current Source-drain Current (pulsed)				100 400	A A
V <sub>SD</sub> (*)	Forward On Voltage	I <sub>SD</sub> = 100 A V <sub>GS</sub> = 0			1.2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$      I_{SD} = 100 \text{ A} \qquad di/dt = 100 \text{ A}/\mu\text{s} \\       V_{DD} = 25 \text{ V} \qquad T_j = 150^\circ\text{C} \\       (see test circuit, Figure 3) $		32 34 2.1		ns nC A

(\*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

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## STSJ100NH3LL

**Fig. 1:** Switching Times Test Circuits For Resistive Load

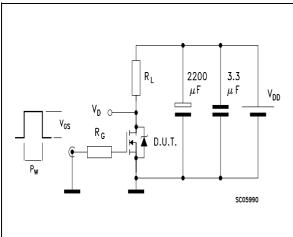
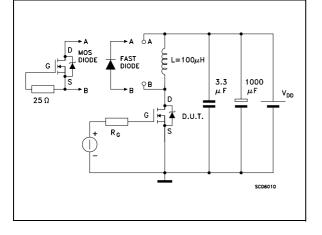
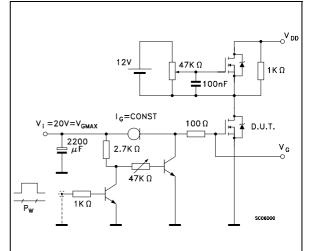


Fig. 3: Test Circuit For Diode Recovery Behaviour



#### Fig. 2: Gate Charge test Circuit

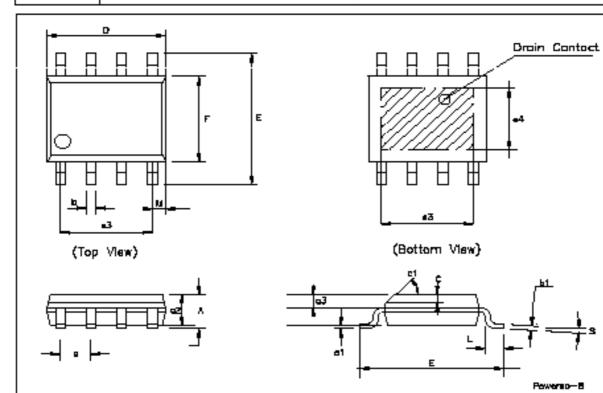


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DIM.		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45°	(typ.)		
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S		•	8° (r	nax.)	•	

## PowerSO-8™ MECHANICAL DATA



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