DATA SHEET

74AHC273; 74AHCT273
Octal D-type flip-flop with reset; positive-edge trigger

Product specification
Supersedes data of 1999 Sep 01

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Philips
Semiconductors

PHILIPS

Octal D-type flip-flop with reset; positive-edge trigger

74AHC273; 74AHCT273

FEATURES

- Ideal buffer for MOS microcontroller or memory
- Common clock and master reset
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accepts voltages higher than V_{CC}
- Related products:
  - See 74AHC(T)377 for clock enable version
  - See 74AHC(T)373 for transparent latch version
  - See 74AHC(T)374 for 3-state version.
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC/AHCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC/AHCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74AHC273	74AHCT273	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	CP to Qn		4.2	4.0	ns
	$\overline{MR}$ to Qn		3.7	3.9	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	165	120	MHz
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	14.0	18.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT			OUTPUT
	$\overline{MR}$	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;
   X = don't care;
   ↑ = LOW-to-HIGH transition.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74AHC273D	–40 to +125 °C	20	SO20	plastic	SOT163-1
74AHCT273D	–40 to +125 °C	20	SO20	plastic	SOT163-1
74AHC273PW	–40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74AHCT273PW	–40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74AHC273BQ	–40 to +125 °C	20	DHVQFN20	plastic	SOT764-1
74AHCT273BQ	–40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{MR}$	master reset input (active LOW)
2	Q0	flip-flop output
3	D0	data input
4	D1	data input
5	Q1	flip-flop output
6	Q2	flip-flop output
7	D2	data input
8	D3	data input
9	Q3	flip-flop output
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH; edge-triggered)
12	Q4	flip-flop output
13	D4	data input
14	D5	data input
15	Q5	flip-flop output
16	Q6	flip-flop output
17	D6	data input
18	D7	data input
19	Q7	flip-flop output
20	V_{CC}	supply voltage

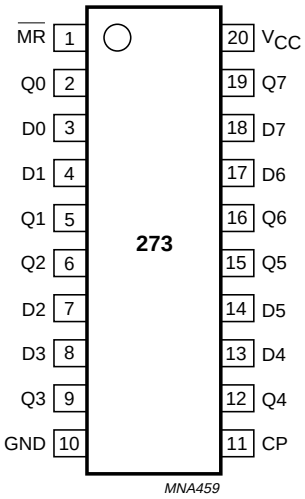
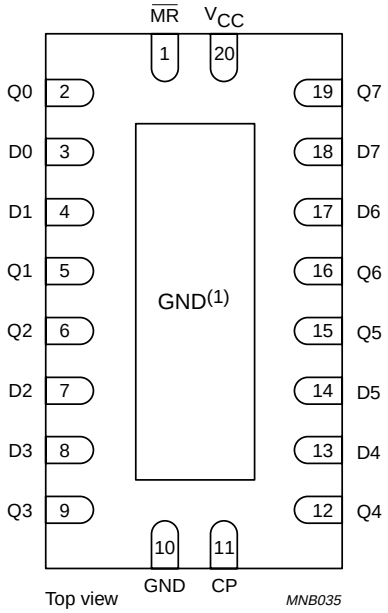


Fig.1 Pin configuration SO20 and TSSOP20.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

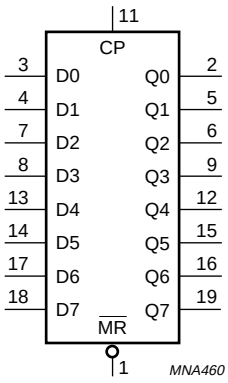


Fig.3 Logic symbol.

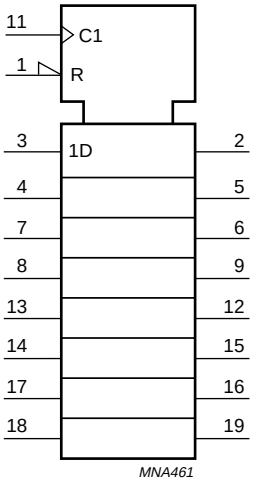


Fig.4 IEC logic symbol.

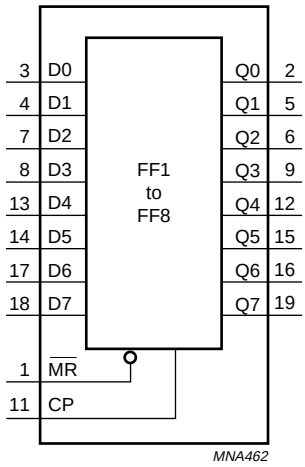


Fig.5 Function diagram.

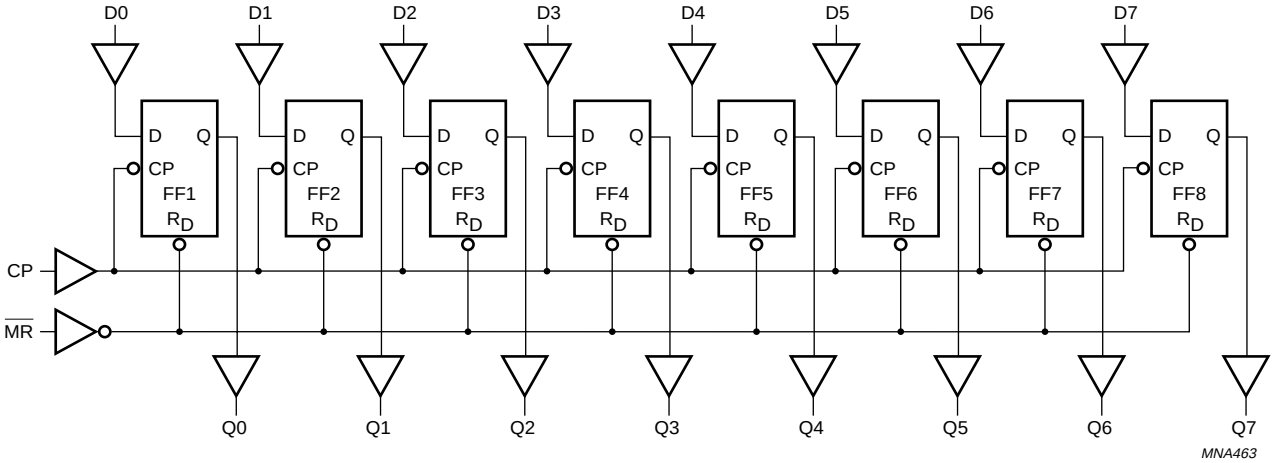


Fig.6 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall ratio	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	V_O = –0.5 V to V_{CC} + 0.5 V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO20 packages: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP20 packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.
   For DHVQFN20 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

Type 74AHC273

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	2.0	–	V
			3.0	2.9	3.0	–	V
			4.5	4.4	4.5	–	V
		I_O = –4.0 mA	3.0	2.58	–	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	2.0	–	0	0.1	V
			3.0	–	0	0.1	V
			4.5	–	0	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.36	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	4.0	μA
C_I	input capacitance		–	–	3	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	–	–	V
			3.0	2.9	–	–	V
			4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.48	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					V
		I_O = 50 μA	2.0	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.44	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	2.0	1.9	–	–	V
			3.0	2.9	–	–	V
			4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.40	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	2.0	–	–	0.1	V
			3.0	–	–	0.1	V
			4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.55	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	2.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	80	μA
C_I	input capacitance		–	–	–	10	pF

Type 74AHCT273

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	4.5	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	0	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	4.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.35	mA
C_I	input capacitance		–	–	3	10	pF
T_{amb} = –40 to +85 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	2.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; I_O = 0	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

AC CHARACTERISTICS

Type 74AHC273

Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)	V_{CC} (V)				
T_{amb} = 25 °C; note 1								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	3.0 to 3.6	–	6.0	13.6	ns
				4.5 to 5.5	–	4.2	9	ns
			50	3.0 to 3.6	–	8.6	17.1	ns
				4.5 to 5.5	–	6.0	11.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	3.0 to 3.6	–	5.1	13.6	ns
				4.5 to 5.5	–	3.7	8.5	ns
			50	3.0 to 3.6	–	7.3	17.1	ns
				4.5 to 5.5	–	5.3	10.5	ns
f_{max}	maximum clock pulse frequency		15	3.0 to 3.6	75	120	–	MHz
				4.5 to 5.5	120	165	–	MHz
			50	3.0 to 3.6	50	75	–	MHz
				4.5 to 5.5	80	110	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	3.0 to 3.6	5.0	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	3.0 to 3.6	5.0	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	3.0 to 3.6	2.5	–	–	ns
				4.5 to 5.5	2.0	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	3.0	–	–	ns
				4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	1.0	–	–	ns
				4.5 to 5.5	1.0	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)	V_{CC} (V)				
T_{amb} = −40 to +85 °C								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	3.0 to 3.6	1.0	–	16.0	ns
				4.5 to 5.5	1.0	–	10.5	ns
			50	3.0 to 3.6	1.0	–	19.5	ns
				4.5 to 5.5	1.0	–	12.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	3.0 to 3.6	1.0	–	16.0	ns
				4.5 to 5.5	1.0	–	10.0	ns
			50	3.0 to 3.6	1.0	–	19.5	ns
				4.5 to 5.5	1.0	–	12.0	ns
f_{max}	maximum clock pulse frequency		15	3.0 to 3.6	65	–	–	MHz
				4.5 to 5.5	100	–	–	MHz
			50	3.0 to 3.6	45	–	–	MHz
				4.5 to 5.5	70	–	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	3.0 to 3.6	6.5	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	3.0 to 3.6	6.0	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	3.0 to 3.6	2.5	–	–	ns
				4.5 to 5.5	2.0	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	3.0	–	–	ns
				4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	1.0	–	–	ns
				4.5 to 5.5	1.0	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)	V_{CC} (V)				
T_{amb} = −40 to +125 °C								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	3.0 to 3.6	1.0	–	17.0	ns
				4.5 to 5.5	1.0	–	11.5	ns
			50	3.0 to 3.6	1.0	–	21.5	ns
				4.5 to 5.5	1.0	–	14.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	3.0 to 3.6	1.0	–	17.0	ns
				4.5 to 5.5	1.0	–	11.0	ns
			50	3.0 to 3.6	1.0	–	21.5	ns
				4.5 to 5.5	1.0	–	13.5	ns
f_{max}	maximum clock pulse frequency		15	3.0 to 3.6	65	–	–	MHz
				4.5 to 5.5	100	–	–	MHz
			50	3.0 to 3.6	45	–	–	MHz
				4.5 to 5.5	70	–	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	3.0 to 3.6	6.5	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	3.0 to 3.6	6.0	–	–	ns
				4.5 to 5.5	5.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	3.0 to 3.6	2.5	–	–	ns
				4.5 to 5.5	2.0	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	3.0	–	–	ns
				4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	3.0 to 3.6	1.0	–	–	ns
				4.5 to 5.5	1.0	–	–	ns

Note

1. Typical values are measured at V_{CC} = 3.3 V for V_{CC} = 3.0 to 3.6 V and at V_{CC} = 5.0 V for V_{CC} = 4.5 to 5.5 V.

Type 74AHCT273

Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

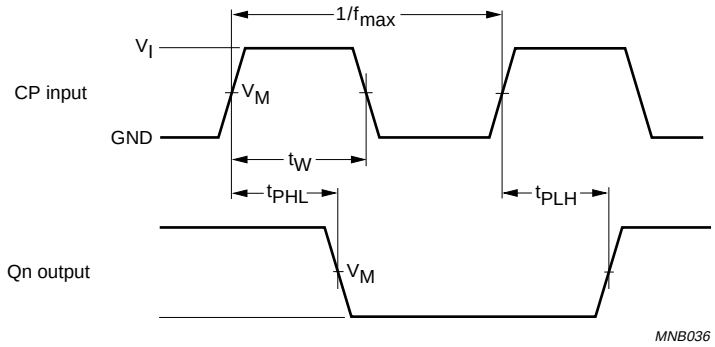
SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)	V_{CC} (V)				
T_{amb} = 25 °C; note 1								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	4.5 to 5.5	–	4.0	7.5	ns
			50	4.5 to 5.5	–	5.8	9.2	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	4.5 to 5.5	–	3.9	10.0	ns
			50	4.5 to 5.5	–	5.6	11.0	ns
f_{max}	maximum clock pulse frequency		15	4.5 to 5.5	75	120	–	MHz
			50	4.5 to 5.5	50	75	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	4.5 to 5.5	5.0	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	4.5 to 5.5	5.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	4.5 to 5.5	2.5	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	1.0	–	–	ns
T_{amb} = −40 to +85 °C								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	4.5 to 5.5	1.0	–	8.8	ns
			50	4.5 to 5.5	1.0	–	10.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	4.5 to 5.5	1.0	–	11.6	ns
			50	4.5 to 5.5	1.0	–	12.6	ns
f_{max}	maximum clock pulse frequency		15	4.5 to 5.5	65	–	–	MHz
			50	4.5 to 5.5	45	–	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	4.5 to 5.5	6.5	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	4.5 to 5.5	6.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	4.5 to 5.5	2.5	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	1.0	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L (pF)	V_{CC} (V)				
T_{amb} = −40 to +125 °C								
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	4.5 to 5.5	1.0	–	9.5	ns
			50	4.5 to 5.5	1.0	–	11.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 8 and 10	15	4.5 to 5.5	1.0	–	12.5	ns
			50	4.5 to 5.5	1.0	–	14.0	ns
f_{max}	maximum clock pulse frequency		15	4.5 to 5.5	65	–	–	MHz
			50	4.5 to 5.5	45	–	–	MHz
t_W	clock pulse width HIGH or LOW	see Figs 7 and 10	50	4.5 to 5.5	6.5	–	–	ns
	master reset pulse width LOW	see Figs 8 and 10	50	4.5 to 5.5	6.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Figs 8 and 10	50	4.5 to 5.5	2.5	–	–	ns
t_{su}	set-up time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	3.0	–	–	ns
t_h	hold time Dn to CP	see Figs 9 and 10	50	4.5 to 5.5	1.0	–	–	ns
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 7 and 10	15	4.5 to 5.5	1.0	–	9.5	ns

Note

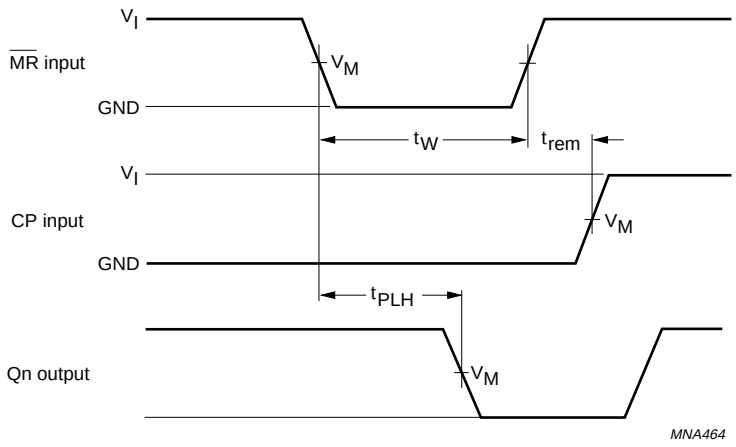
1. All typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS



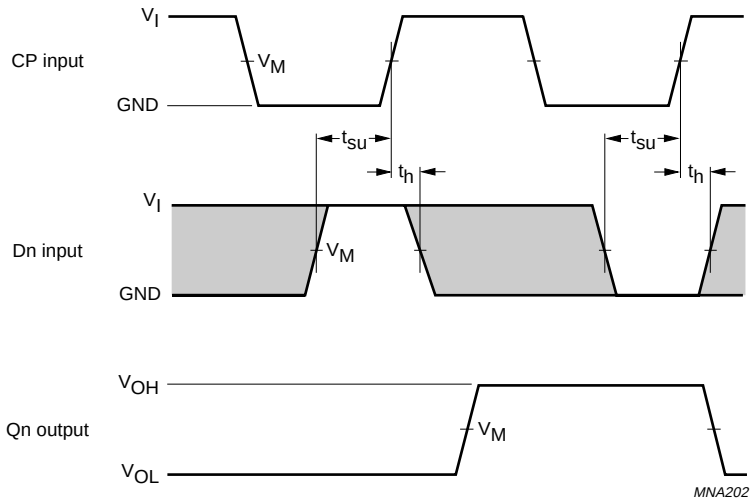
FAMILY	V_I	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
AHCT	GND to 3.0 V	1.5 V	$0.5V_{CC}$

Fig.7 The clock (CP) to output (Qn) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.



FAMILY	V_I	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
AHCT	GND to 3.0 V	1.5 V	$0.5V_{CC}$

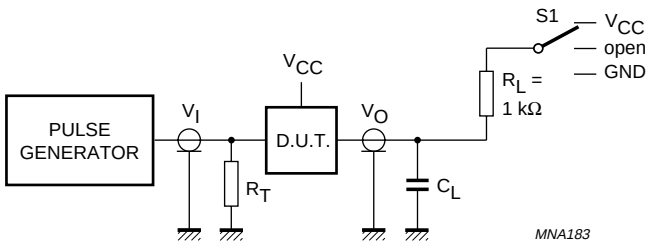
Fig.8 The master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays and master reset to clock (CP) removal time.



FAMILY	V_I	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
AHCT	GND to 3.0 V	1.5 V	$0.5V_{CC}$

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig.9 The data set-up and hold times for the data input (Dn).



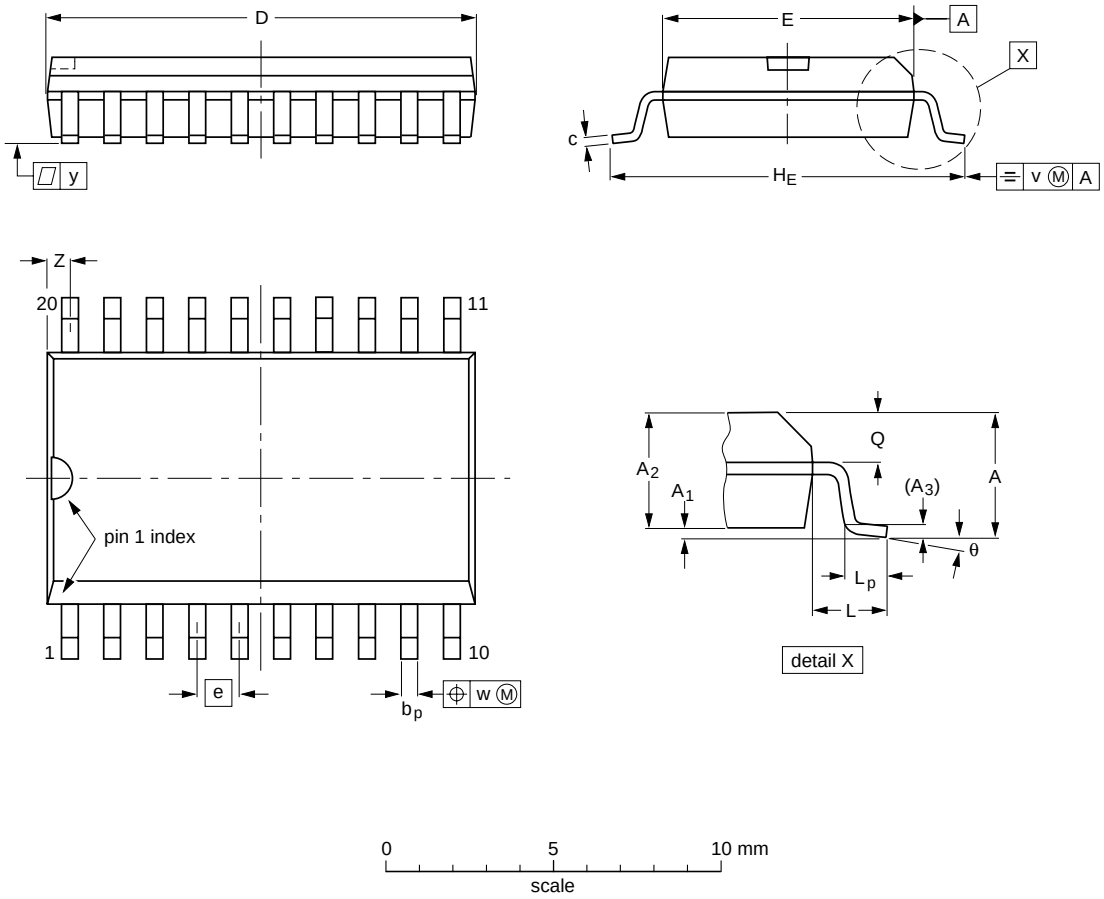
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit.
C_L = Load capacitance including jig and probe capacitance (See Chapter “AC characteristics”).
R_L = Load resistor.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

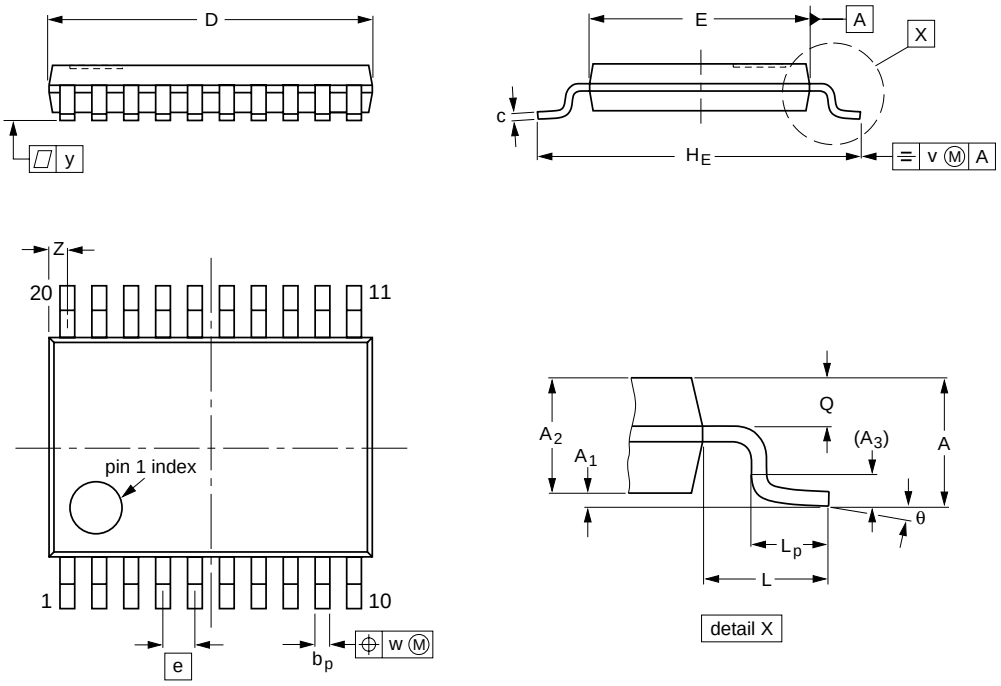
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

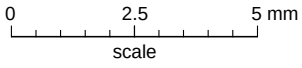
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

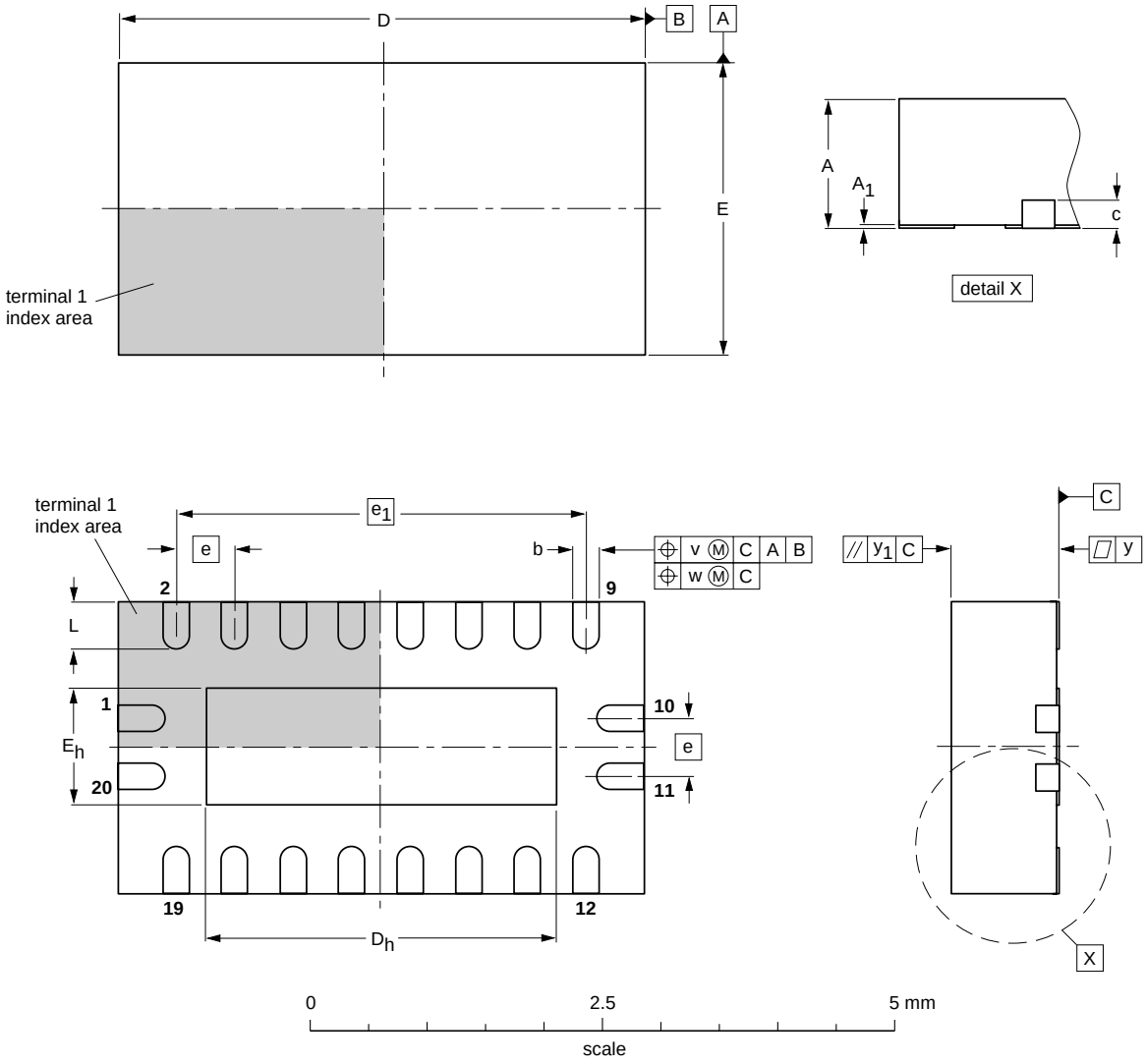
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

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