REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Change case 2 to case X. Changes to recommended operating conditions, table I, and table II. Convert to military drawing format. Editorial changes throughout. Add vendor CAGE 34649.	87 FEB 26	Weckman
C	Add device type 02. Change drawing CAGE code. Editorial changes throughout.	89 OCT 25	Weckman
D	CLK rise time (t_{CH1CH2}) device type 01 and 02 changed from 15 ns maximum to 10 ns maximum. CLK fall time (t_{CL2CL1}) device type 01 and 02 changed from 15 ns maximum to 10 ns maximum. Table I: RD inactive to next address active (t_{RHAV}) device type 02 changed from -45 ns minimum to -40 ns minimum. Editorial changes throughout.	90 MAY 31	Weckman

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	D	C	C	C	C	C	D																	
SHEET	22	23	24	25	26	27	28																	

REV STATUS OF SHEETS	REV	D	C	D	C	C	C	D	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

PREPARED BY: Christopher A. Rauch

CHECKED BY: Charles Reusing

APPROVED BY: William K. Heckman

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, DIGITAL, CMOS, 16 BIT MICROPROCESSOR, MONOLITHIC SILICON

DRAWING APPROVAL DATE: 29 NOVEMBER 1984

REVISION LEVEL: D

SIZE	CAGE CODE	
A	14933	84052

SHEET 1

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1688

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84052	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	80C86	5 MHz	16 bit microprocessor
02	80C86-2	8 MHz	16 bit microprocessor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground)	+8.0 V dc maximum
Input, output or I/O voltage applied	GND -0.5 V dc to V_{CC} +0.5 V dc
Storage temperature	-65°C to +150°C
Maximum power dissipation, (P_D)	1 W
Lead temperature (soldering, 5 seconds)	260°C
Junction temperature (T_J)	150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q and X	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}):	
Device type 01	+4.5 V dc minimum to +5.5 V dc maximum
Device type 02	+4.75 V dc minimum to +5.25 V dc maximum
Frequency of operation:	
Device type 01	5.0 MHz
Device type 02	8.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Address float delay (t_{CLAZ}):	
Device type 01	t_{CLAX} minimum to 80 ns maximum 1/ 2/
Device type 02	t_{CLAX} minimum to 50 ns maximum 1/ 2/
Data hold time (t_{CLDX2})	10 ns minimum 1/ 2/
Status float delay (t_{CHSZ})	80 ns 1/ 2/
MCE inactive delay (t_{CLMCL})	15 ns 1/

1/ These device design parameters were characterized using C_L = 100 pF, clock rise/fall time are driven at 1 ns/V, and input rise/fall time are driven at 1 ns/V.
2/ Minimum and maximum mode.

Data hold time after WR (t_{WHDX})	t_{CLCH} -30 ns minimum 1/ 3/
System design characteristics:	
RDY setup time into clock generator (t_{R1VCL})	35 ns minimum 4/
RDY hold time into clock generator (t_{CLR1X})	0 ns minimum 4/
Command active delay (t_{CLML}):	
Device type 01	5 ns to 45 ns maximum 5/
Device type 02	5 ns to 35 ns maximum 5/
Command inactive delay (t_{CLMH}):	
Device type 01	5 ns to 45 ns maximum 5/
Device type 02	5 ns to 35 ns maximum 5/
Status valid to ALE high (t_{SVLH}):	
Device type 01	35 ns maximum 5/
Device type 02	20 ns maximum 5/
Status valid to MCE high (t_{SVMCH}):	
Device type 01	35 ns maximum 5/
Device type 02	30 ns maximum 5/
CLK low to MCE high (t_{CLMCH}):	
Device type 01	35 ns maximum 5/
Device type 02	25 ns maximum 5/
Control active delay (t_{CVNV})	5 ns minimum to 45 ns maximum 5/
Control inactive delay (t_{CVNX})	5 ns minimum to 45 ns maximum 5/
Direction control active delay (t_{CHDTL})	50 ns maximum 5/
Direction control inactive delay (t_{CHDTH}):	
Device type 01	35 ns maximum 5/
Device type 02	30 ns maximum 5/
CLK low to ALE valid (t_{CLLH})	20 ns maximum 5/
ALE inactive delay (t_{CHLL}):	
Device type 01	4 ns minimum to 35 ns maximum 5/
Device type 02	4 ns minimum to 25 ns maximum 5/
CLK rise time (t_{CH1CH2}):	
Device type 01	10 ns maximum
Device type 02	10 ns maximum
CLK fall time (t_{CL2CL1}):	
Device type 01	10 ns maximum
Device type 02	10 ns maximum
Input rise time (except CLK) (t_{ILIH})	15 ns maximum
Input fall time (except CLK) (t_{IHIL})	15 ns maximum

1/ These device design parameters were characterized using C_L = 100 pF, clock rise/fall time are driven at 1 ns/V, and input rise/fall time are driven at 1 ns/V.
2/ Minimum and maximum mode.
3/ Minimum complexity system timing responses.
4/ Setup requirement for asynchronous signal only to guarantee recognition at next clock.
5/ Design reference limits when the device is used in conjunction with a bus controller in maximum mode.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connnections shall be as specified on figure 1.

3.2.2 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1989—749-033

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified V_{CC} = minimum 1/	Group A subgroups	Limits		Unit
				Min	Max	
Clock input low voltage	V_{IL1}		1, 2, 3		0.8	V
Clock input high voltage	V_{IH1}	V_{CC} = maximum	1, 2, 3	V_{CC} -0.8		V
Input low voltage	V_{IL2}	2/	1, 2, 3		0.8	V
Input high voltage	V_{IH2}	V_{CC} = maximum 2/	1, 2, 3	2.2		V
High level output voltage	V_{OH}	I_{OH} = -100 µA 3/	1, 2, 3	V_{CC} -0.4		V
		I_{OH} = -2.5 mA 3/	1, 2, 3	3.0		
Low level output voltage	V_{OL}	I_{OL} = 2.5 mA 3/	1, 2, 3		0.4	V
Input leakage current	I_{IL}	V_{IN} = 0 V or V_{CC} V_{CC} = maximum	1, 2, 3	-1.0	1.0	µA
Input leakage current-bus hold high	IBHH	V_{IN} = 3.0 V, V_{CC} = minimum and maximum 4/	1, 2, 3	-40	-400	µA
Input leakage current-bus hold low	IBHL	V_{IN} = 0.8 V 3/ 5/ V_{CC} = minimum and maximum	1, 2, 3	+40	400	µA
Output leakage current	I_O	V_O = 0 V V_{CC} = maximum	1, 2, 3		-10.0	µA
Standby power supply current	ICCSB	V_{CC} = maximum, V_{IN} = V_{CC} or GND 6/ Outputs unloaded	1, 2, 3		500	µA
Operating power supply current	ICCOP	V_{CC} = 5.0 V, V_{IH} = V_{CC}, V_{IL} = GND	1, 2, 3		10	mA/MHz
Pin capacitance	C_{IN}, $C_{I/O}$, C_{OUT}	Freq = 1 MHz, T_C = 25°C All measurements referenced to device GND See 4.3.1c	4		25	pF
Functional tests		See 4.3.1d	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified V_{CC} = minimum 1/	Device types	Group A subgroups	Limits		Unit
					Min	Max	
CLK Cycle period	t_{CLCL}	Minimum and maximum mode See figure 3	01 02	9, 10, 11	200 125		ns
CLK low time	t_{CLCH}		01 02	9, 10, 11	118 68		ns
CLK high time	t_{CHCL}		01 02	9, 10, 11	69 44		ns
Data in setup time	t_{DVCL}		01 02	9, 10, 11	30 20		ns
Data in hold time	t_{CLDX1}		01 02	9, 10, 11	10 10		ns
READY setup time into device	t_{RYHCH}		01 02	9, 10, 11	118 68		ns
READY hold time into device	t_{CHRYX}		01 02	9, 10, 11	30 20		ns
READY inactive to CLK 7/	t_{RYLCL}		01 02	9, 10, 11	-5 -5		ns
INTR, NMI, TEST setup time 8/	t_{INVCH}		01 02	9, 10, 11	30 15		ns
Address valid delay	t_{CLAV}		01 02	9, 10, 11	10 10	110 60	ns
Address hold time	t_{CLAX}		01 02	9, 10, 11	10 10		ns
Data valid delay	t_{CLDV}		01 02	9, 10, 11	10 10	110 60	ns
Address float to READ active	t_{AZRL}		01 02	9, 10, 11	0 0		ns
RD active delay	t_{CLRL}		01 02	9, 10, 11	10 10	165 100	ns
RD inactive delay	t_{CLRH}		01 02	9, 10, 11	10 10	150 80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified V_{CC} = minimum 1/	Device type	Group A subgroups	Limits		Unit
					Min	Max	
RD inactive to next address active	t_{RHAV}	See figure 3	01	9, 10, 11	t_{CLCL} -45		ns
			02		t_{CLCL} -40		
Output rise time	t_{OLOH}	From 0.8 V to 2.0 V See figure 3	01 02	9, 10, 11		20 15	ns
Output fall time	t_{OHOL}	From 2.0 V to 0.8 V See figure 3	01 02	9, 10, 11		20 15	ns
Status active delay	t_{CHSV}	See figure 3	01 02	9, 10, 11	10 10	110 60	ns
HOLD setup time	t_{HVCH}	Minimum mode See figure 3	01 02	9, 10, 11	35 20		ns
ALE width	t_{LHLL}		01	9, 10, 11	t_{CLCH} -20		ns
			02		t_{CLCH} -10		
ALE active delay	t_{CLLH}		01 02	9, 10, 11		80 50	ns
ALE inactive delay	t_{CHLL}		01 02	9, 10, 11		85 55	ns
Address hold time to ALE inactive	t_{LLAX}		01	9, 10, 11	t_{CHCL} -10		ns
			02		t_{CHCL} -10		
Control active delay 1	t_{CVCTV}		01 02	9, 10, 11	10 10	110 70	ns
Control active delay 2	t_{CHCTV}		01 02	9, 10, 11	10 10	110 60	ns
Control inactive delay	t_{CVCTX}		01 02	9, 10, 11	10 10	110 70	ns
HLDA valid delay	t_{CLHAV}		01 02	9, 10, 11	10 10	160 100	ns
RD width	t_{RLRH}		01	9, 10, 11	$2t_{CLCL}$ -75		ns
			02		$2t_{CLCL}$ -50		

See footnotes at end of table.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1988—550-547

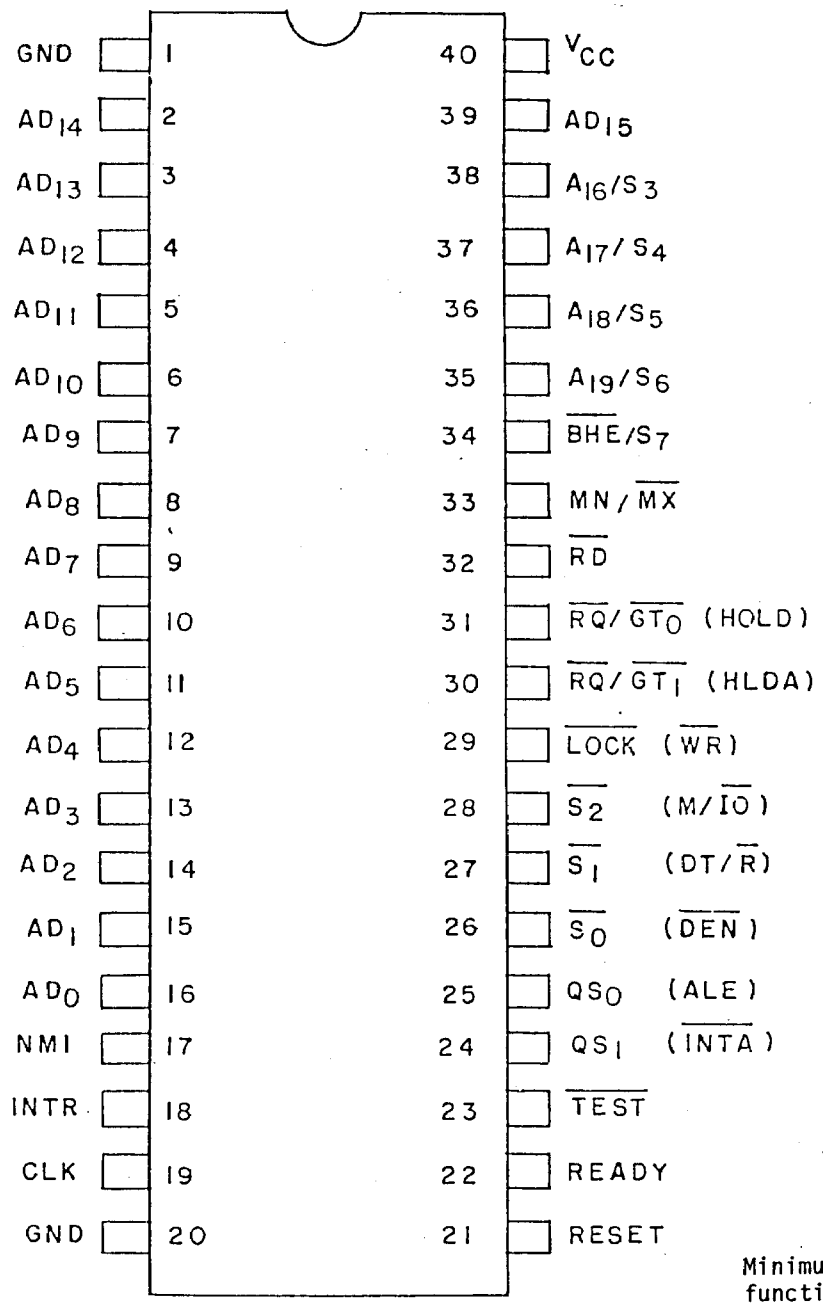
TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified V_{CC} = minimum 1/	Device type	Group A subgroups	Limits Min	Limits Max	Unit
WR width	t_{WLWH}	Minimum mode See figure 3	01	9, 10, 11	$2t_{CLCL}$ -60		ns
			02		$2t_{CLCL}$ -40		
Address valid to ALE low	t_{AVAL}		01	9, 10, 11	t_{CLCH} -60		ns
			02		t_{CLCH} -40		
$\overline{RQ}/\overline{GT}$ setup time	t_{GVCH}	Maximum mode See figure 3	01	9, 10, 11	30		ns
			02		15		
$\overline{RQ}$ hold time 9/ into device	t_{CHGX}		01	9, 10, 11	40		ns
			02		30		
Ready active to status passive 7/ 10/	t_{RYHSH}		01	9, 10, 11		110	ns
			02			65	
Status inactive delay 10/	t_{CLSH}		01	9, 10, 11	10	130	ns
			02		10	70	
GT active delay	t_{CLGL}		01	9, 10, 11	10	85	ns
			02		0	50	
GT inactive delay	t_{CLGH}		01	9, 10, 11	10	85	ns
			02		0	50	
RD width	t_{RLRH}		01	9, 10, 11	$2t_{CLCL}$ -75		ns
					$2t_{CLCL}$ -50		

1/ V_{CC} minimum is 4.5 V for device type 01 and 4.75 V for device type 02. V_{CC} maximum is 5.5 V for device type 01 and 5.25 V for device type 02.
2/ MN/MX pin is a strap option and should be held at V_{CC} or GND.
3/ Interchanging of force and sense conditions permitted.
4/ IBHH should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0 V on the following pins: 2 through 16, 26 through 32, 34 through 39.
5/ IBHL should be measured after lowering V_{IN} to GND and then raising to 0.8 V on the following pins: 2-16, 34-39.
6/ ICCSB tested during clock high time after halt instruction executed. Outputs are unloaded.
7/ Applies only to T_2 state (8 ns into T_3).
8/ Setup requirements for asynchronous signal only to guarantee recognition at next CLK.
9/ The device actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
10/ Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

Device types 01 and 02

Case Q

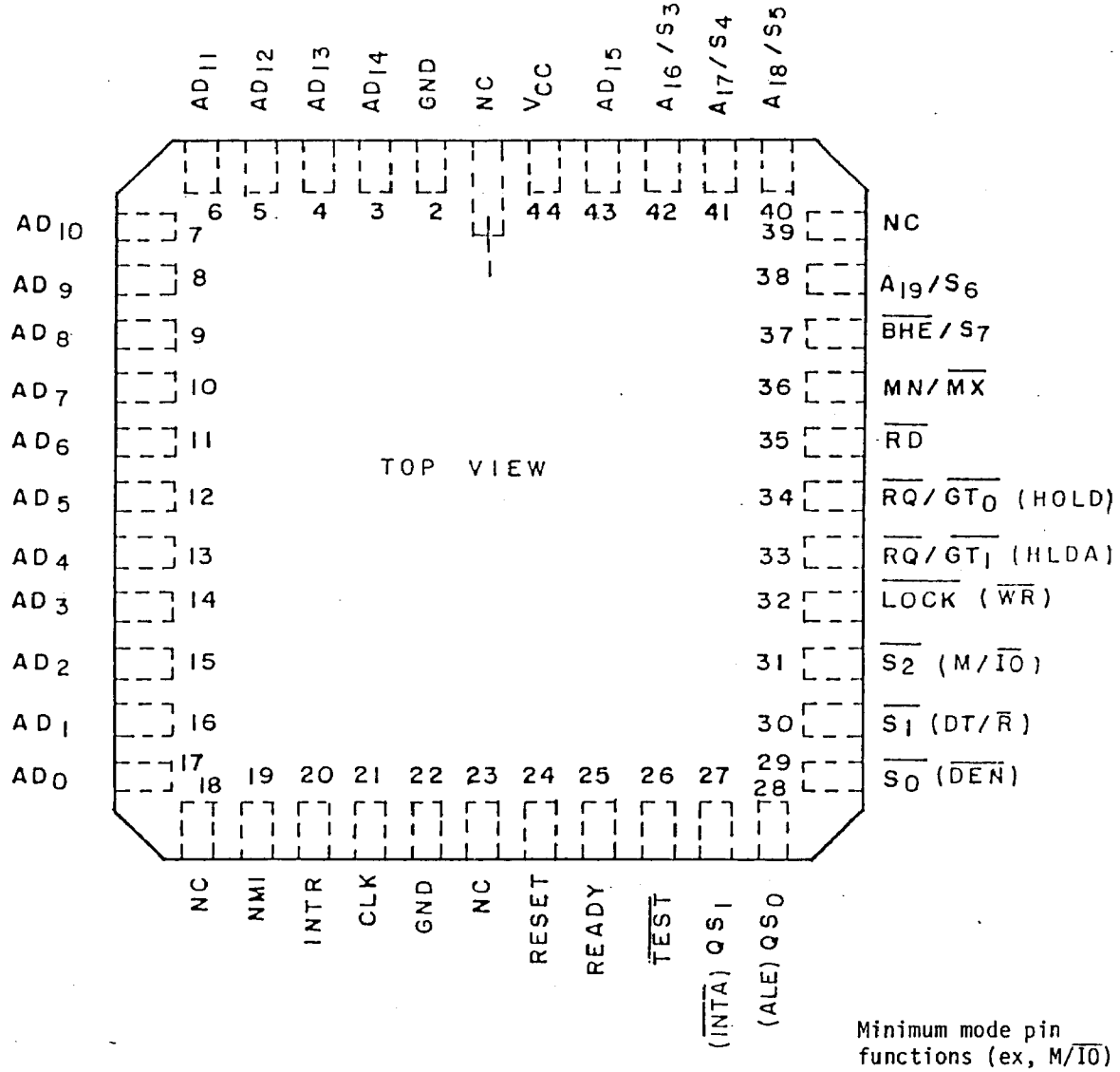


Minimum mode pin functions (ex, M/$\overline{IO}$) are shown in parantheses

FIGURE 1. Terminal connections.

Device types 01 and 02

Case X



Minimum mode pin functions (ex, M/$\overline{IO}$) are shown in parantheses

FIGURE 1. Terminal connections - Continued.

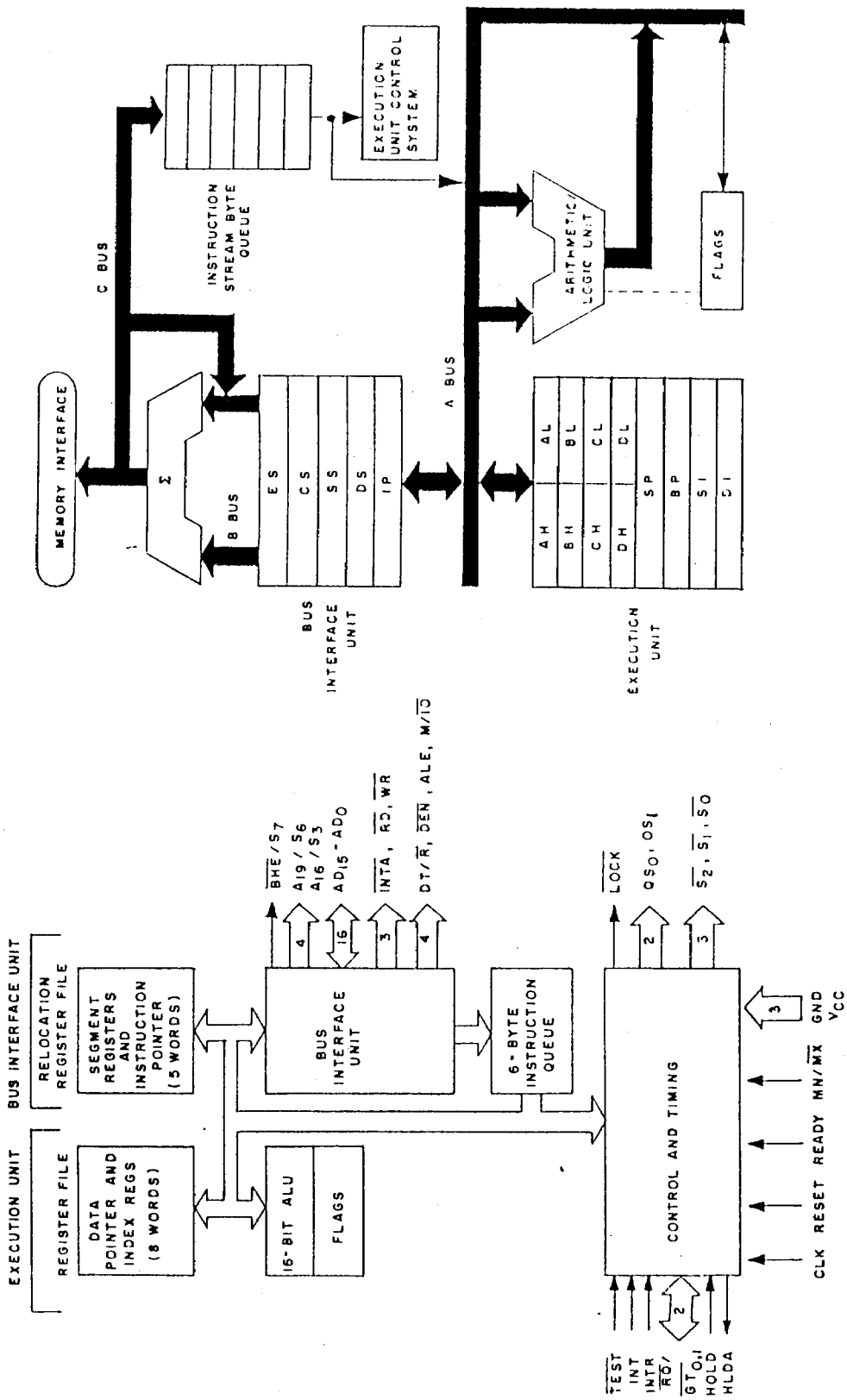


FIGURE 2. Functional diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84052
		REVISION LEVEL C	SHEET 11

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

Maximun mode

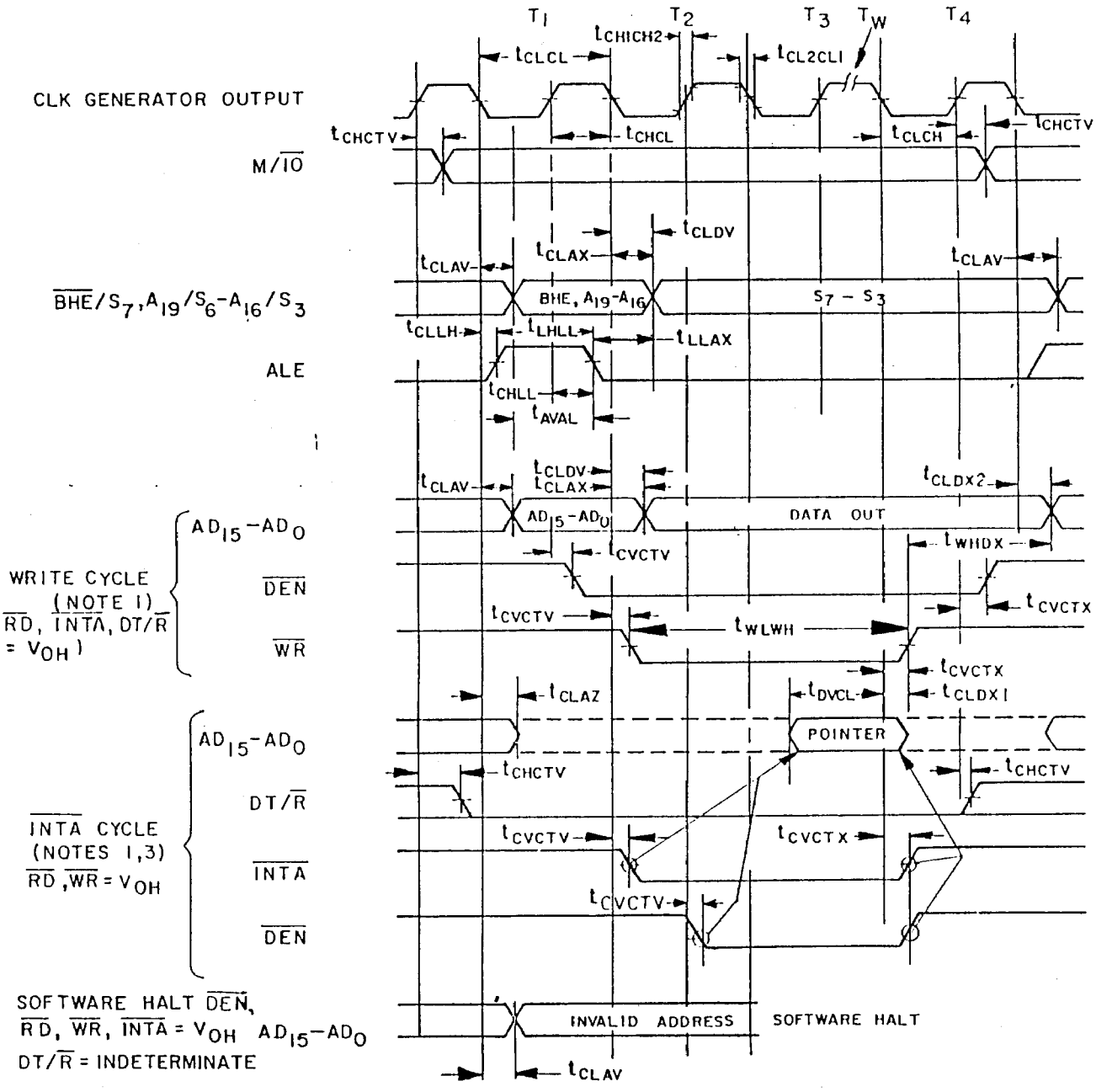
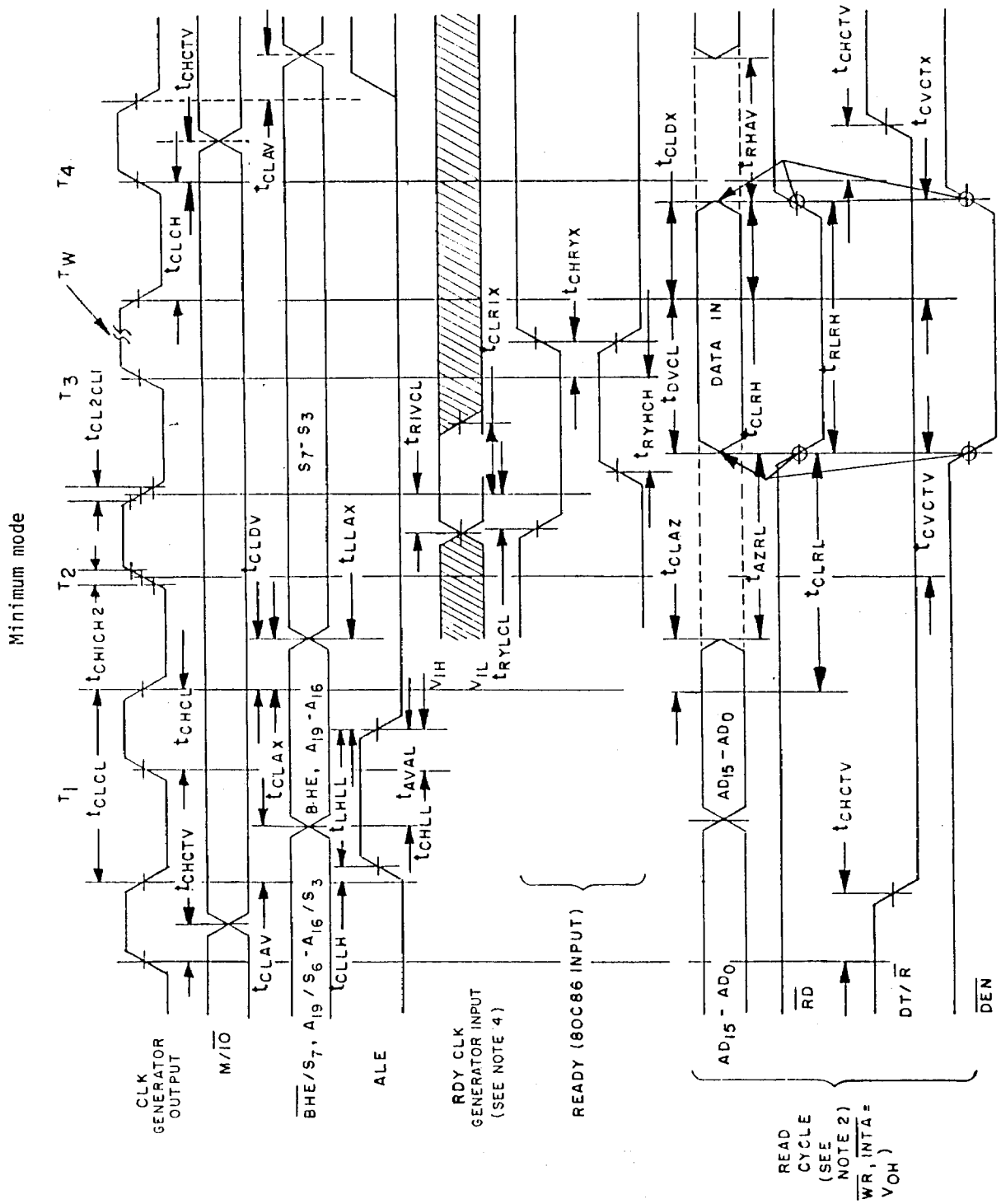


FIGURE 3. AC test circuit and waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84052
		REVISION LEVEL C	SHEET 12



NOTE: See note 5.

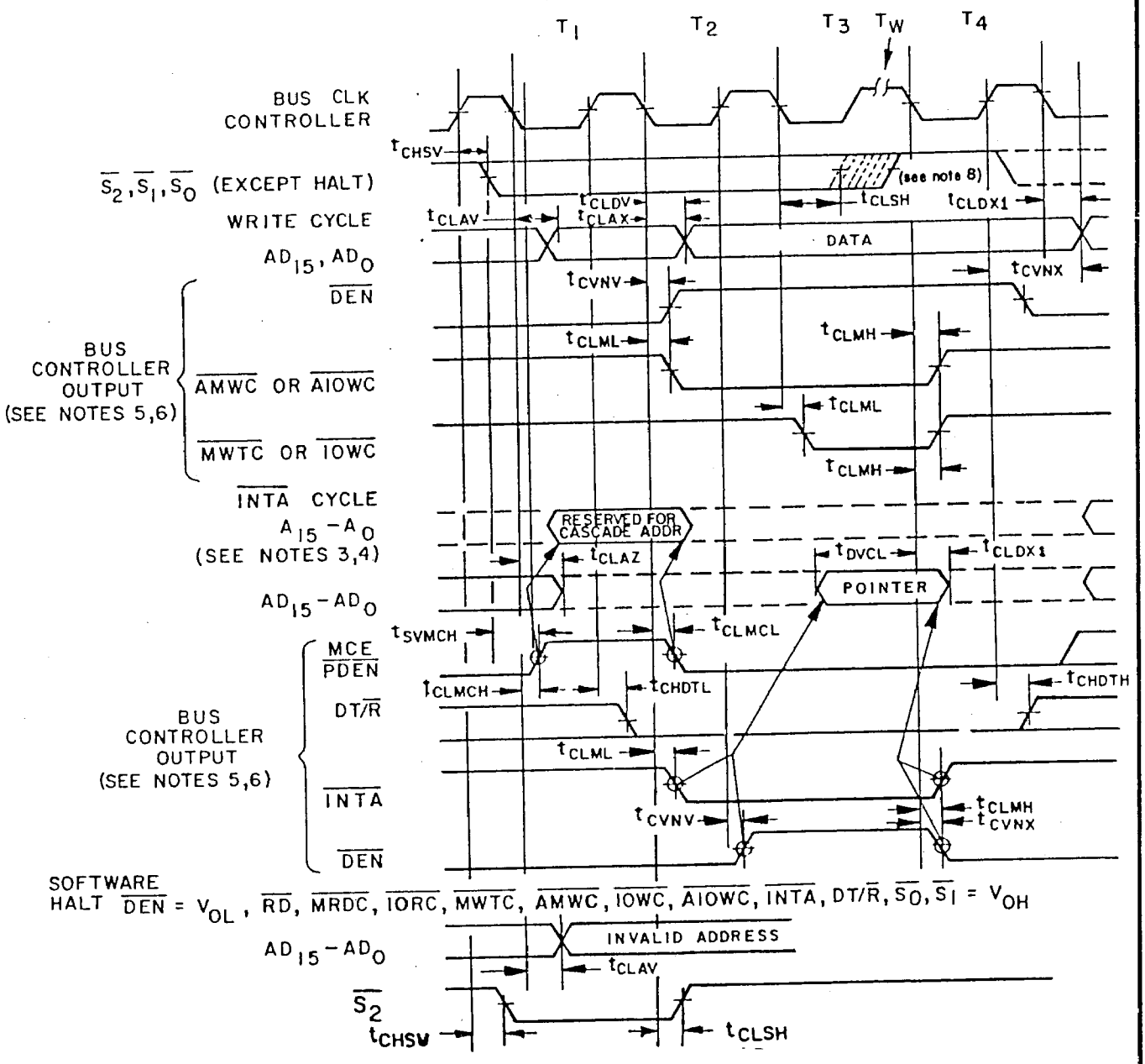
FIGURE 3. AC test circuit and waveforms - Continued.

Minimum mode

NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, and T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 80C86 local addr-data bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals are shown for reference only.
5. All timing measurements are made at 1.5 V unless otherwise noted.

FIGURE 3. AC test circuit and waveforms - Continued.

Maximum mode



See note 7.

FIGURE 3. AC test circuit and waveforms - Continued.

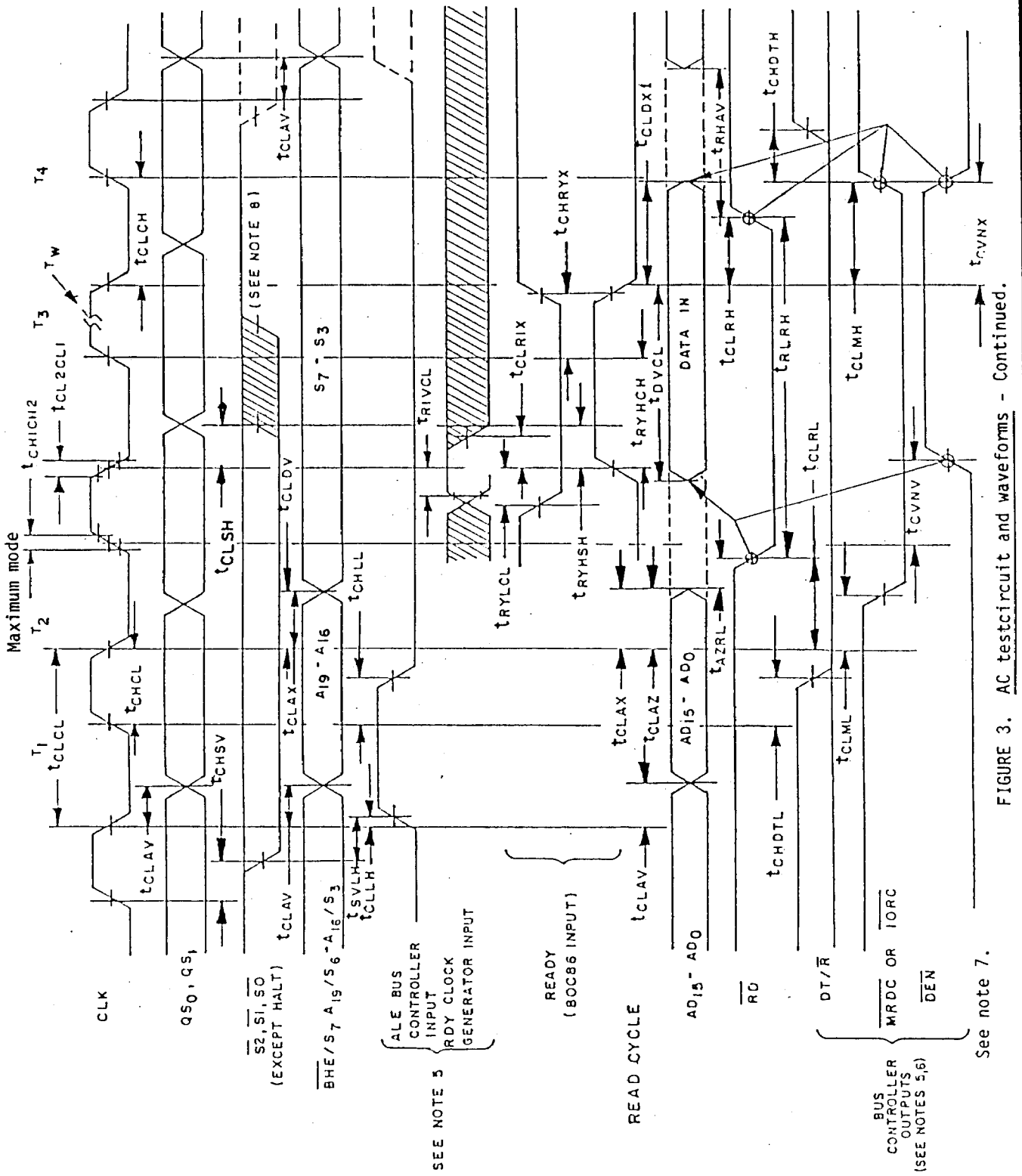
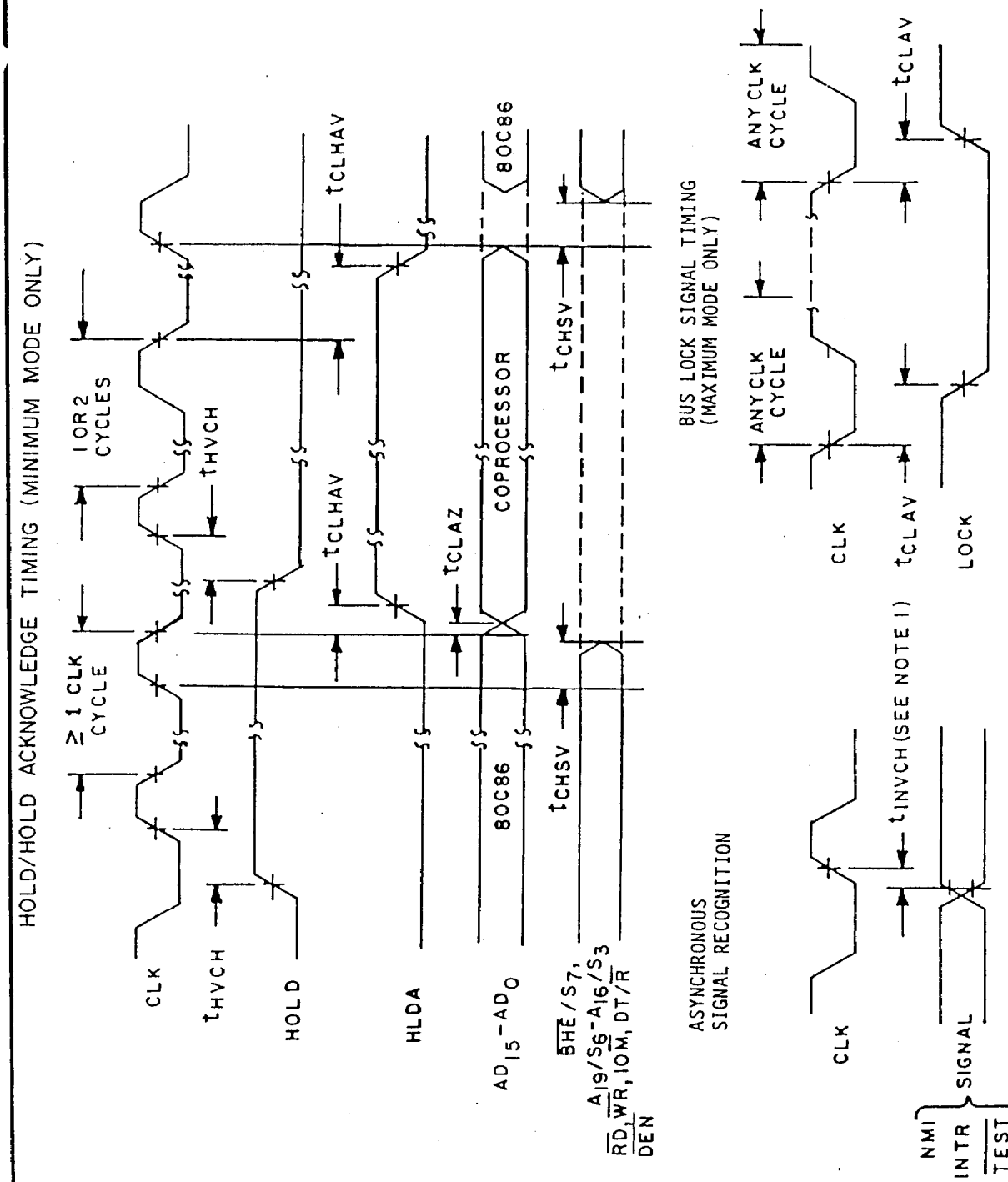


FIGURE 3. AC testcircuit and waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		84052
		REVISION LEVEL C	SHEET 16

DESC FORM 193A
SEP 87



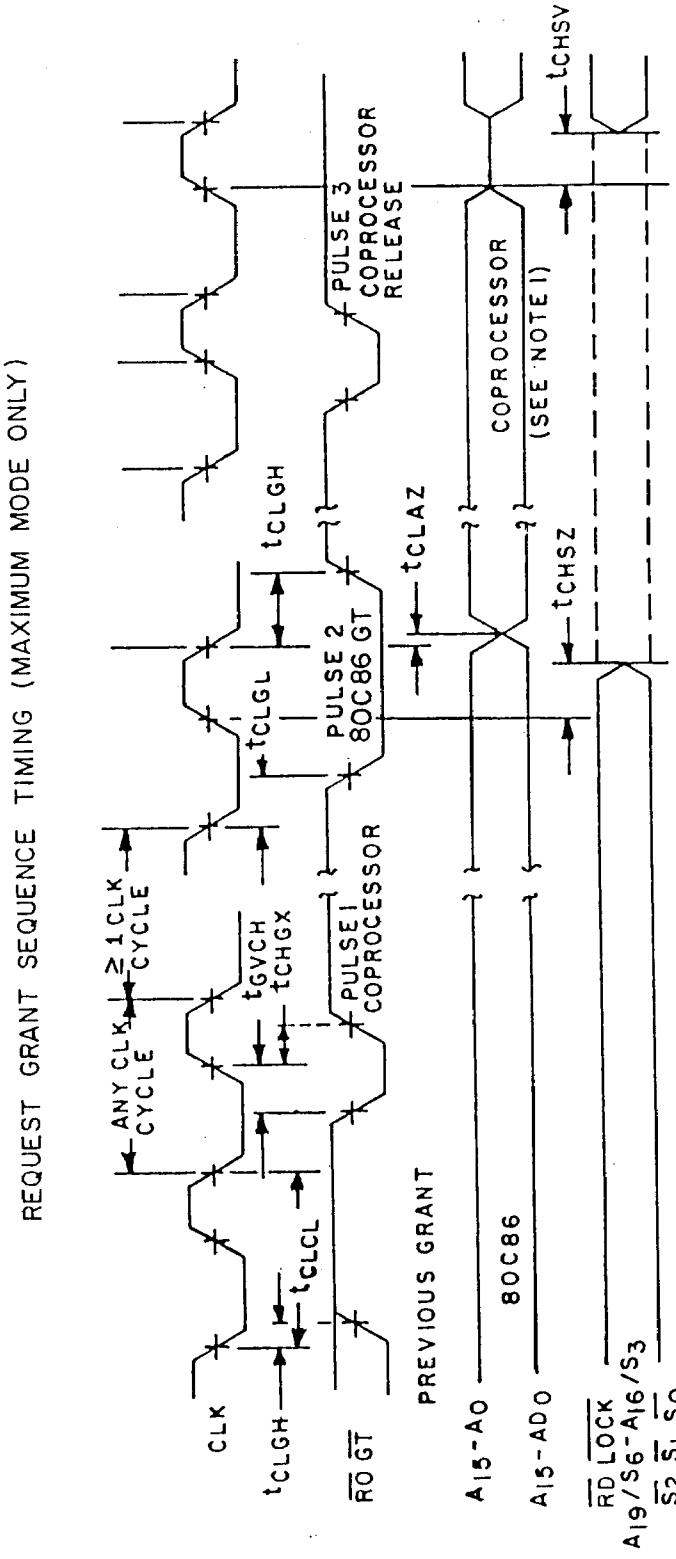
NOTE: Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

FIGURE 3. AC testcircuit and waveforms - Continued.

Maximum mode

NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, and T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycles.
4. Two INTA cycles run back-to-back. The 80C86 local addr-data bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
5. Signals are shown for reference only.
6. The issuance of the bus controlled command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$, and $\overline{DEN}$) as the active high bus controller CEN.
7. All timing measurements are made at 1.5 V unless otherwise noted.
8. Status inactive in state just prior to T_4.

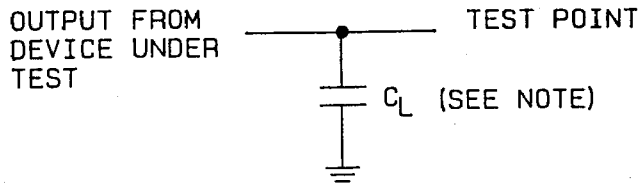
FIGURE 3. AC test circuit and waveforms - Continued.



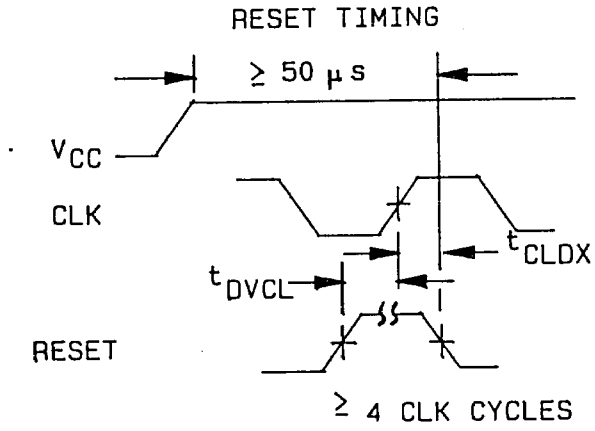
NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 3. AC test circuit and waveforms - Continued.

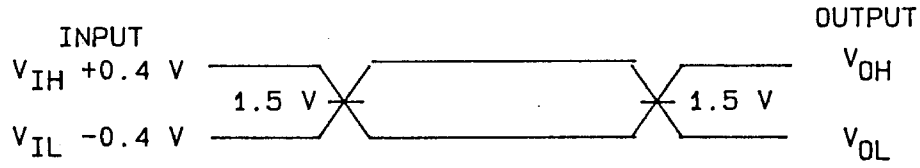
AC test circuit



NOTE: C_L = 100 pF stray and jig capacitance



AC testing input, output waveform.



AC testing: All input signals (other than CLK) must switch between $V_{IL(max)}$ -0.4 V and $V_{IH(min)}$ +0.4 V. CLK must switch between 0.4 V and V_{CC} -0.4 V. t_r and t_f are driven at 1 ns/V.

FIGURE 3. AC test circuit and waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available on shore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from approved source of supply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Initial electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*,2,3,7,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8 (125°C),10

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883 conditions.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional description for this device shall be as follows:

SYMBOL	Name and function (Minimum and maximum mode)
AD_{15} - AD_0	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions (see $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence."
A_{19}/S_6 A_{18}/S_5 A_{17}/S_4 A_{16}/S_3	ADDRESS/STATUS: During T_1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. S_6 is always low. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. S_4 and S_3 are encoded as follows:

S_4	S_3	Characteristics
0 (LOW)	0	Alternate data
0	1	Stack
1 (HIGH)	0	Code or none
1	1	Data
S_6 is 0 (LOW)		

This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".

$\overline{BHE}/S_7$	BUS HIGH ENABLE/STATUS: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and is held to high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge". It is LOW during T_1 for the first interrupt acknowledge cycle.

Name and function
(Minimum and maximum mode)

SYMBOL

$\overline{BHE}$	A_0	Characteristics
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

$\overline{RD}$ — READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the $\overline{S_2}$ or M/$\overline{IO}$ pin. This signal is used to read devices which reside on the microprocessor local bus. RD is active LOW during T_2, T_3, and T_W of any read cycle, and remains HIGH in T_2 until the microprocessor local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence."

READY — READY: Is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the Clock Generator to form READY. This signal is active HIGH. The microprocessor READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.

INTR — INTERRUPT REQUEST: A level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.

$\overline{TEST}$ — $\overline{TEST}$: Input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.

NMI — NON-MASKABLE INTERRUPT: An edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.

RESET — RESET: Causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and must remain active HIGH for at least four clock cycles. It restarts execution when RESET returns LOW. RESET is internally synchronized.

Name and function
(minimum mode)
$MN/\overline{MX} = V_{CC}$

SYMBOL	
CLK	CLOCK: Provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing.
V_{CC}	V_{CC} power supply pin. A 0.1 µF capacitor between pins 20 and 40 is recommended for decoupling. Reference pin numbers are for case Q. A 0.1 µF capacitor should be connected between pins 2z and 4a for case X.
GND	GND: Ground.
$MN/\overline{MX}$	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in.
$M/\overline{IO}$	STATUS LINE: Logically equivalent to $\overline{S_2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. $M/\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). $M/\overline{IO}$ is held high impedance logic zero internally during local bus "hold acknowledge".
$\overline{WR}$	WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the $M/\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and is held to high impedance logic one internally during local bus "hold acknowledge."
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE: Is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3, and T_W of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	ADDRESS LATCH ENABLE: Provided by the processor to latch the address into the external address latch. It is a HIGH pulse active during clock low of T_1 of any bus cycle. Note that ALE is never floated.
$DT/\overline{R}$	DATA TRANSMIT/RECEIVE: Is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, $DT/\overline{R}$ is equivalent to $\overline{S_1}$ in maximum mode, and its timing is the same as for $IO/\overline{M}$ (T = HIGH, R = LOW). This signal is held to a high impedance logic one internally during local bus "hold acknowledge."
$\overline{DEN}$	DATA ENABLE: Is provided as an output enable for the bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T_2 until the middle of T_4, while for a write cycle, it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ is held to high impedance logic one internally during local bus "hold acknowledge."

Name and function (maximum mode) $MN/\overline{MX}$ = GND	SYMBOL
HOLD: Indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.	HOLD HLDA
STATUS: active during T_4, T_1, and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These signals are held internally to a high impedance logic one state during "grant sequence."	$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

These status lines are encoded as follows:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

REQUEST/GRANT: Pins are used by other local bus masters to force the RQ/GT_1 processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ/GT_0}$ having higher priority than $\overline{RQ/GT_1}$. $\overline{RQ/GT}$ has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see figure 3): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the device (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse one clock wide from the device to the requesting master (pulse 2), indicates that the device has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence." The same rules as for HOLD/HOLDA apply as for when the bus is released.	$\overline{RQ/GT_0}$

Name and function
(maximum mode)
MN/$\overline{MX}$ = GND

SYMBOL

3. A pulse one CLK wide from the requesting master indicates to the device (pulse 3) that the "hold" request is about to end and that the device can reclaim the local bus at the next CLK. The CPU then enters T_4.

Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.

If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:

1. Request occurs on or before T_2.
2. Current cycle is not the low bit of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.

If the local bus is idle when the request is made, the two possible events will follow:

1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.

$\overline{LOCK}$

$\overline{LOCK}$: Indicates that other system bus masters are not go gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "$\overline{LOCK}$" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held high internally during "grant sequence."

QS_1, QS_0

QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed.

QS_1 and QS_0 provide status to allow external tracking of the internal instruction queue. Note that QS_1, QS_0 never become high impedance.

QS_1	QS_0	
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number
8405201QX	34371 34649	MD80C86/883 MD80C86/B
8405201XX	34371	MR80C86/883
8405202QX	34371 34649	MD80C86-2/883 MD80C86-2/B
8405202XX	34371	MR80C86-2/883

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor 200 Palm Bay Boulevard P. O. Box 883 Melbourne, FL 32901
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 West Williams Field Road Chandler, AZ 85224