

## Features

- 2.7V to 3.6V Supply  
Full Read and Write Operation
- Low Power Dissipation  
8 mA Active Current  
50  $\mu$ A CMOS Standby Current
- Read Access Time - 300 ns
- Byte Write - 3 ms
- Direct Microprocessor Control  
DATA Polling  
READY/BUSY Open Drain Output
- High Reliability CMOS Technology  
Endurance: 100,000 Cycles  
Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

## Description

The AT28BV64 is a low-voltage, low-power Electrically Erasable and Programmable Read Only Memory specifically designed for battery powered applications. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50  $\mu$ A.

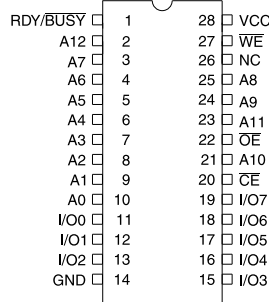
The AT28BV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Fol-

(continued)

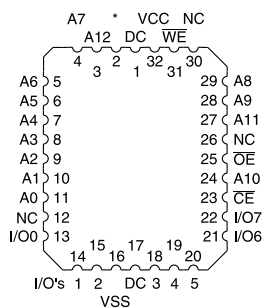
## Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
$\overline{\text{RDY/BUSY}}$	Ready/Busy Output
NC	No Connect
DC	Don't Connect

PDIP, SOIC Top View

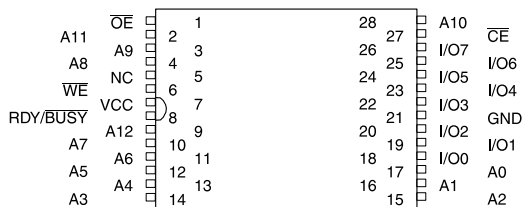


PLCC Top View



\* =  $\overline{\text{RDY/BUSY}}$

TSOP Top View



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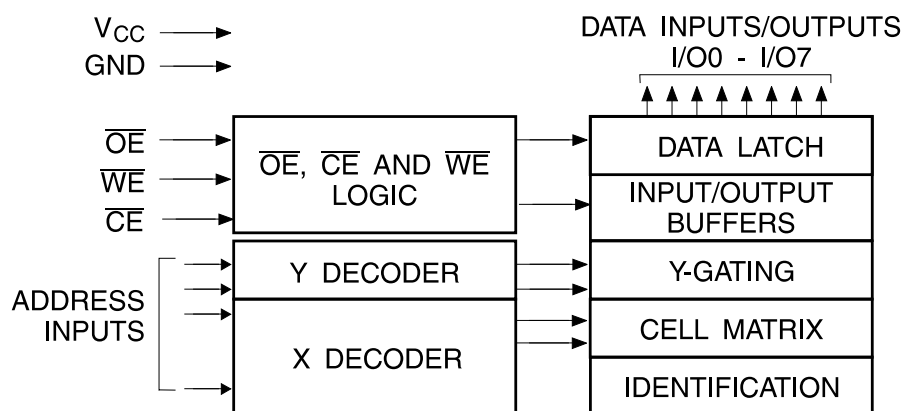


## Description (Continued)

Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY and DATA polling of I/O<sub>7</sub>. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's 28BV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of E<sup>2</sup>PROM are available for device identification or tracking.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground .....	-0.6V to +6.25V
All Output Voltages with Respect to Ground .....	-0.6V to V <sub>CC</sub> + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground .....	-0.6V to +13.5V

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Device Operation

**READ:** The AT28BV64 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers increased flexibility in preventing bus contention.

**BYTE WRITE:** Writing data into the AT28BV64 is similar to writing into a Static RAM. A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{OE}$  high and  $\overline{CE}$  or  $\overline{WE}$  low (respectively) initiates a byte write. The address location is latched on the falling edge of  $\overline{WE}$  (or  $\overline{CE}$ ); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{wc}$ , a read operation will effectively be a polling operation.

**READY/BUSY:** Pin 1 is an open drain  $\overline{RDY/BUSY}$  output that can be used to detect the end of a write cycle.  $\overline{RDY/BUSY}$  is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same  $\overline{RDY/BUSY}$  line.

**DATA POLLING:** The AT28BV64 provides  $\overline{DATA POLLING}$  to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O<sub>7</sub> (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

**WRITE PROTECTION:** Inadvertent writes to the device are protected against in the following ways. (a)  $V_{CC}$  sense— if  $V_{CC}$  is below 1.8V (typical) the write function is inhibited. (b)  $V_{CC}$  power on delay— once  $V_{CC}$  has reached 2.0V the device will automatically time out 10 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits byte write cycles.

## DC and AC Operating Range

		AT28BV64-30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
Vcc Power Supply		2.7V to 3.6V

## Operating Modes

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write (2)	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	X	
Output Disable	X	V <sub>IH</sub>	X	High Z

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.  
2. Refer to AC Programming Waveforms.

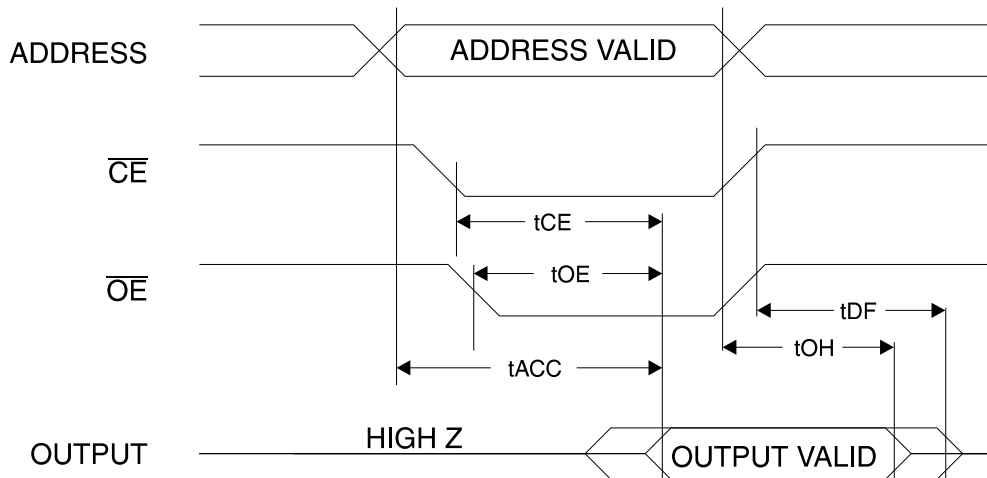
## DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> + 1.0V		5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>CC</sub>		5	μA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{\text{CE}}$ = V <sub>CC</sub> - 0.3V to V <sub>CC</sub> + 1.0V		50	μA
I <sub>CC</sub>	V <sub>CC</sub> Active Current AC	f = 5 MHz; I <sub>OUT</sub> = 0 mA; CE = V <sub>IL</sub>		8	mA
V <sub>IL</sub>	Input Low Voltage			0.6	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1 mA		0.3	V
		I <sub>OL</sub> = 2 mA for RDY/ $\overline{\text{BUSY}}$		0.3	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100 μA	2.0		V

## AC Read Characteristics

Symbol	Parameter	AT28BV64-30		Units
		Min	Max	
$t_{ACC}$	Address to Output Delay		300	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		300	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	150	ns
$t_{DF}^{(3,4)}$	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	60	ns
$t_{OH}$	Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	0		ns

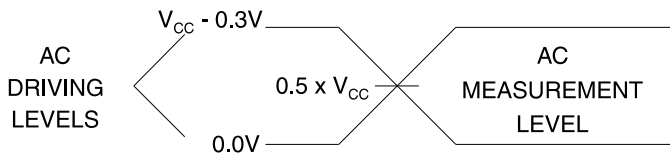
## AC Read Waveforms (1, 2, 3, 4)



- Notes:
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
  - $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .

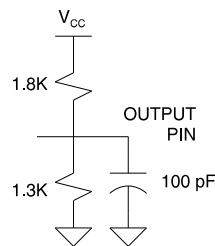
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5 \text{ pF}$ ).
- This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



$t_R, t_F < 20 \text{ ns}$

## Output Test Load



## Pin Capacitance ( $f = 1 \text{ MHz}$ , $T = 25^\circ\text{C}$ ) <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

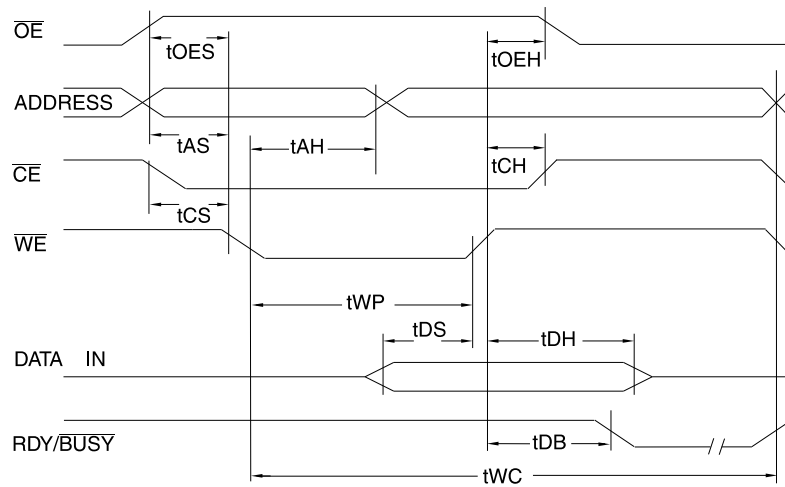
Note: 1. This parameter is characterized and is not 100% tested.

## AC Write Characteristics

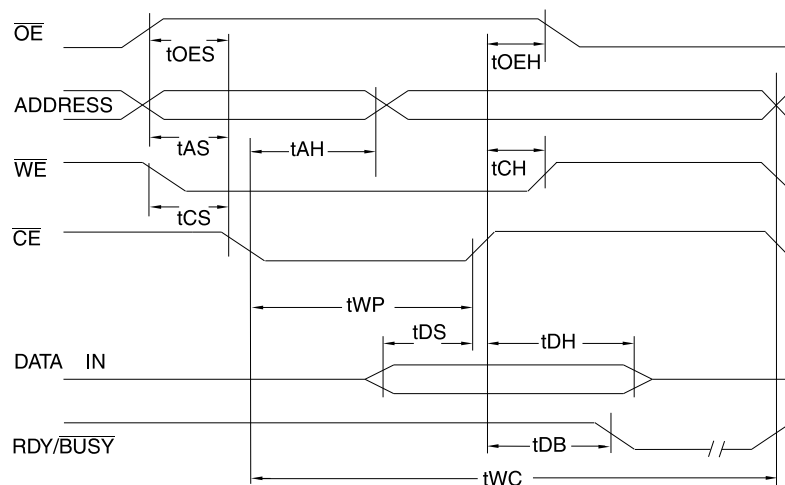
Symbol	Parameter	Min	Max	Units
$t_{AS}, t_{OES}$	Address, $\overline{OE}$ Set-up Time	10		ns
$t_{AH}$	Address Hold Time	100		ns
$t_{WP}$	Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ )	150	1000	ns
$t_{DS}$	Data Set-up Time	100		ns
$t_{DH}, t_{OEH}$	Data, $\overline{OE}$ Hold Time	10		ns
$t_{DB}$	Time to Device Busy		50	ns
$t_{WC}$	Write Cycle Time		3	ms

## AC Write Waveforms

### $\overline{WE}$ Controlled



### $\overline{CE}$ Controlled

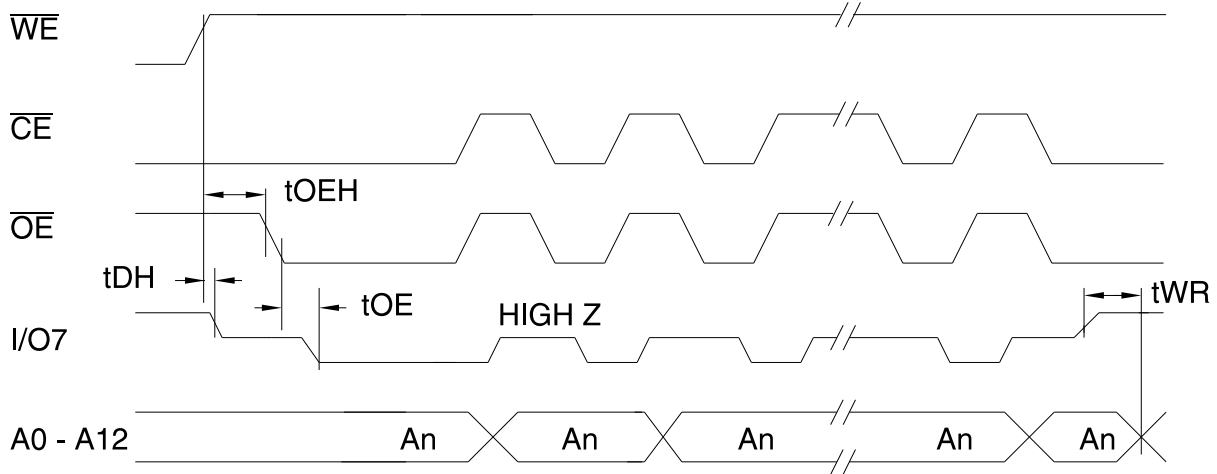


### Data Polling Characteristics <sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Units
t <sub>DH</sub>	Data Hold Time	10			ns
t <sub>OE<math>\overline{H}</math></sub>	$\overline{OE}$ Hold Time	10			ns
t <sub>OE</sub>	$\overline{OE}$ to Output Delay <sup>(2)</sup>				ns
t <sub>WR</sub>	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.  
 2. See AC Read Characteristics.

### Data Polling Waveforms





## Ordering Information <sup>(1)</sup>

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Operating Voltage	Ordering Code	Package	Operation Range
	Active	Standby				
300	8	0.05	2.7V to 3.6V	AT28BV64-30JC AT28BV64-30PC AT28BV64-30SC AT28BV64-30TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
	8	0.05	2.7V to 3.6V	AT28BV64-30JI AT28BV64-30PI AT28BV64-30SI AT28BV64-30TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

## Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV64	30	JC, JI, PC, PI, SC, SI, TC, TI

Package Type	
<b>32J</b>	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>28P6</b>	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>28S</b>	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
<b>28T</b>	28 Lead, Plastic Thin Small Outline Package (TSOP)