

October 1987 Revised January 1999

CD4514BC• CD4515BC 4-Bit Latched/4-to-16 Line Decoders

General Description

The CD4514BC and CD4515BC are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514BC (output active high option) presents a logical "1" at the selected output, whereas the CD4515BC presents a logical "0" at the selected output. The input latches are R-S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL: fan out of 2 compatibility: driving 74L
- Low quiescent power dissipation: 0.025 µW/package @ 5.0 V_{DC}
- Single supply operation
- Input impedance = $10^{12}\Omega$ typically
- Plug-in replacement for MC14514, MC14515

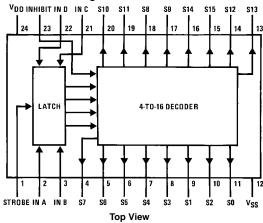
Ordering Code:

Order Number	Package Number	Package Diagram					
CD4514BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide					
CD4514BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide					
CD4515BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide					
CD4515BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide					

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for SOIC and DIP



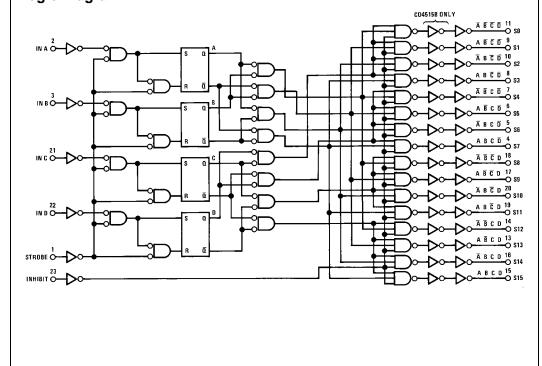
Truth Table

Decode Truth Table (Strobe = 1)

	Data Inputs				Selected Output		
Inhibit	D	С	В	Α	CD4514 = Logic "1"		
					CD4515 = Logic "0"		
0	0	0	0	0	S0		
0	0	0	0	1	S1		
0	0	0	1	0	S2		
0	0	0	1	1	S3		
0	0	1	0	0	S4		
0	0	1	0	1	S5		
0	0	1	1	0	S6		
0	0	1	1	1	S7		
0	1	0	0	0	S8		
0	1	0	0	1	S9		
0	1	0	1	0	S10		
0	1	0	1	1	S11		
0	1	1	0	0	S12		
0	1	1	0	1	S13		
0	1	1	1	0	S14		
0	1	1	1	1	S15		
1	Х	Х	Х	Х	All Outputs = 0, CD4514		
					All Outputs = 1, CD4515		

X = Don't Care

Logic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_{DD}) -0.5 V to +18 V Input Voltage (V_{IN}) $-0.5 \text{V to } \text{V}_{\text{DD}} + 0.5 \text{V}$

Storage Temperature Range (T_S) $-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD}) 3V to 15V Input Voltage (V_{IN}) 0V to V_{DD}

Operating Temperature Range (T_A)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

CD4514BC, CD4515BC

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
Cymbol	rarameter	Conditions	Min	Max	Min	Тур	Max	Min	Max	Jillis
I _{DD}	Quiescent Device	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.005	20		150	μΑ
	Current	$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		40		0.010	40		300	μΑ
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		80		0.015	80		600	μΑ
V _{OL}	LOW Level	$V_{IL} = 0V$, $V_{IH} = V_{DD}$,								
	Output Voltage	$ I_O < 1 \mu A$							Max 150 300	
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V _{OH}	HIGH Level	$V_{IL} = 0V$, $V_{IH} = V_{DD}$,								
	Output Voltage	$ I_O < 1 \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		V _{DD} = 10V	9.95		9.95	10.0		9.95		V
		V _{DD} = 15V	14.95		14.95	15.0		14.95	1.5	V
V _{IL}	LOW Level	I _O < 1 μA								
	Input Voltage	$V_{DD} = 5V$, $V_{O} = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V, V_{O} = 1.5V \text{ or } 13.5V$		4.0		6.75	4.0		4.0	V
V _{IH}	HIGH Level	I _O < 1 μA								
	Input Voltage	$V_{DD} = 5V$, $V_{O} = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_{O} = 1.0V \text{ or } 9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V, V_{O} = 1.5V \text{ or } 13.5V$	11.0		11.0	8.25		11.0		V
l _{OL}	LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.52		0.44	0.88		0.36		mA
	Current (Note 3)	$V_{DD} = 10V, V_{O} = 0.5V$	1.3		1.1	2.25		0.90		mA
		$V_{DD} = 15V, V_{O} = 1.5V$	3.6		3.0	8.8		2.4	1.5 3.0 4.0	mA
I _{OH}	HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
·OH	Current (Note 3)	$V_{DD} = 10V, V_{O} = 9.5V$	-1.3		-1.1	-2.25		-0.90		mA
		$V_{DD} = 15V, V_{O} = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I _{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10 ⁻⁵	-0.3		-1.0	μΑ
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10 ⁻⁵	0.3		1.0	μΑ
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Note 3: I_{OH} and I_{OL} are tested one output at a time.

CD4514BC• CD4515BC

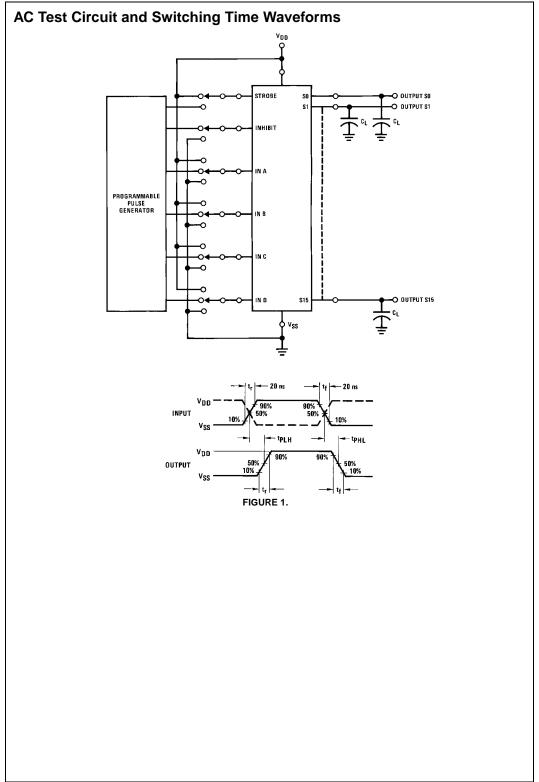
AC Electrical Characteristics (Note 4) All types $C_L=50$ pF, $T_A=25^{\circ}C$, $t_r=t_f=20$ ns unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{THL} , t _{TLH}	Transition Times	V _{DD} = 5V		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		V _{DD} = 15V		40	80	ns
t _{PLH} , t _{PHL}	Propagation Delay Times	$V_{DD} = 5V$		550	1100	ns
		$V_{DD} = 10V$		225	450	ns
		V _{DD} = 15V		150	300	ns
t _{PLH} , t _{PHL}	Inhibit Propagation	$V_{DD} = 5V$		400	800	ns
	Delay Times	$V_{DD} = 10V$		150	300	ns
		V _{DD} = 15V		100	200	ns
t _{SU}	Setup Time	$V_{DD} = 5V$		125	250	ns
		V _{DD} = 10V		50	100	ns
		$V_{DD} = 15V$		38	75	ns
t _{WH}	Strobe Pulse Width	$V_{DD} = 5V$		175	350	ns
		$V_{DD} = 10V$		50	100	ns
		V _{DD} = 15V		38	75	ns
C _{PD}	Power Dissipation Capacitance	Per Package (Note 5)		150		pF
C _{IN}	Input Capacitance	Any Input (Note 6)		5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note,

Note 6: Capacitance is guaranteed by periodic testing.



Applications

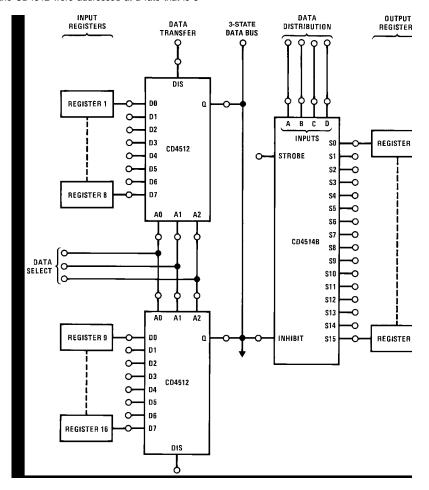
Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-STATE data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

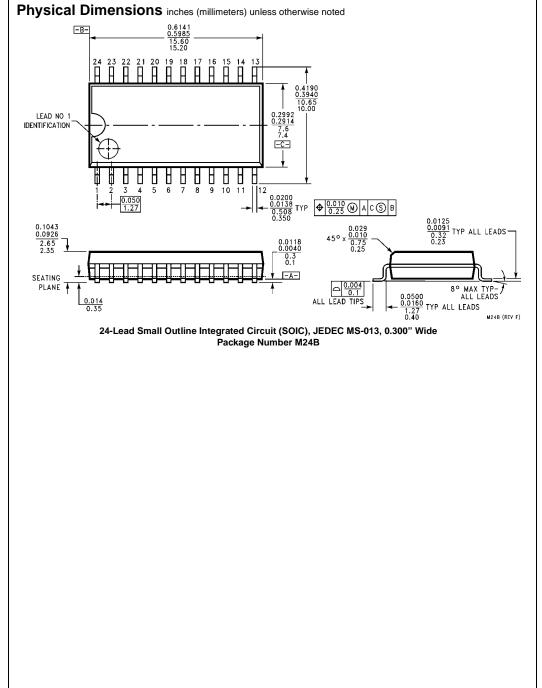
Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the 3-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

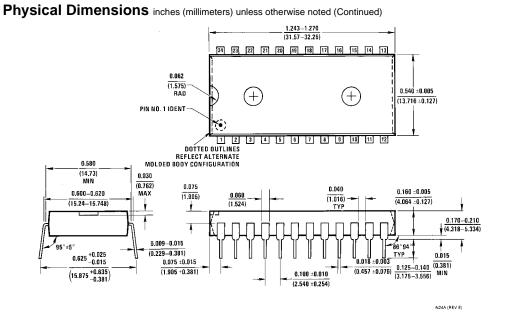
In addition to a choice of input registers, 1–16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is 8

times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA-IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A-P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.







24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide Package Number N24A

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