Integrated Device Technology, Inc.

128K x 8 CMOS STATIC RAM

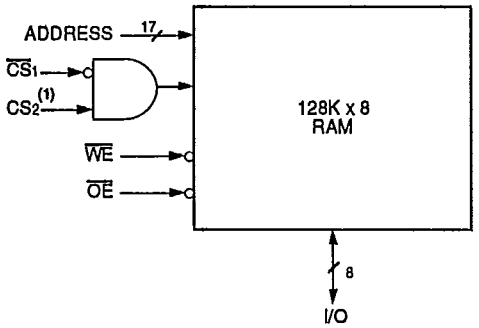
IDT71M024
IDT71M025

T-46-23-14

FEATURES:

- High density 1 megabit (128K x 8) static RAM
- Dual Chip Select Version (IDT71M024)
  Single Chip Select Version (IDT71M025)
- Fast access time:
  – commercial: 55ns (max.)
  – military: 60ns (max.)
- Low power consumption
  – active: 100mA (max.)
  – CMOS standby: 2mA (max.)
- Very low power version
  – data retention: 50µA (max.) Vcc = 3V
  – CMOS standby: 100µA (max.)
- 32-pin ceramic sidebrazed DIP or ceramic leadless chip carrier (LCC)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

FUNCTIONAL BLOCK DIAGRAM



2820 drw 01

NOTE:
1. For the IDT71M024 version only.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-16	Addresses
$\overline{CS}_1$, CS_2	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
N.C.	No Connect
Vcc	Power
GND	Ground

2820 tbl 01

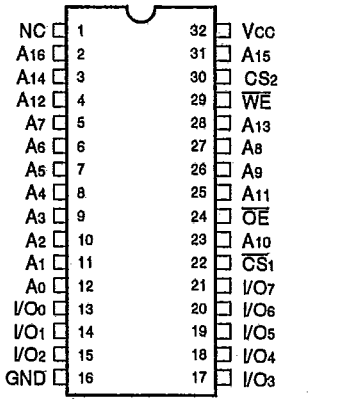
DESCRIPTION:

The IDT71M024/71M025 is a 1 megabit (128K x 8) static RAM packaged in a sidebrazed ceramic dual in-line package (DIP) and a ceramic leadless chip carrier (LCC). The IDT71M024/71M025 is available with access times as fast as 55ns. For battery backup applications, a very low power version is available, offering a commercial temperature data retention current of 50µA with Vcc = 3V.

The IDT71M024/71M025 are packaged in JEDEC standard 600 mil 32-pin ceramic DIPs. The IDT71M024 as comes in a hermetic 400 mil by 820 mil LCC. For surface mount applications, the proposed JEDEC standard 400 mil by 820 mil LCC is ideal.

All inputs and outputs of the IDT71M024/71M025 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use. All IDT military semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION(1)



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DIP, LCC
TOP VIEW

NOTE:
1. For the IDT71M024 version Pin 30=CS2. For the IDT71M025 version Pin 30=N.C.

TRUTH TABLE[1]

Mode	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	L	X	X	High-Z	Standby
Read	L	H	L	H	DOUT	Active
Read	L	H	H	H	High-Z	Active
Write	L	H	X	L	DIN	Active

NOTE: 2820 tbl 02
1. CS_2 is available for the IDT71M024 version only.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2820 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2820 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2820 tbl 04
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2820 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	2.5	—	5	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS_1}$ = VIH and CS_2 = VIL, VOUT = GND to VCC	—	2.5	—	5	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA,	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ 1≤ VIL and CS_2 ≥ VIH, f = fMAX, Outputs Open	—	100	—	100	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS_1}$ ≥ VIH and CS_2 ≤ VIL, VCC = Max., f = fMAX, Outputs Open	—	2.5	—	2.5	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS_1}$ ≥ VCC - 0.2V and CS_2 ≤ 0.2V VIN ≥ VCC - 0.2V or ≤ 0.2V	—	2	—	2	mA
		Very Low Power Version[1]	—	100	—	350	µA

NOTE: 2820 tbl 07
1. For data retention version, please specify L power when ordering.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2820 tbl 08

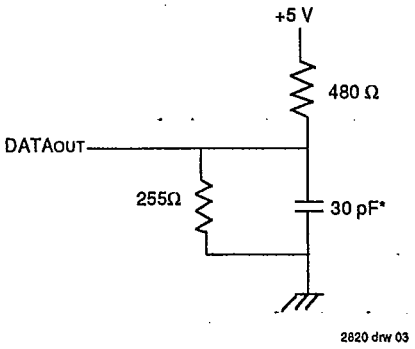


Figure 1. Output Load

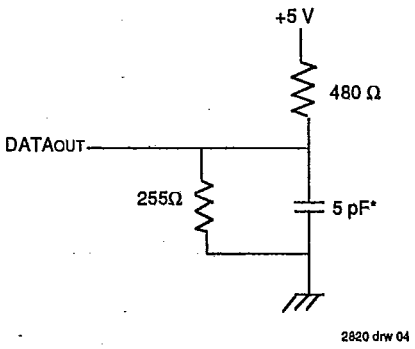


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

* Including scope and jig

DATA RETENTION CHARACTERISTICS[1]

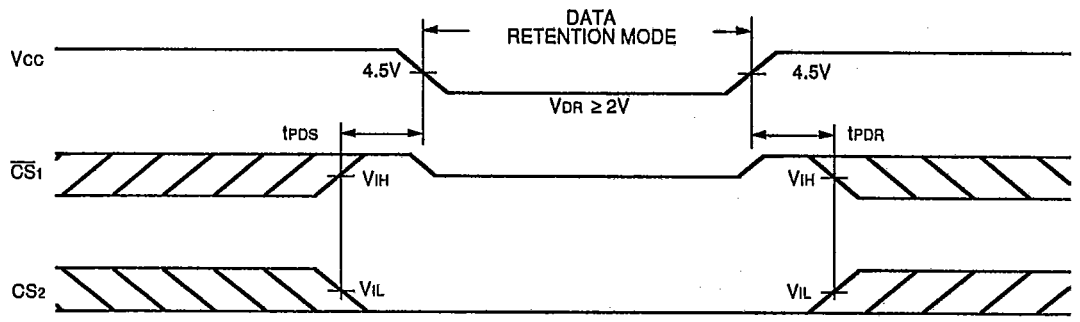
(TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Comm. Max.	Military Max.	Unit
V_{DR}	Vcc for Data Retention	—	2.0	—	—	V
$V_{\overline{CS}1}$	$\overline{CS}_1$ Input Voltage	$V_{DR} \geq 2.2V$	2.2	—	—	V
V_{CS2}	CS_2 Input Voltage	$V_{DR} \geq 4.5V$	—	0.8	0.8	V
		$V_{DR} < 4.5V$	—	0.2	0.2	V
I_{CCDR1}	Data Retention Current	V_{CC} = 3.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	300	µA
I_{CCDR2}	Data Retention Current	V_{CC} = 2.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	200	µA
t_{PDS}[2]	Power Down Set Up Time		0	—	—	ns
t_{PDR}[2]	Power Down Recovery Time		t_{RC}[3]	—	—	ns

NOTES:
1. This option is only offered when ordering L power version.
2. This parameter is guaranteed by design, but not tested.
3. t_{RC} = Read Cycle Time.

2820 tbl 09

DATA RETENTION WAVEFORM



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AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	71M024 or 71M025 -55(2,3) Min.	-55(2,3) Max.	-60(2) Min.	-60(2) Max.	-65(2) Min.	-65(2) Max.	-70 Min.	-70 Max.	Unit
Read Cycle										
tRC	Read Cycle Time	60	—	65	—	70	—	70	—	ns
tAA	Address Access Time	—	55	—	60	—	65	—	70	ns
tACS1	Chip Select ($\overline{CS_1}$) Access Time	—	55	—	60	—	65	—	70	ns
tACS2	Chip Select (CS_2) Access Time	—	60	—	65	—	70	—	70	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	35	—	35	ns
tOHZ(1)	Output Disable to Output in High Z	—	20	—	25	—	25	—	25	ns
tOLZ(1)	Output Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tCLZ1,2(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ1,2(1)	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	ns
tOH	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	60	—	65	—	70	—	70	ns
Write Cycle										
tWC	Write Cycle Time	60	—	65	—	70	—	70	—	ns
tWP	Write Pulse Width	45	—	50	—	55	—	55	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tAW	Address Valid to End of Write	55	—	60	—	65	—	65	—	ns
tCW1	Chip Select ($\overline{CS_1}$) to End of Write	55	—	60	—	65	—	65	—	ns
tCW2	Chip Select (CS_2) to End of Write	55	—	60	—	65	—	65	—	ns
tDW	Data to Write Time Overlap	25		30	—	30	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	20	—	25	—	25	—	25	ns
tOW(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.
3 Commercial temperature only.

2820 tbl 10

T-46-23-14

AC ELECTRICAL CHARACTERISTICS

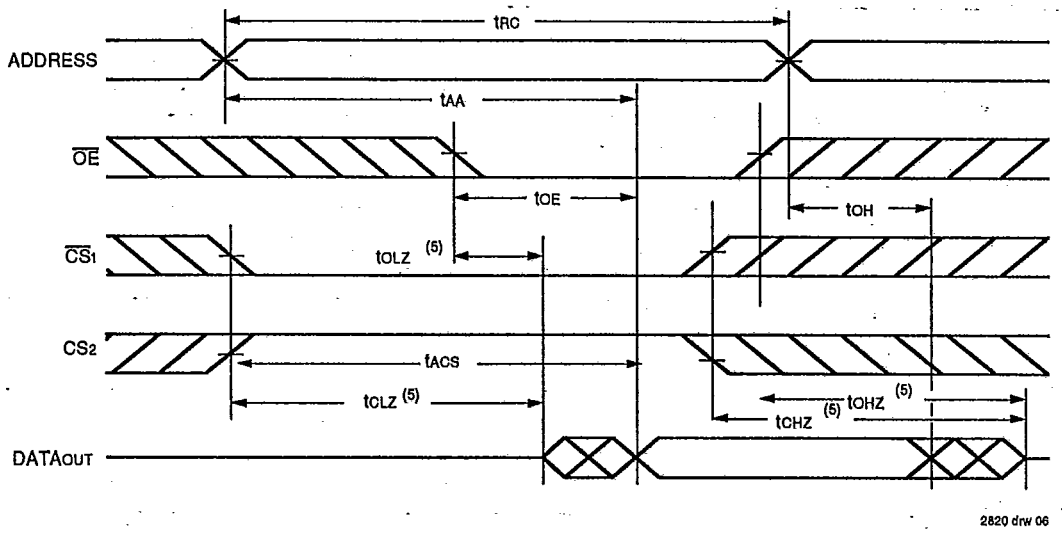
(Vcc = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	71M024 or 71M025 -85 Min.	-85 Max.	-100 Min.	-100 Max.	-120 Min.	-120 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS1}	Chip Select ($\overline{CS_1}$) Access Time	—	85	—	100	—	120	ns
t_{ACS2}	Chip Select (CS_2) Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	30	—	35	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
$t_{CLZ1,2}$[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
$t_{CHZ1,2}$[1]	Chip Deselect to Output in High Z	—	30	—	35	—	35	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	60	—	65	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	70	—	75	—	75	—	ns
t_{CW1}	Chip Select ($\overline{CS_1}$) to End of Write	70	—	75	—	75	—	ns
t_{CW2}	Chip Select (CS_2) to End of Write	70	—	75	—	75	—	ns
t_{DW}	Data to Write Time Overlap	35	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	30	—	35	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

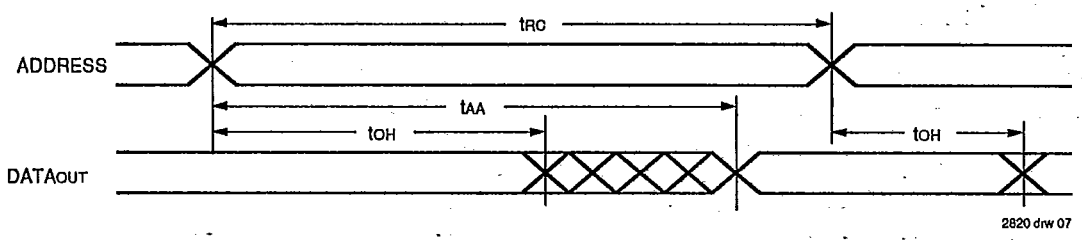
2620 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



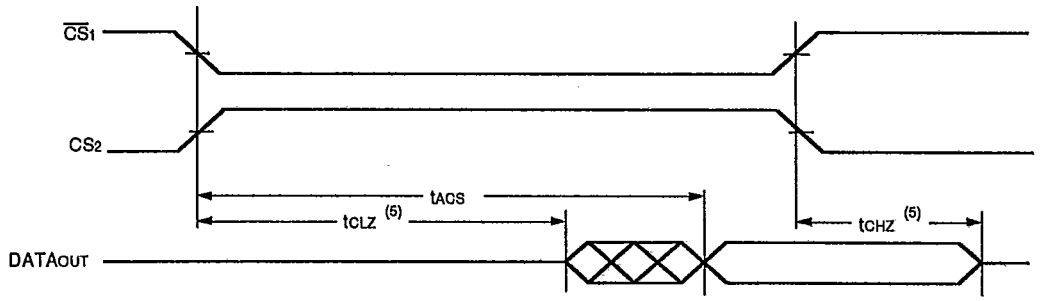
2820 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2820 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



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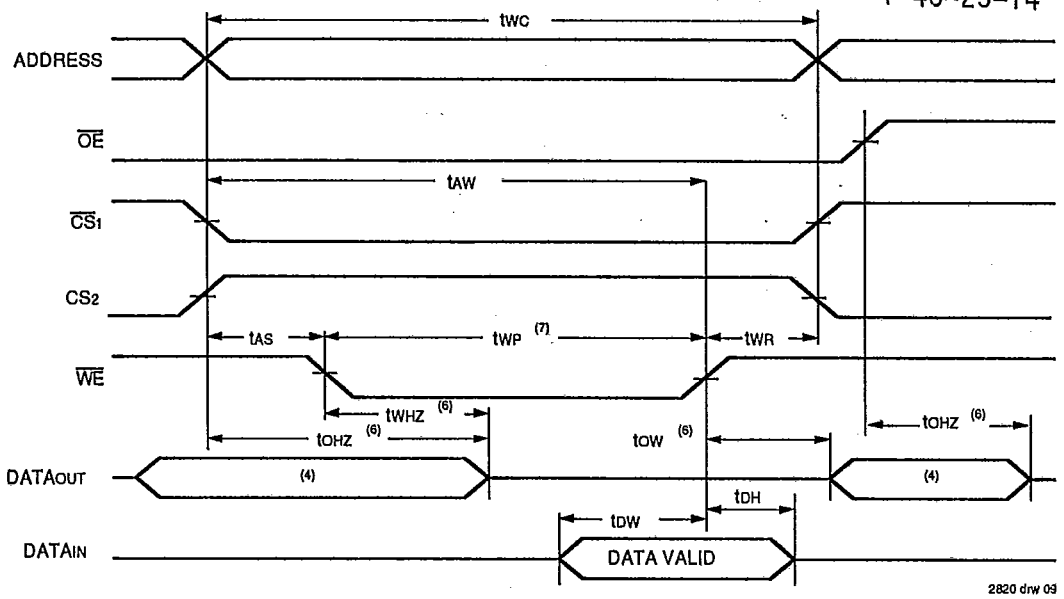
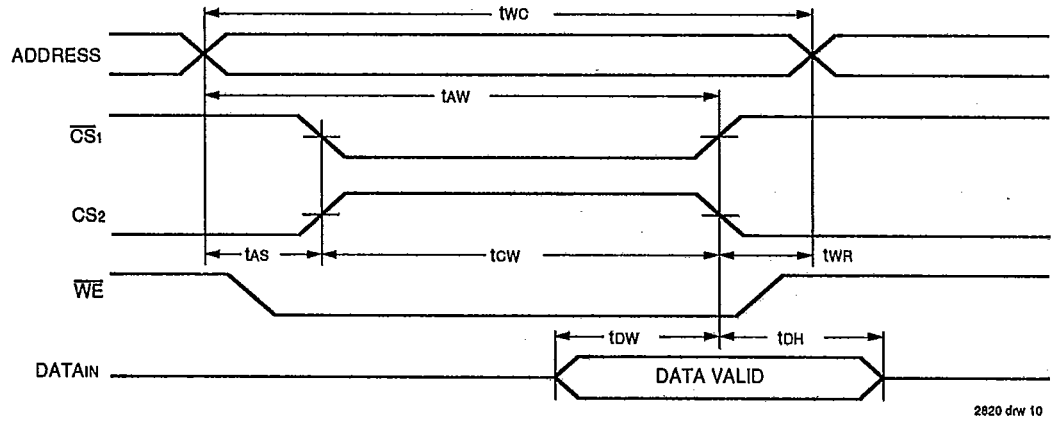
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

T-46-23-14

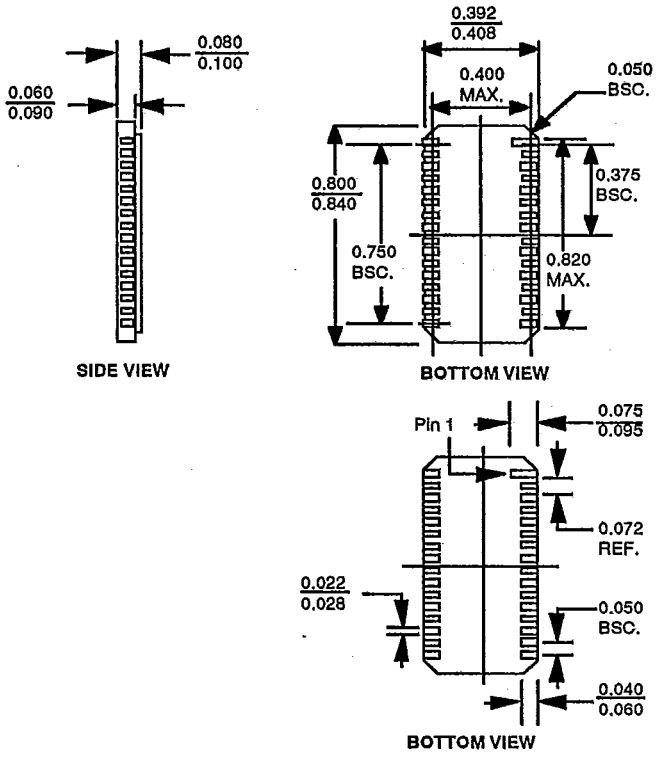


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS_1}$, CS_2 CONTROLLED TIMING)(1, 2, 3, 5)



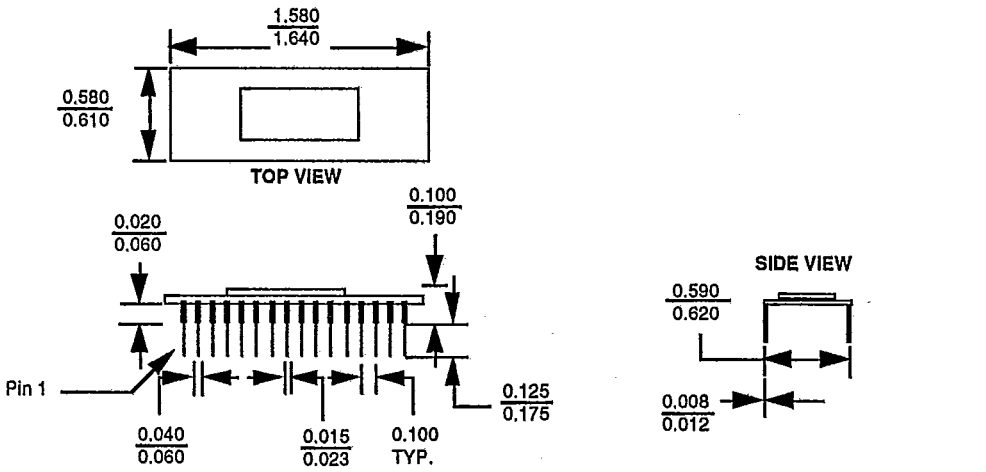
NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$ must be high, or CS_2 must be low during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, high CS_2, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS_1}$ low transition, CS_2 high transition occur simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, t_{WP} must be greater than $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS
400 MIL BY 820 MIL LCC PACKAGE



2820 drw 11

600 MIL DUAL IN-LINE PACKAGE



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