

DATA SHEET

74F579

8-bit bidirectional binary counter (3-State)

Product specification

1992 May 04

IC15 Data Handbook

8-bit bidirectional binary counter (3-State)

74F579

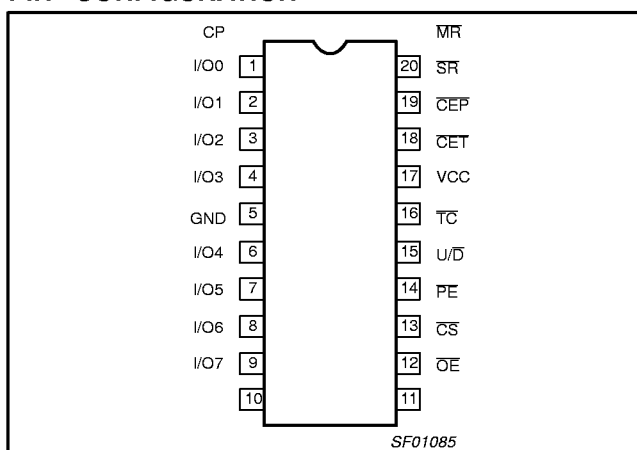
FEATURES

- Fully synchronous operation
- Multiplexed 3-State I/O ports for bus oriented applications
- Built in cascading carry capability
- U/ $\bar{D}$ pin to control direction of counting
- Separate pins for Master reset and Synchronous operation
- Center power pins to reduce effects of package inductance
- Count frequency 115MHz Typ
- Supply current 100mA Typ
- See 74F269 for 24-pin separate I/O port version
- See 74F779 for 16-pin version

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/ $\bar{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. TC output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

PIN CONFIGURATION



ORDERING INFORMATION

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{\text{CC}} = 5V \pm 10\%$, $T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	PKG DWG #
20-Pin Plastic DIP	N74F579N	SOT146-1
20-Pin Plastic SOL	N74F579D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

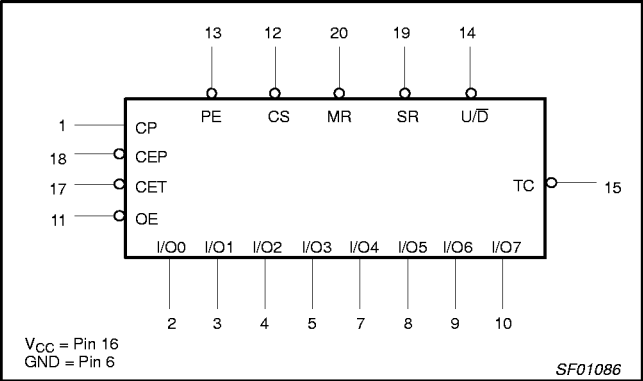
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O _n	Data Inputs	3.5/1.0	70 μ A/0.6mA
	Data Outputs	150/40	3.0mA/24mA
PE	Parallel Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
U/ $\bar{D}$	Up/Down count control input	1.0/1.0	20 μ A/0.6mA
MR	Master Reset input (active Low)	1.0/1.0	20 μ A/0.6mA
SR	Synchronous Reset input (active Low)	1.0/1.0	20 μ A/0.6mA
CEP	Count Enable Parallel input (active Low)	1.0/1.0	20 μ A/0.6mA
CET	Count Enable Trickle input (active Low)	1.0/1.0	20 μ A/0.6mA
CS	Chip Select input (active Low)	1.0/1.0	20 μ A/0.6mA
OE	Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
CP	Clock input (active Rising Edge)	1.0/1.0	20 μ A/0.6mA
TC	Terminal Count Output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

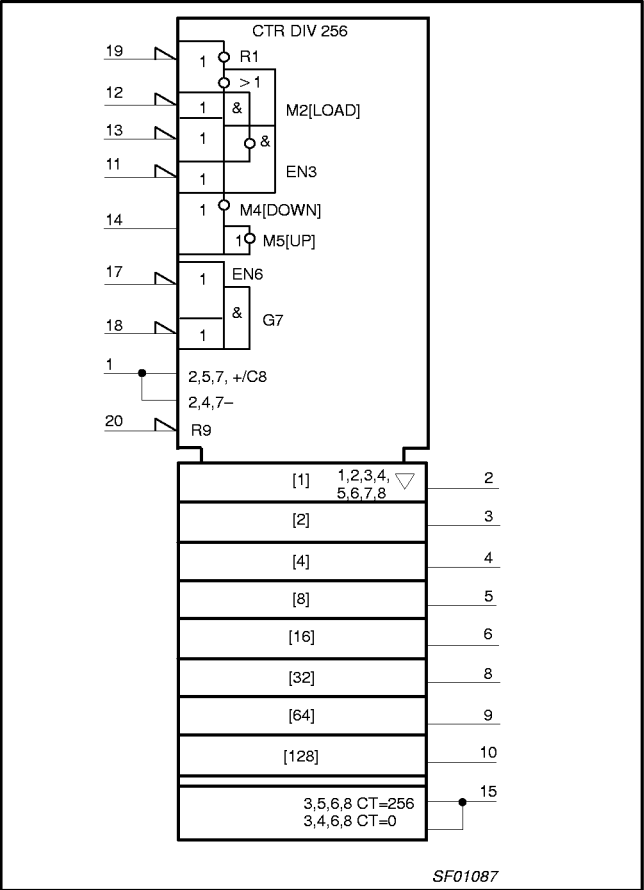
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

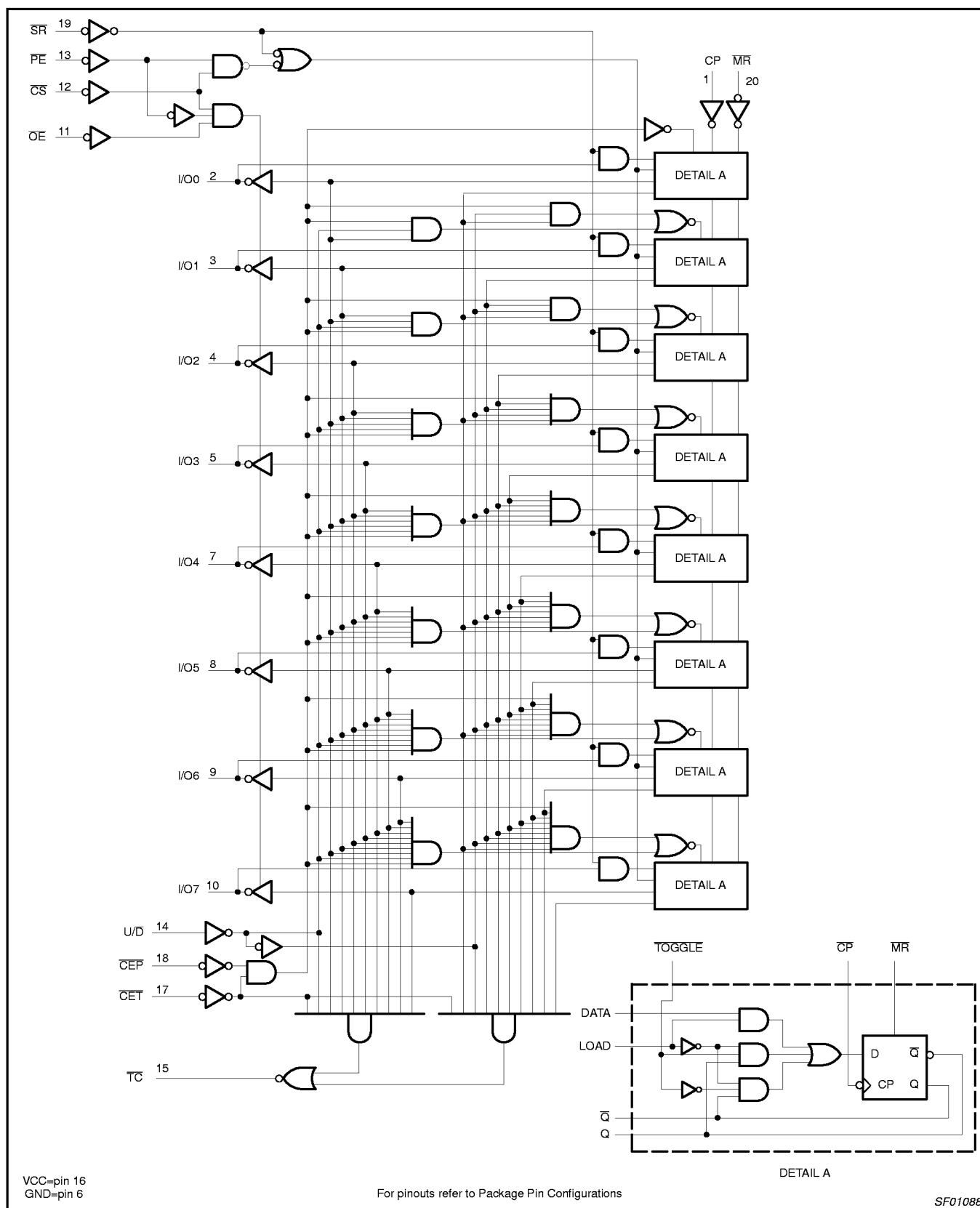
INPUTS									OPERATING MODE
MR	SR	CS	PE	CEP	CET	U/D	OE	CP	
X	X	H	X	X	X	X	X	X	I/O0 to I/O7 in high impedance (PE disabled)
X	X	L	H	X	X	X	H	X	I/O0 to I/O7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/On lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold (TC held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = CS and PE should never be Low voltage level at the same time.

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LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_O	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	TC	40	mA
		I/O0	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	TC		-1	mA
		I/O _n		-3	mA
I_{OL}	Low-level output current	TC		20	mA
		I/O _n		24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	T _C	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN (V _{IL} = 0.0V, V _{IH} = 4.5V for MR, CP inputs)	I _{OH} = −1mA	±10%V _{CC}	2.5			V
					±5%V _{CC}	2.7	3.4		V
		I/O _n		I _{OH} = −3mA	±10%V _{CC}	2.4	3.3		V
					±5%V _{CC}	2.7	3.3		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX,	±10%V _{CC}		0.35	0.50	V
					±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				−0.73	−1.2	V
I _I	Input current at maximum input voltage	I/O _n	V _{CC} = MAX, V _I = 5.5V					1	mA
		others	V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current	except I/O _n	V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					−0.6	mA
I _{OZH} + I _{IH}	Off-state output current High-level voltage applied	I/O _n	V _{CC} = MAX, V _O = 2.7V					70	μA
I _{OZL} + I _{IL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V					−600	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX			−60		−150	mA
I _{CC}	Supply current (total)	I _{CC} H	V _{CC} = MAX				95	135	mA
		I _{CC} L					105	145	mA
		I _{CC} Z					105	150	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}, R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns ns
t_{PHL}	Propagation delay MR to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$	Waveform 4	4.0 6.0	6.5 8.0	9.0 10.5	4.0 6.0	10.5 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns ns
t_{PZH} t_{PZL}	Output Enable time PE to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time PE to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns ns
t_{PZH} t_{PZL}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns ns

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AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low I/O _n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low I/O _n to CP	Waveform 5	0 0			0 0		ns ns
t _s (H) t _s (L)	Setup time, High or Low U/D to CP	Waveform 5	8.0 8.0			9.0 9.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low U/D to CP	Waveform 5	0 0			0 0		ns ns
t _s (H) t _s (L)	Setup time, High or Low PE, SR or CS to CP	Waveform 5	9.5 9.5			10.0 10.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low PE, SR or CS to CP	Waveform 5	0 0			0 0		ns ns
t _s (H) t _s (L)	Setup time, High or Low CEP or CET to CP	Waveform 5	5.0 9.0			5.5 10.5		ns ns
t _h (H) t _h (L)	Hold time, High or Low CEP or CET to CP	Waveform 5	0 0			0 0		ns ns
t _w (H) t _w (L)	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns ns
t _w (L)	MR Pulse width, Low	Waveform 2	3.0			3.0		ns
t _{rec}	Recovery time, MR to CP	Waveform 2	4.0			4.5		ns

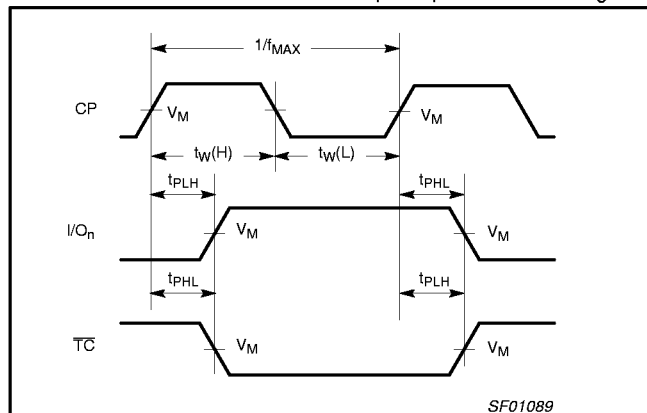
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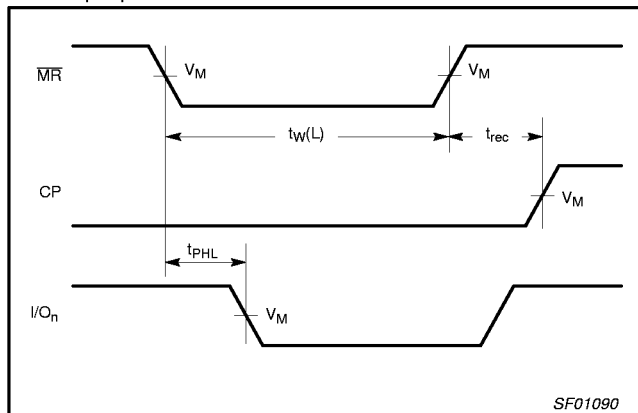
AC WAVEFORMS

NOTE: For all waveforms $V_M = 1.5V$.

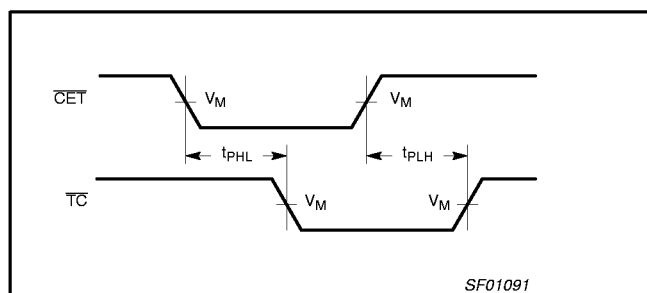
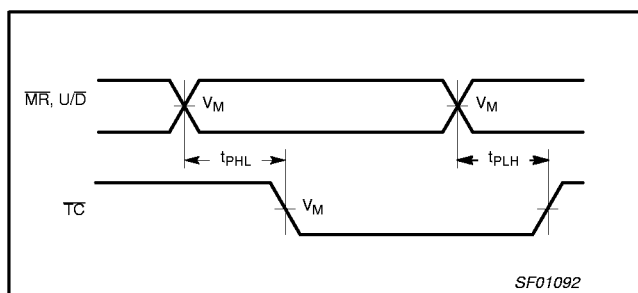
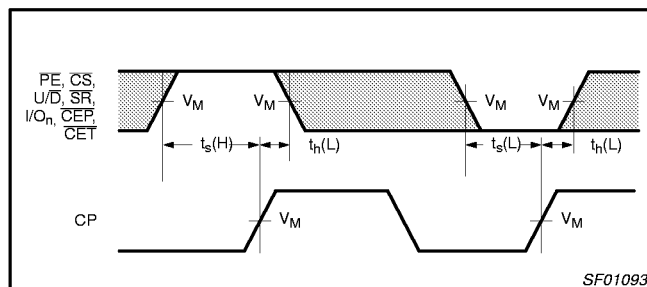
The shaded areas indicate when the input is permitted to change for predictable output performance.



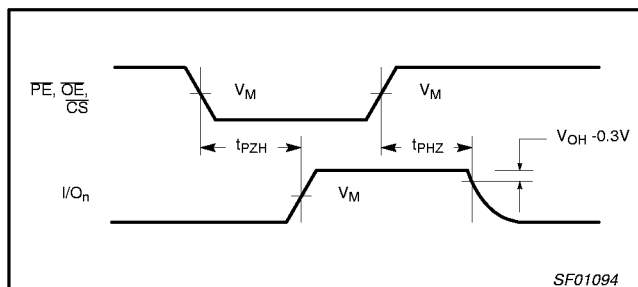
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



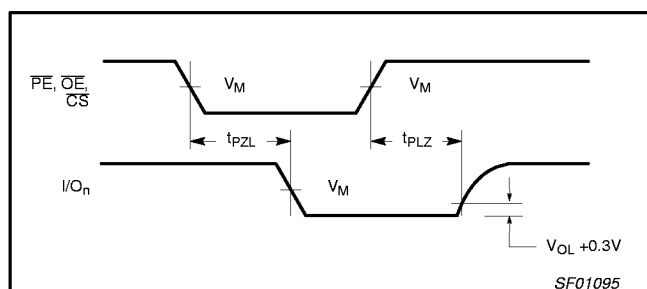
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

Waveform 3. Propagation Delay, $\overline{C}_{ET}$ Input to Terminal Count OutputWaveform 4. Propagation Delay, $U/\overline{D}$ and $\overline{MR}$ Inputs to Terminal Count Output

Waveform 5. Setup and Hold Times



Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

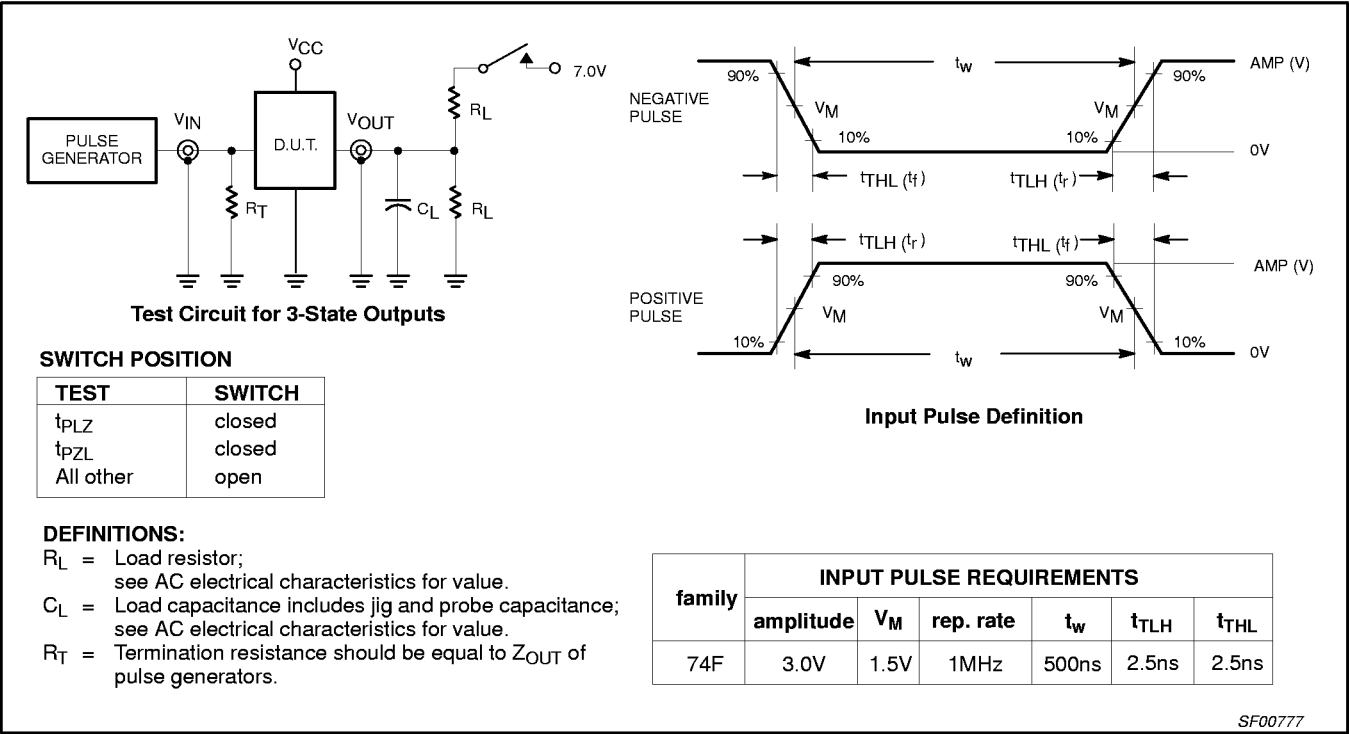


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS



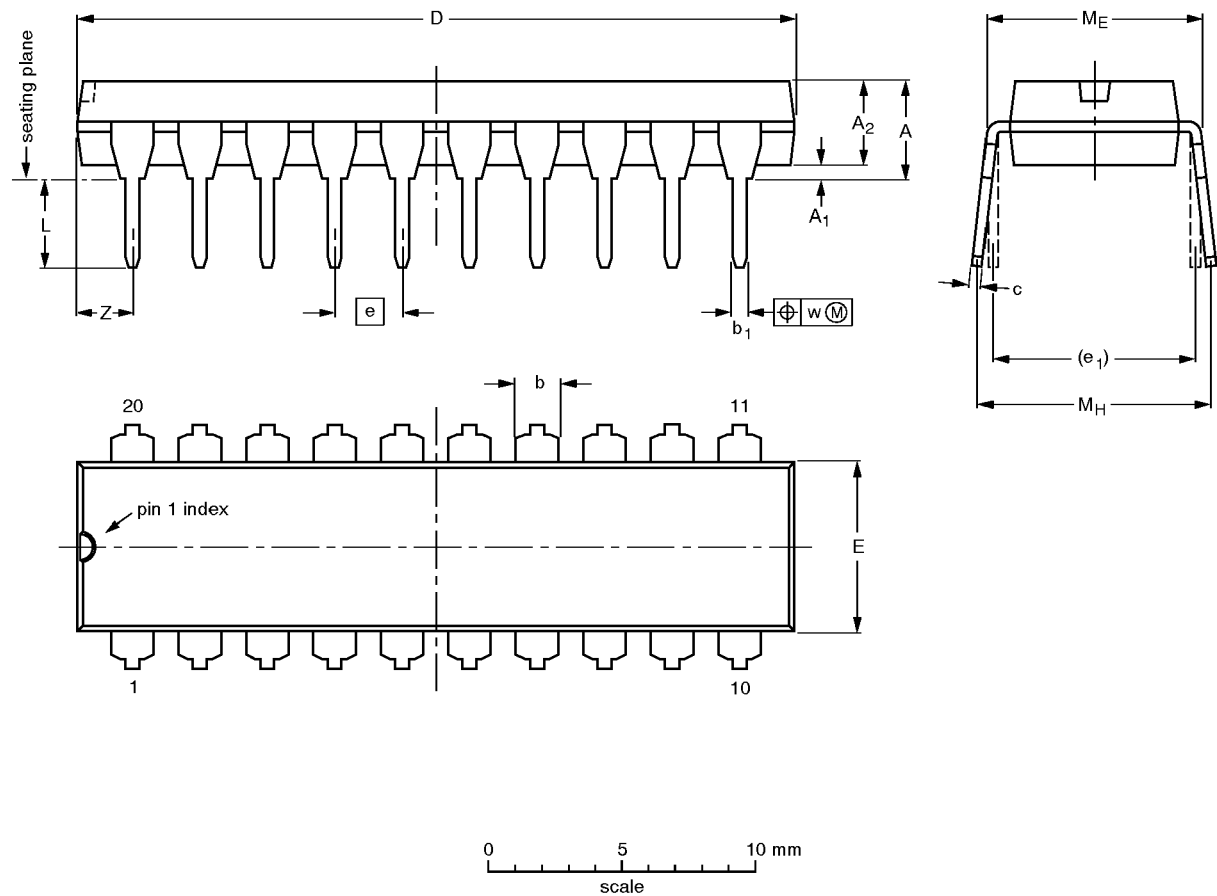
SF00777

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

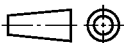


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

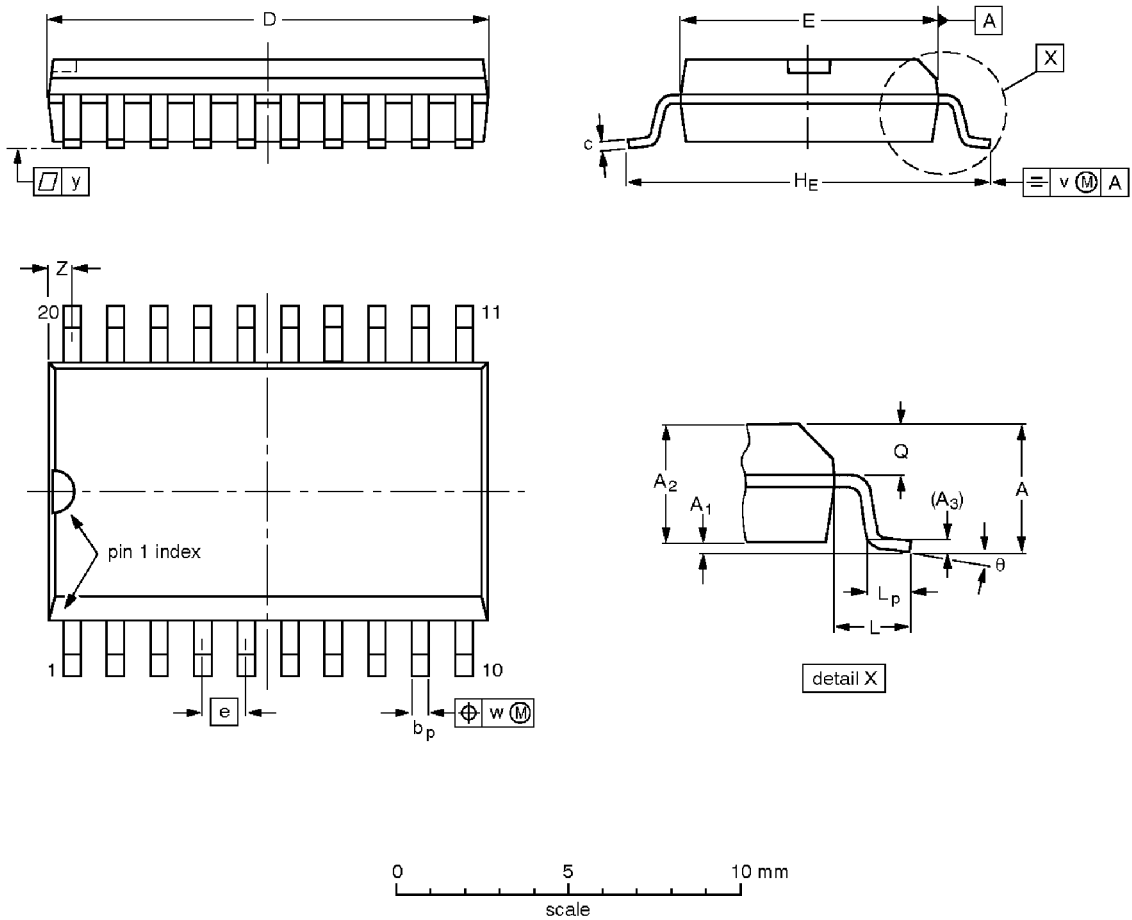
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

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