



SR D02

Ultra Low Noise Phase locked 500 MHz SAW Oscillator
Preliminary specification (Rev.A1)

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Features

- Phase locked SAW Oscillator
- Nominal Frequency: 500 MHz
- Ultra low phase noise: - 165 dBc/Hz @ 10 kHz offset (Typical)
- 181 dBc/Hz noise floor (Typical)
- External reference: 10 MHz Ultra Stable Crystal Oscillator
- Digital phase lock loop
- Automatic frequency calibration at warm-up time
- Airborne environment (suspended oscillator core)
- Shielded package 70 x 70 x 35 mm
- SMA connectors for Frequency Output and Reference Input
- Solder pins (Feedthru filters) for DC power supply & status

Environmental conditions

Parameters	Unit	Minimum	Typical	Maximum
Operating temperature range	°C	- 40		+ 70
Storage temperature range	°C	- 40		+ 85
Random vibration	g ² /Hz [BW Hz]	0.02 [10-1000] 0.005 [1000-2000]		
Mechanical shock	-	Half sine 30 g 11 ms		
Humidity	-	As per MIL-STD- 810F Method 507.4 (93% RH at 60°C)		
Low pressure & temperature	-	120 hPa within [-40, +55 °C]		
Constant acceleration	-	18 g all directions		

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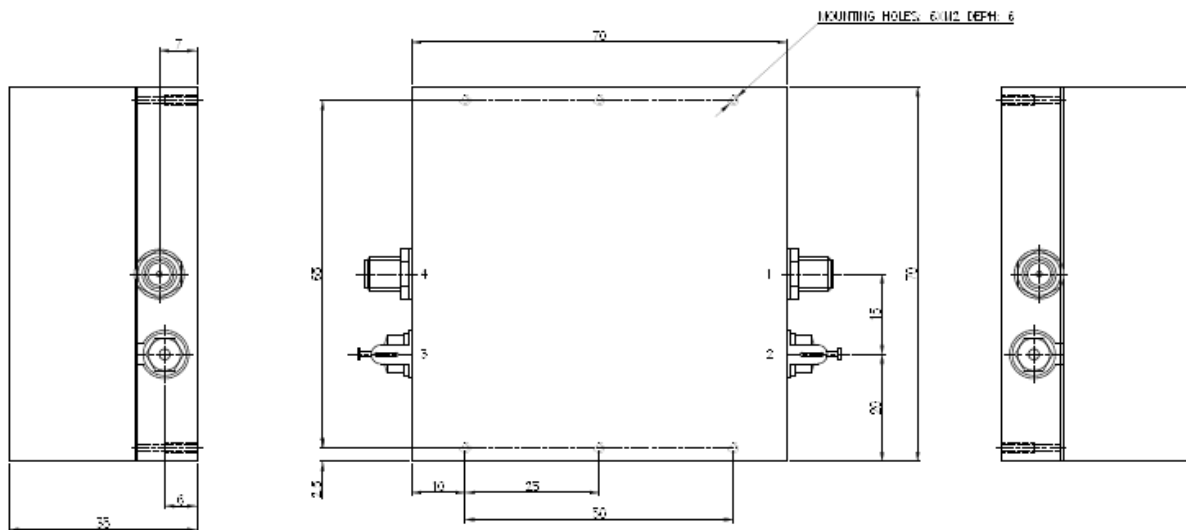
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Mechanical characteristics

Package:

- Machined, shielded enclosure
- SMA connector & Feedthru solder pins
- Case: AG4,5MC
- Finish: Ni15(I)/Zn1(II)/AG4,5MC



Foot-print:

- 70 x 70 mm typical
- ± 0.2 mm

Height:

- 35 mm typical
- ± 0.2 mm

Pin description

Pin number	Type	Label	Function
1	Female SMA	Frequency output	500 MHz
2	Feedthru + Ground	DC Supply voltage	Oscillator & oven power supply
3	Feedthru + Ground	Status	Ready or Alarm
4	Female SMA	Reference input	10 MHz

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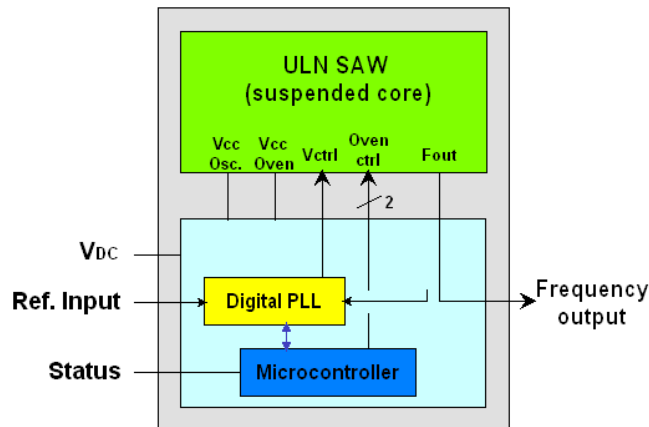
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Technical Characteristics

Block diagram



Electrical specifications

Electrical Parameters	Unit	Minimum	Typical	Maximum
Frequency output (SMA Connector)				
Nominal frequency	MHz		500	
Relative frequency stability	ppm	As reference input		
Warm up time (phase locked)	mn		2	5
Output level (50 Ω load)	dBm	11.5	12.5	13.5
Harmonics suppression	dBc	30		
Phase noise @ 1 kHz offset (static)	dBc/Hz	- 141	- 137	- 134
Phase noise @ 2 kHz offset	dBc/Hz	- 150	- 146	- 143
Phase noise @ 10 kHz offset	dBc/Hz	- 168	- 165	- 162
Phase noise @ 100 kHz offset	dBc/Hz	< - 180	- 180	- 175
Phase noise floor (see note here after)	dBc/Hz	< - 180	< - 180	- 175
VSWR	-			2:1
Reference input (SMA Connector)				
Nominal frequency	MHz		10	
Relative frequency stability (all causes)	ppm			± 0.3
Input level (50 Ω load)	dBm	10	13	
Harmonics suppression	dBc	30		
DC Supply voltage (V_{DC} pin)				
Voltage range	V _{DC}	11.75	12	12.25
Supply current	mA		300 @ + 25°C	750
Ripple (DC to 5 MHz)	mVpp			10
Status (Status pin)				
Interface	-	Open drain (external pull resistor to 3.3 V)		
Logic 1	-	Oscillator ready		
Logic 0	-	Alarm (Warm up or failure)		

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Note on the measurement of SR D02 phase noise:

- SR D02 features a phase noise floor which is better than the noise floor of current test setups as shown below with e. g. the PN9000 setup of Aeroflex: noise floor measurement is limited around -175 dBc/Hz by the noise floor of the test setup,
- Multi-channel measurement and cross correlation technique improve the noise floor of the test setup as e. g. with the new DCNTS (Dual Core Noise Test System) of Aeroflex: residual noise floor is better than -190 dBc/Hz
- With this later setup, SR D02 noise floor is measured at -182 dBc/Hz!

