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SSI 34P3500

PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

Advance Information

December 1995

DESCRIPTION

The SSI 34P3500 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 24 to 80 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8, 9 GCR ENDEC, data synchronizer, time base generator, and FWR servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V power supply.

The SSI 34P3500 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 24 to 80 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Three tap transversal filter for adaptive PR4 equalization**
- **8/9 GCR ENDEC**
- **Data Scrambler/Descrambler**
- **Programmable write precompensation**
- **Low operating power (0.75W typical at 5V)**
- **Register programmable power management**
- **Register programmable WG polarity**
- **Dual-bit and byte wide bi-directional NRZ data interfaces**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5V ± 10%)**
- **Small footprint 100-pin TQFP package**
- **Presettable Precoder state**
- **AGC Charge Pump held during Write Mode**
- **Dual Sync Byte Detection**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, analog during acquisition, sampled during read data**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents during read data**
- **Charge pump currents track programmable data rate**
- **Low drift AGC hold circuitry**
- **Low Z input switch**
- **AGC hold, fast recovery, and AGC input impedance control signals**
- **Wide bandwidth, precision full-wave rectifier**

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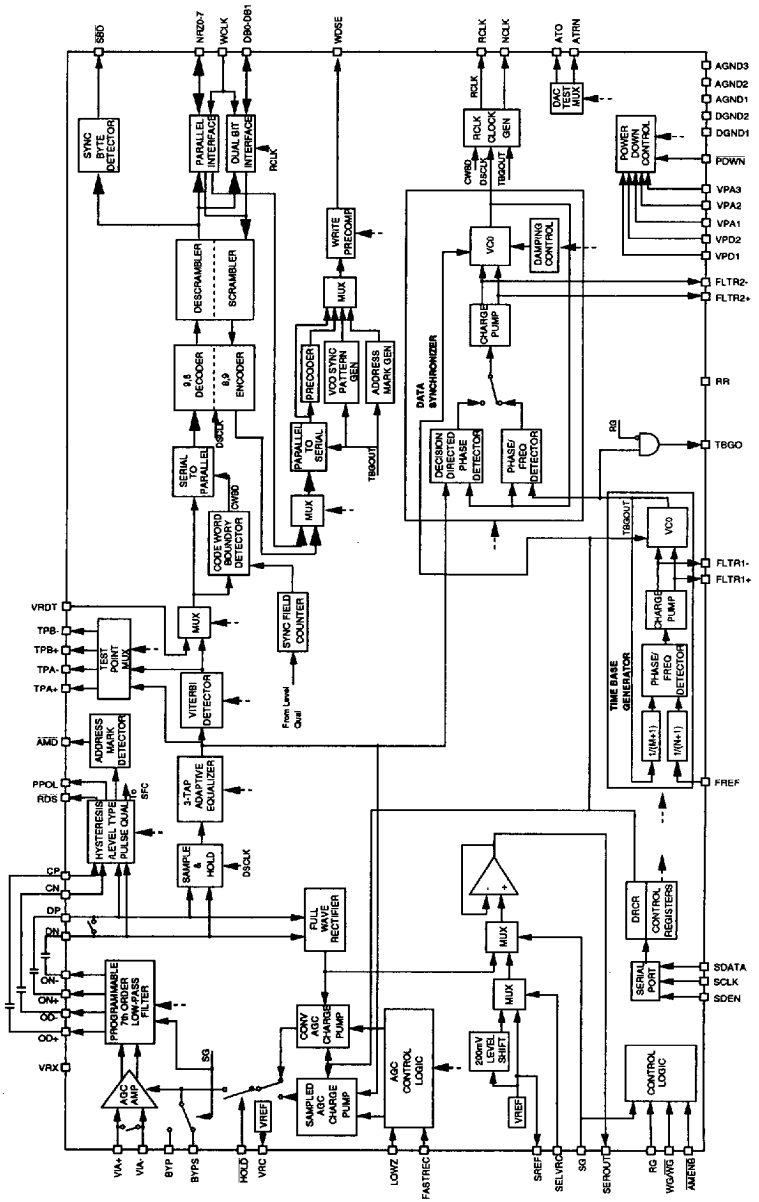
BLOCK DIAGRAM



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FEATURES (continued)

FILTER / EQUALIZER

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 3 to 24 MHz
  - Programmable boost /equalization of 0 to 13 dB
  - ±0.6 ns group delay variation from 0.2 fc to fc, with fc = 24 MHz
  - Minimizes size and power
  - Low Z input switch
- Three tap self adapting transversal filter for fine equalization to PR4
- No external components required

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register selection between dual level pulse qualifier or hysteresis qualifier for servo reads

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 90 MHz frequency output
- Independent M and N divide-by registers
- No active external components required
- TBGO: TTL level Time Base Generator Output

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 80 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive (+) and (-) clock recovery thresholds for use with asymmetrical amplitude signals (e.g., from MR heads)
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Dual-bit and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- TTL level write data output
- Integrated sync byte detection
- Hard and soft sector operation

SERVO

- Wide bandwidth, precision full-wave rectifier
- Buffered FWR analog servo output with selectable reference voltage
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Compatible with SSI 32H6521 Embedded Servo Controller

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FUNCTIONAL DESCRIPTION

The SSI 34P3500 implements a complete high performance PR4 read channel, including an AGC, programmable filter / equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 8,9 ENDEC and scrambler/descrambler, and FWR servo, that supports data rates up to 80 Mbit/s.

A serial port is provided to write control data to the 16 internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input of the pulse detector while the input to the amplifier varies. The circuit consists of a loop that includes the AGC amplifier and charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. Depending on whether the read is of servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to noise.

During servo reads the loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (C_{BYPS}). The dual rate charge pump drives C_{BYPS} with currents that drive the differential voltage at DP/DN to 1.4 Vp-pd. Attack currents lower the V_{BYPS} which reduces the amplifier gain. The dual rate attack charge pump is included for fast transient recovery. The normal AGC attack current in servo mode is 150 µA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 8. The nominal decay current is 8.3 µA, and increases by a factor of 8 when the FASTREC input is high. In this mode, transients that produce low gain will recover more rapidly with the Fast Decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode.

For data reads, the loop described above is used during address mark detection and until the data synchronizer is locked to the incoming VCO preamble, except that to optimize recovery for constant density recording, both of the AGC charge pumps' currents track the data rate value loaded in the Data Rate Register and that the BYP hold capacitor (C_{BYP}) is now used. In addition, at the maximum data rate, the nominal AGC attack current is 403 µA and the nominal decay current is 22.4 µA. The fast attack and fast decay current factors are the same as in servo mode. After this point, the loop is switched to include the AGC amplifier with a sampled dual rate charge pump, the programmable continuous time filter, full wave rectifier, and the sampling 3-tap adaptive equalizer to more accurately control the signal amplitude into the Viterbi qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled and held and compared to a threshold to generate the error current. The maximum charge pump current value can be programmed from the Sample Loop Control Register to 0, 20, 40, or 60 µA.

The gain of the AGC amplifier is 38 dB/V typical.

For maximum application flexibility, all AGC mode control inputs are designed to be externally controlled. When the LOWZ input is high, Low-Z mode is activated. In the Low-Z mode, the AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. This mode should be activated during and for a short time after a write operation.

When either the $\overline{\text{HOLD}}$ input is active low or WG is active high, the dual rate charge pumps are disabled. This de-activates the AGC loop. The AGC amplifier gain will be held constant at a level set by the voltage at the BYP or BYPS pins.

In most applications, the BYP and BYPS pin voltages are stored on external capacitors. In applications where AGC action is not desired, the BYP and BYPS voltages can be set by resistor divider networks connected from VPA to VRC. If programmable gain is desired, the resistor network could be driven by a current DAC.

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PULSE QUALIFICATION CIRCUIT DESCRIPTIONS

This device utilizes three different types of pulse qualification, two primarily for servo reads and the other for data reads.

Servo Qualifiers (Dual Level/Window & Hysteresis)

During servo reads (SG high) and when bit 6 of the Control Operating Register is set to 1, a dual level/ window type of pulse qualifier is used. The level qualification thresholds are set by a 7-bit DAC which is controlled by the Servo Level Threshold Register. The register value is relative to the peak voltage at the output of the continuous time filter, and the DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT Register does not affect this DAC's reference. The $\overline{RDS}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity as the pulse, respectively.

When bit 6 of the Control Operating Register is set to 0, a hysteresis type of pulse qualifier is used. The $\overline{RDS}$ output will recognize only alternating polarity qualified pulses. If a pulse exceeds the threshold and is of the same polarity of the previous qualified pulse, then it is ignored.

In data read mode (RG high), the same dual level/ window qualifier as was used for servo reads, is used for Address Mark Detection and for ensuring pulse polarity changes during VCO sync field counting. It's qualification thresholds are set by a 7-bit DAC which is controlled by or the Data Level Threshold Register. The register value is relative to the peak voltage at output of the continuous time filter and the DAC is referenced to an fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the WP/LT Register does not affect the DAC's reference until the sync field count has been achieved. The $\overline{RDS}$ and the PPOL outputs of the level qualifier are not active in data read mode.

Viterbi Qualifier

The second type of pulse qualification, the Viterbi qualifier, is only used during data read mode after the sync field count has been achieved. The Viterbi qualifier has two significant blocks, one that feeds the other. The first block is the sampled pulse detector and the second is the survival sequence register.

The sampled pulse detector performs the pulse acquisition/detection in the sampled domain. It acquires pulses by comparing the code clock sampled level of the analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The Viterbi threshold window is defined to be the difference between the positive and negative threshold levels. The threshold window, Vth, is set by a 7-bit DAC which is controlled by the Viterbi Detector Control Register. While the window size is fixed by the programmed Vth value, the actual positive and negative thresholds track the most positive and the most negative samples of the equalized input signal. For example, the Viterbi positive signal threshold, Vpt = Vpeak (+) max if the previous detected level was (+). If the previous detect level was (-), Vpt = Vpeak(-)max + Vth, where Vpeak(-)max is the maximum amplitude of the previously detected negative signal. Normally Vth is set to equal Vpeak (approx. 500 mV).

After the pulses have been detected they must be further qualified by the survival sequence registers and associated logic. This logic guarantees that for sequential pulses of the same polarity within the maximum run length, only the latest is qualified. By definition, this is the pulse of greatest amplitude.

The Viterbi qualifier is implemented as two parallel qualifiers that operate on interleaved samples. Each qualifier has a survival sequence register length of 5.

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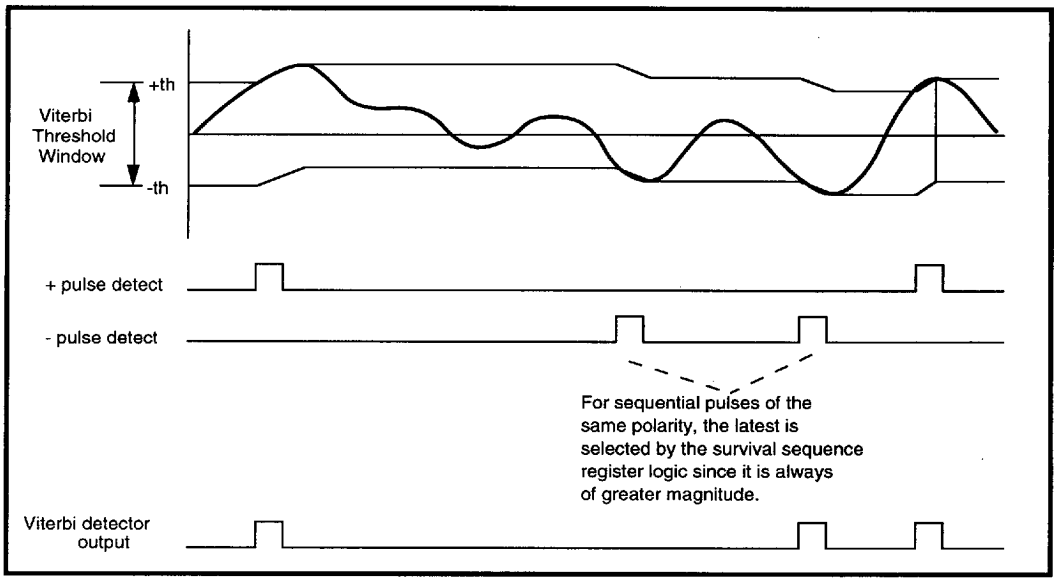

FIGURE 1: Viterbi Detector

FUNCTIONAL DESCRIPTION (continued)

Programmable Filter Circuit Description

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to 1.75 times the cutoff frequency. For pulse slimming two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. Both the boost and the filter cutoff frequency are programmed through internal 7-bit DACs, accessed via the serial port logic. The nominal boost range at the cutoff frequency is 0 to 12.75 dB at maximum fc and is controlled by the Data Boost Register or the Servo Boost Register in the servo mode. The cutoff frequency, Fc is variable from 3 to 24 MHz and controlled by the Data Cutoff Register or Servo Cutoff Register in the servo mode. The cutoff and boost values for servo reads are automatically switched when servo mode is entered.

The current reference for the filter DACs is set using a single 12.1 kΩ resistor, from the VRX pin to ground. The voltage at VRX is proportional-to-absolute temperature (PTAT).

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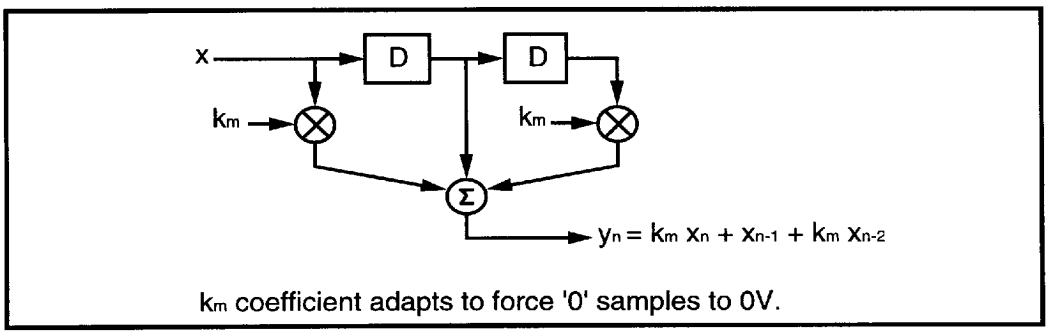

FIGURE 2: 3-Tap Adaptive Equalizer Circuit

ADAPTIVE EQUALIZER CIRCUIT DESCRIPTION

Up to 7 dB of cosine equalization for fine shaping of the incoming read signal to the PR4 wave shape is provided by a 3 tap, sampled analog, transversal filter with an adaptive multiplier coefficient. The same multiplier coefficient (k_m) is used for both of the outside taps. The value of k_m is adjusted to force "zero" samples to zero volts. A special equalizer training pattern, located after the VCO sync field in the sector format, is used to provide an optimum signal for the equalizer to adapt to. The adaptive property of the equalizer is enabled or disabled by the AEE bit in the Sample Loop Register. If the adaptive property is enabled, whether adaptation occurs only during the training pattern or both during the training pattern and the user data is controlled by the AED bit in the Sample Loop Register.

Time Base Generator Circuit Description

The time base generator (TBG) is a PLL based circuit, that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N and DR Registers. The TBG output frequency, Fout, should be programmed as close as possible to ((9/8) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of common mode noise. An applications note is published in the 32P4741/42/44/46 Single-Chip Read Channel Device Applications Notes section of the SSI Data Book that gives information on how to program and optimize the time base generator.

In servo read, write and idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. The TBG output is brought out at the TBGO pin. Also in the write and idle modes, the Time Base Generator output, when selected by the Control Test Mode Register, can be monitored at the TPA+ and TPA- test pins. In the read mode, the TBG output should not be selected for output on the test pins so that the possibility of jitter in the data separator PLL is minimized.

The TBGO output is disabled by RG being active high.

The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$F_{TBG} = FREF \bullet [(M + 1) \div (N + 1)]$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center

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FUNCTIONAL DESCRIPTION (continued)

frequency. The time base generator PLL responds to any changes to the M and N registers, only after the DR register is updated.

The DR register value, directly affects the following:
- center frequency of the time base generator VCO,
- center frequency of the data separator VCO,
- phase detector gain of the time base generator phase detector,
- phase detector gain of the data separator phase detector,
- write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the ground and RR pins.

$$RR = 12.1\ k\Omega$$

DATA SEPARATOR CIRCUIT DESCRIPTION

The Data Separator circuit provides complete encoding, decoding, and synchronization for 8,9 (0,4,4) GCR data. In data read mode, the circuit performs address mark detect, clock recovery, code word synchronization, decoding, sync byte detection, descrambling, and NRZ interface conversion. In the write mode, the circuit generates address marks, generates the VCO sync field, scrambles and converts the NRZ data into 8,9 (0,4,4) GCR format, precodes the data, and performs write precompensation.

The circuit consists of five major functional blocks; the data synchronizer, 8,9 ENDEC, NRZ scrambler/descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to recover the code rate clock from the incoming read data. To achieve fast acquisition, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the read mode and phase-frequency detector is used in the idle, servo, and write modes.

In the read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent "one" samples or comparing the "zero" sample magnitude to ground for the entire sample period. A special (non IBM) algorithm is used to prevent "hang up" during the acquisition phase. The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, dual mode, threshold comparator. This comparator's threshold levels are determined by the value, Lth, programmed in the Data Threshold Register. The fixed level threshold before the sync field count (SFC) has been achieved will be 1.4 times the threshold level after SFC since this is the ratio of the peak signal to the sampled "1" signal amplitude for PR4. The dual mode nature of this comparator allows the selection of either symmetric fixed or independent self adapting (+) and (-) thresholds by programming the adaptive level enable (ALE) bit in the WP/LT Register.

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When adaptive mode is selected, the fixed thresholds are used until the sync field count (SFC)

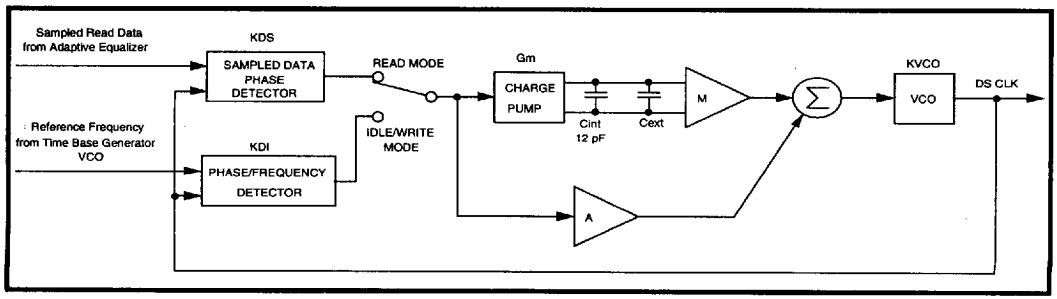

FIGURE 3: Data Synchronizer Phase Locked Loop

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has been reached, then the adaptive levels are internally enabled. The time constant of a single pole filter that controls the rate of adaptation, is programmable by bits TC3-1 in the WP/LT Register.

In the write and idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, F_{TBG}. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

The two phase detectors' outputs are muxed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6-0 in the Damping Ratio Control Register. The programmed damping ratio is independent of data rate. The decision directed phase detector goes through a gain reduction of 6 or 10 (based on the value of the serial port GS_10 bit and enabled by GS bit) at sync field count.

In write mode, the TBG output is used to clock the encoder, precoder, and write precompensation circuits.

ENDEC

The ENDEC implements an 8,9 (0,4,4) Group Coded Recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of four zeros between ones for the interleaved samples. During write operations the encoder portion of the ENDEC converts 8 bit parallel, scrambled or nonscrambled, data to 9 bit parallel code words that are then converted to serial format. In data read operation, after the code word boundary has been detected in the Viterbi qualified serial data stream, the data is converted to 9 bit parallel form and the decoder portion of the ENDEC converts the 9 bit code words to 8 bit NRZ format.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled by bit 2 of the Control Operating Register. In write mode, if enabled, the circuit scrambles the 8 bit internal NRZ data before passing it to the encoder. Only user data, i.e., the NRZ data following the sync bytes, is scrambled. In data read mode, only the decoded NRZ data after the sync bytes is descrambled. The scrambler polynomial is $H(X) = 1 \oplus X7 \oplus X10$.

Write Precoder

The 32P3500 implements a write precoder which is used to precode the serialized encoder data for PR4. The state of the precoder is preset to 0,0 upon exiting write mode. This guarantees that the precoder will begin the next write in the 0,0 state. The state of the precoder is presetable to be in a known state when the write data changes from sync field to encoded data. This is done via the power down register bits 4 and 5. Bit 4 = 0 enables the precoder, and bit 5 = 1 sets the precoder in the "1" state. Setting bit 5 = 0 sets the precoder in the "0" state. All four of these patterns will decode properly upon read back. The precoder operation consists of the current encoded data being XOR'ed to the write data information one code period back. The current write data information is the current output of the precoder XOR.

NRZ Interface

The NRZ interface circuit provides the ability to interface with a byte wide controller. The NRZ interface type is specified by the programming of bit 4 of the Control Operating Register. If byte wide mode is selected, the circuit does not reformat the data before passing it to and from the internal 8 bit bus. If dual bit mode is selected, the NRZ interface circuit converts the external dual bit bus to the internal 8-bit bus. Only the selected NRZ interface is enabled and the other can be left floating. Both the byte wide and dual bit interfaces define the most significant bit of the interface as the most significant bit of the data and the dual bit interface defines the first pair clocked in or out as the most significant pair.

For both byte wide and dual bit operation, the NRZ write data is latched by the 34P3500 on the rising edge of the WCLK input. The WCLK frequency must be appropriate for the data rate chosen or else overflow/underflow will occur. It is recommended that WCLK be connected to RCLK to prevent this from occurring.

In data read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the second sync byte (69H). The NRZ interface is at a high impedance state when not in data read mode.

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FUNCTIONAL DESCRIPTION (continued)

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effect. The magnitude of the time shift, WPC, is programmable via the Write Precomp Register and is made proportional to the time base generator's VCO period (i.e., data rate). The circuit performs write precompensation only on the second of two consecutive "ones" and only shifts in the late direction. If more than two consecutive "ones" are written, all but the first are precompensated in the late direction. This appears as a delay of the rising edge of WDSE.

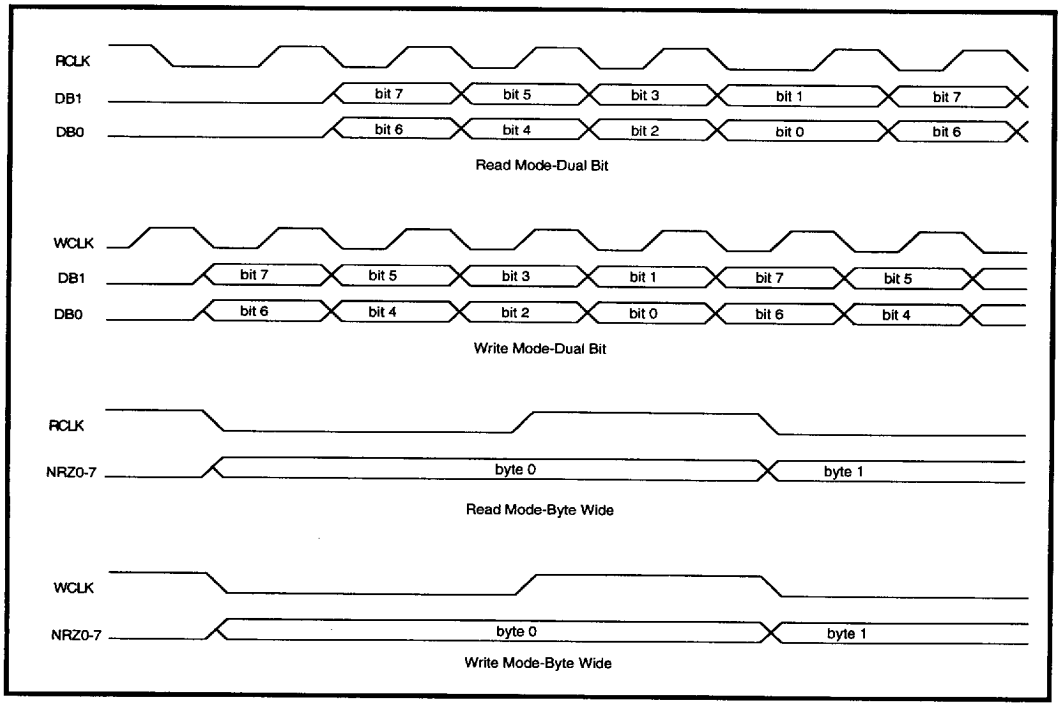

FIGURE 4: RCLK, WCLK vs. NRZ Data

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SERVO CIRCUIT DESCRIPTION

Embedded servo capture is provided with a buffered full-wave rectified (FWR) output. The differential signal across the DP/DN inputs is applied to a full-wave rectifier. The output signal of the rectifier is the rectified servo burst signal, level-shifted above SREF (which is a bandgap reference from VPA). The output at the SEROUT pin is selectable between the FWR output and two references, SREF and SREF + 200 mV. When the SG is high (active) the FWR output is selected for the SEROUT pin. When SG is low (i.e., during the data field) then the SEROUT pin is selected between SREF and SREF + 200 mV, depending on the input at SELVRC.

The dual level pulse qualifier outputs $\overline{\text{RDS}}$ and PPOL are enabled when the servo gate input (SG) goes high and provide the indication of a qualified servo pulse and the polarity of the pulse, respectively.

SG	SELVRC	SEROUT
1	1	FWR Output
1	0	FWR Output
0	1	SREF
0	0	SREF + 200 mV

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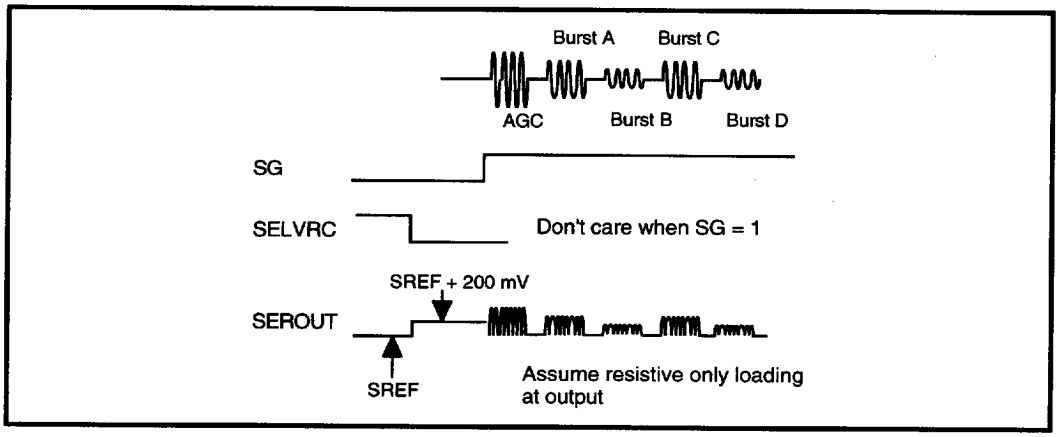

FIGURE 5: Servo Function Diagram

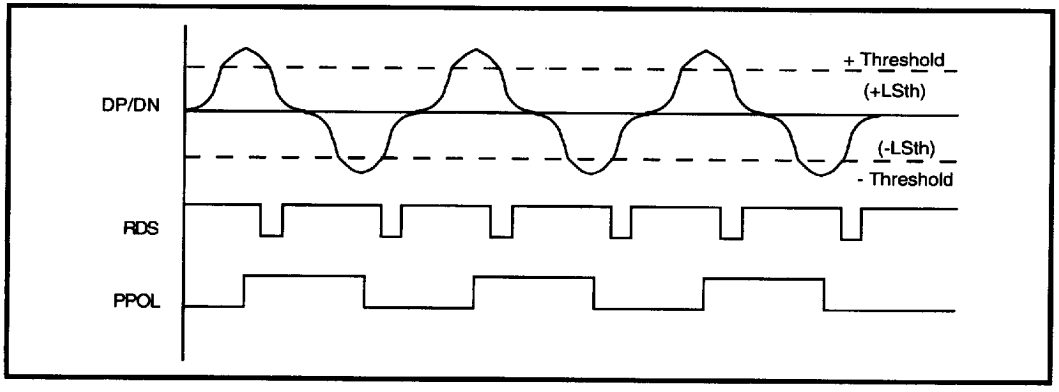

FIGURE 6: $\overline{\text{RDS}}$ and PPOL vs. DP/DN Relationship

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FUNCTIONAL DESCRIPTION (continued)

SERIAL PORT CIRCUIT DESCRIPTION

The serial port interface is used to program the 34P3500's sixteen internal registers. The serial port is enabled for data transfer when the Serial Data Enable (SDEN) pin is high ("1"). SDEN must be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SDEN should be brought low ("0").

When SDEN is high, the data presented to the Serial Data (SDATA) pin will be latched into the 34P3500 on each rising edge of the Serial Clock (SCLK). Rising edges of SCLK should only occur when the desired bit of address or data is being presented on the serial data line. Serial data transmissions must occur in 16-bit packets. If more than 16 rising edges of SCLK are received during the time that SDEN is high, the additional SCLK and SDATA information will be ignored. During a serial data transmission, if SDEN is switched low before 16 SCLK pulses are received, that serial transmission will be aborted. For all valid transmissions, the data is latched into the internal register on the falling edge of SDEN.

Each 16 bit transmission consists of a R/$\overline{W}$ bit (R/$\overline{W}$ ="0") followed by 3 device select bits, 4 address bits and 8 data bits. The address bits select the internal register to be written to. The device select, address and data fields are input LSB first, MSB last, where LSB is defined as Bit 0. The three device select bits select the device on the SSI serial bus to be communicated with and must set S0 = 0, S1 = 1, and S2 = 0 when communicating with the 34P3500. Figure 7 shows the serial interface timing diagram.

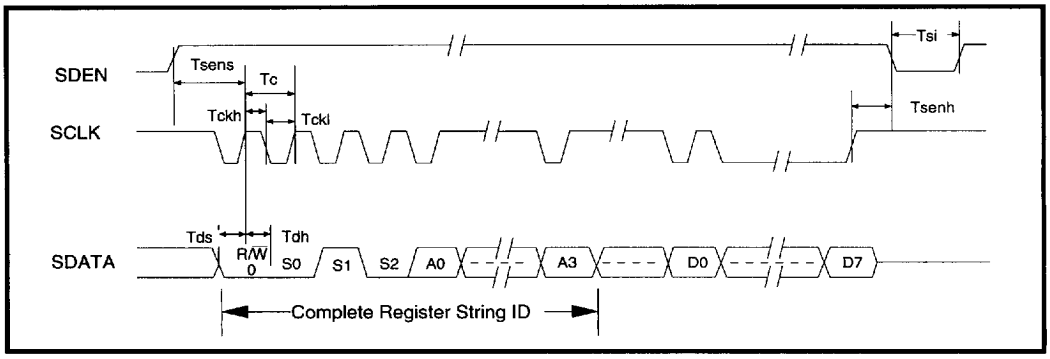

FIGURE 7: Serial Interface Timing

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FUNCTIONAL DESCRIPTION (continued)

DESCRIPTION OF OPERATING MODES

The fundamental operating modes of the 34P3500 are controlled by the SERVO GATE (SG), READ GATE (RG), and WRITE GATE (WG) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in the IDLE mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the media. WG is also an asynchronous input, but should not be terminated prior to the last output write data (WD) pulse.

IDLE MODE OPERATION

If SG, RG, and WG are not active, the 34P3500 is in idle mode. When in Idle mode, the Time Base Generator and the Data Separator PLL are running and the Data Separator PLL is phase-frequency locked to the TBG VCO output. The AGC, continuous time filter, and pulse qualifiers are active but the outputs of the pulse qualifiers are disabled. The continuous time filter is using its programmed values for cutoff frequency and boost determined by the data mode registers. The AGC operation is the same as in the VCO preamble portion of a data read.

SERVO MODE OPERATION

If SG is high, the device is in the servo mode. This mode is the same as idle except that the filter cutoff and boost settings are switched from those programmed for data read mode to those programmed for servo mode, the AGC is switched to servo mode, and the $\overline{RDS}$, PPOL, and SEROUT outputs are enabled. The assertion of SG causes read mode and write mode to be overridden.

WRITE MODE OPERATION

The 34P3500 supports two different write modes; normal write mode and direct write mode. The direct write mode requires that the direct write bit, bit 0 of the Control Operating Register, be active. Both write modes require that the data separator be powered on.

Normal Write Mode

The 34P3500 is in the normal write mode if WG/$\overline{WG}$ is active (register bit selectable whether active high or active low), $\overline{DWR}$ is high, and the direct write bit in the Control Operating Register is low. A minimum of one NRZ time period must elapse after RG goes low before WG/$\overline{WG}$ can be set active. The data separator PLL is phase-frequency locked to the TBG VCO output in this mode.

In normal write mode, the circuit first auto generates an address mark (soft sector only), then auto generates the VCO sync pattern, and finally scrambles the incoming NRZ data from the controller, encodes it into 8,9 GCR formatted data, precodes it, precompensates it, feeds it to write data, and outputs it to the preamp for storage on the disk. The circuit can operate in either soft or hard sector modes.

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Normal Write Mode - Soft Sector

In soft sector operation, when the write gate (WG/$\overline{WG}$) goes active, the NRZ inputs must be low and must be held low for the duration of the address mark and VCO sync field generation. The address mark enable ($\overline{AMENB}$) may be brought active (low) previous to the rising edge of WG (or falling $\overline{WG}$) to initiate the generation of the address mark sequence at the WD output. The address mark sequence will not begin until WG is brought high. The address mark sequence consists of four 8"0" gaps (=9T).

{(1,1,1,1,1,1,1,1,1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,1,1,1,1,1,1,1,1,1,-1,-1,-1,-1,-1,-1,-1,-1,-1) in the write current domain} $\overline{AMENB}$ should be held low for the completion of at least one 9T minimum and not more than three 9T times, then returned high.

Next, the circuit generates the VCO sync field (=2T) at the WD output.

{(1,1,-1,-1,1,1,-1,-1...) in the write current domain}

While the preamble is being written, WCLK must continue to clock in all "0" NRZ data. After the required sync field has been written (approx. 8 byte times, min.), the NRZ data must be changed to 93H for a minimum of 4 byte times to write the minimum 4 byte equalizer training pattern.The device will continue to autogenerate the sync field pattern until the first 93H is latched at the NRZ interface, and detected. The device encodes the 93H pattern and writes the result as the training sequence. Next, the NRZ data must be changed to 1FH for 1 byte time to write the sync byte #1. This is followed by another 93H and then 69H (sync byte #2). The user data must be presented at the NRZ interface immediately following the sync byte. Finally, after the last byte of user data has been clocked in, the WG/$\overline{WG}$ must remain active for a minimum of 34 NRZ bit times in byte-wide mode to ensure the that the device is flushed of data (The delay is 37 NRZ bit times in dual bit mode). WG/$\overline{WG}$ can then go inactive. WD stops outputting a maximum of 2 NRZ (RCLK) time periods after WG/$\overline{WG}$ goes inactive.

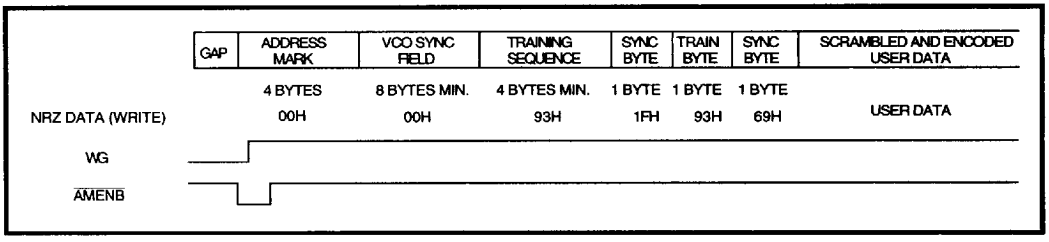

FIGURE 8: Soft Sector Write Sequence

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DESCRIPTION OF OPERATING MODES (continued)

Normal Write - Hard Sector

In hard sector operation, the circuit performs exactly the same as in soft sector except that the $\overline{\text{AMENB}}$ input pin will be held high so the address mark pattern is not generated.

Direct Write Mode

In direct write mode, the NRZ data from the byte-wide interface bypasses the scrambler, the 8,9 encoder and the precoder, but is precompensated before going to the WDSE output pin. The precomp should be set to zero in this mode. The purpose of routing the signal to the precomp circuit is to generate a return to zero pulse every time a "1" occurs in the data so that write data is pulsed. WCLK is required to clock the byte-wide NRZ data into the NRZ interface. Direct write mode is entered simply by setting the DW bit (bit 0) in the Control Operating Register. This mode is not valid when using the dual-bit NRZ interface.

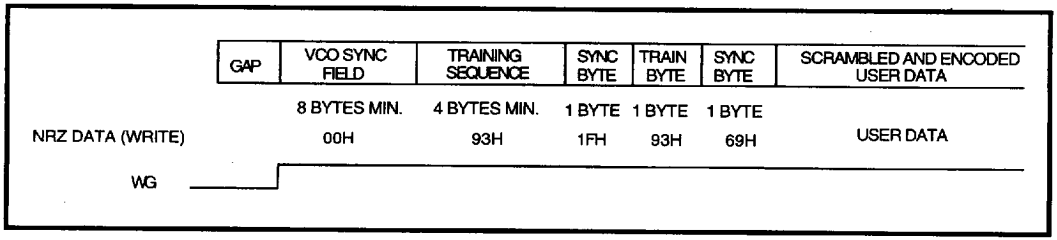

FIGURE 9: Hard Sector Write Sequence

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DATA READ MODE OPERATION

Data read mode is initiated by setting the Read Gate (RG) input pin high. This action causes the data synchronizer to begin acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when the Read Gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

SOFT SECTOR OPERATION

In soft sector read operation the circuit must first detect an address mark before initiating the rest of the read lock sequence.

Address Mark Detect

The address mark consists of four sets of 8"0" (=9T) patterns

{(1,0,0,0,0,0,0,0,0,-1,0,0,0,0,0,0,0,0,1,0,0,0,0,0,0,0,0, -1,0,0,0,0,0,0,0,0,1) in the read domain}.

This pattern was chosen because the interval between polarity changes of the read back pattern is 9 nominal clock periods, which is illegal in an 8,9 (0,4,4) code. The maximum zero read data pattern for a legal 8,9 (0,4,4) code word is 5 nominal clock periods between polarity changes. The read signal polarity changes are detected by the dual level pulse detector. Address mark detection is accomplished by counting the clocks (as "0's") between the polarity changes.

To begin the soft sector read sequence the Address Mark Enable ($\overline{AMENB}$) input pin must be asserted low. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the level qualified read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 7"0's" within the 8"0" patterns. Having detected a 7"0" the AMD then looks for two more 7"0" gaps. If the $\overline{AMD}$ does not detect 3 7"0" gaps within 38 code clock periods it will restart the address mark detect sequence and look for 7"0's". When the $\overline{AMD}$ has acquired a 7"0" 3 gap sequence the $\overline{AMD}$ output pin transitions low. The $\overline{AMD}$ will remain low until $\overline{AMENB}$ is deasserted and then reasserted low or if RG is toggled high (see the soft sector read sequence diagram below).

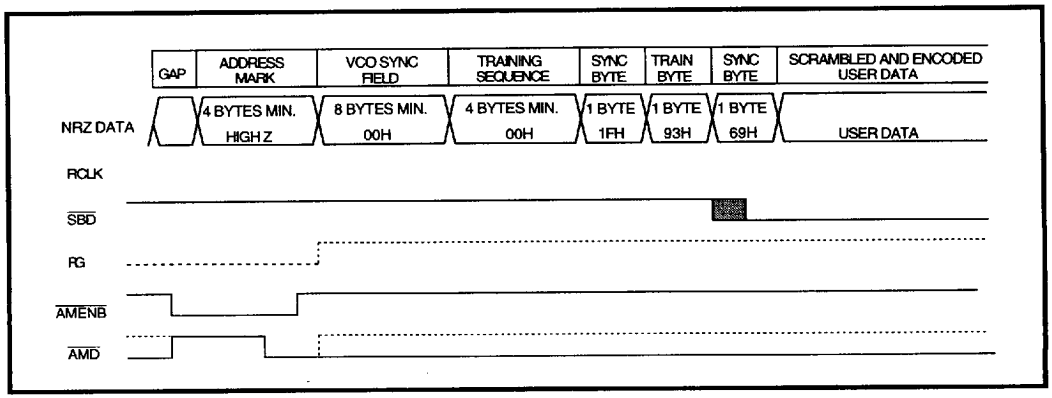

FIGURE 10: Soft Sector Read Sequence

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SOFT SECTOR OPERATIONS (continued)

Acquisition of DS VCO Sync

As soon as the Address Mark (AM) has been detected, the Read Gate input can be asserted high, initiating the remainder of the read sequence. When RG is asserted an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier given the polarity changes of the incoming 1,1,-1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches two polarity reversals, the internal read gate is asserted and the DS PLL input is switched from the TBG's VCO output to the sampled data input. This is also the point at which the DS PLL's phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter is also used to determine whether the selected sync field count, SFC, has been achieved. When the counter reaches the value specified by SFC, the data synchronizer PLL is assumed to be locked and settled (VCO lock). Also at SFC, the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, the SFC can be set to 64, 80, 96 or 128 from the Sample Loop Control Register. The SFC count starts when internal RG goes high. These values for the SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundary Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the Enable Phase Detector Gain Switching (GS) bit in the Control Operating Mode Register. When the GS bit is high, the phase detector gain is reduced by a factor of 6 or 10 as dictated by GS_10 (bit 7 in the Damping Ratio Control Register)after the SFC is reached. When the GS bit is low, no phase detector gain switching takes place.

Also after SFC, the AGC feedback will be switched from the continuous time fullwave rectifier to sampled data feedback.

At SFC, the internal VCO lock signal activates the code word boundary detection circuitry to define the proper decode boundaries. Also, at count SFC, the RCLK generator source switches from the TBG's VCO output to the DS VCO clock signal which is phase locked to the incoming read data samples. The DS VCO is assumed locked to the incoming read data samples at this point. A maximum of 1 RCLK time period may occur for the RCLK transition, however, no short duration glitches will occur. After the code word detection circuitry finds the proper code word boundary, the RCLK generator is resynchronized to guarantee that the RCLK is in sync with the data. The RCLK and NCLK outputs will not glitch and will not toggle during the RCLK generator resynchronization for up to 2 byte times maximum.

Also at the code word boundary detect, the internal 9-bit code words are allowed to pass to the ENDEC for decoding. This decoding will occur until read gate is deasserted.

Adaptive Equalizer Training Sequence

As was previously discussed, in a normal write sequence, a minimum of 4 bytes of NRZ 93H, sync byte #1 (1FH), another 93H and sync byte #2 (69H) must be written between the end of the VCO sync field and the beginning of the user data. The 5 bytes of 93H are 8,9 encoded and precoded during write mode to produce the adaptive equalizer training pattern. Also sync byte #1 has been chosen to have the same properties as the 93H training byte. During read mode, this sequence (100110011 read data sequence) is used to adaptively train the three tap transversal filter in a zero forcing manner. The error at the filter output is integrated to derive the tap weight multiplying coefficient, km. The filter input and output taps will have the same km. It is anticipated that the continuous time filter will be used for coarse equalization and that their transversal filter will be used adaptively for fine tuning. This will reduce km's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during data mode can selected from the Sample Loop Control Register. After the training pattern, if the loop is active during data, the equalizer loop gain will be reduced by 4. The loop's integration time constant is made inversely proportional to the selected data rate.

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Sync Byte Detect and NRZ Output

As the read data is 8,9 decoded, it is compared to one of two internally fixed sync bytes (1FH or 69H). Sync byte detection is considered to have occurred if either of the two sync bytes is found, but the sync byte detect output pin ($\overline{SBD}$) is transitioned at the position in time when the second sync byte (69H) would have been detected. The transition will occur on the rising edge of the RCLK period in which 69H sync byte occurs. The next byte presented on the NRZ outputs is the first byte of user data. $\overline{SBD}$ will remain low and NRZ data will continue to be presented at the NRZ interface until the read gate is deasserted at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state.

Surface Defect Scan Mode

The 34P3500 helps check for media defects using the surface defect scan mode. In write mode, all zeros are presented (written) at the NRZ interface. When this pattern is read back, bit 7 (DSE bit) of the N counter register is enabled which enables the surface defect scan mode. In this mode, $\overline{SBD}$ will transition low at SFC. The NRZ0 pin is monitored. If no defect occurs, the NRZ0 pin will stay low. If a defect occurs, the NRZ0 pin will transition high on the falling edge of RCLK and will stay high as long as a defect occurs.

Hard Sector Operation

In hard sector operation, Address Mark search and detection is not required, so by setting $\overline{AMENB}$ high, the Address Mark Detection circuitry is disabled and $\overline{AMD}$ remains inactive. A hard sector read operation begins with the assertion of RG which starts the VCO sync field counting as in soft sector mode and sequences identically. In all respects, with exception of the lack of an address mark search sequence, hard sector read operation is the same as soft sector read.

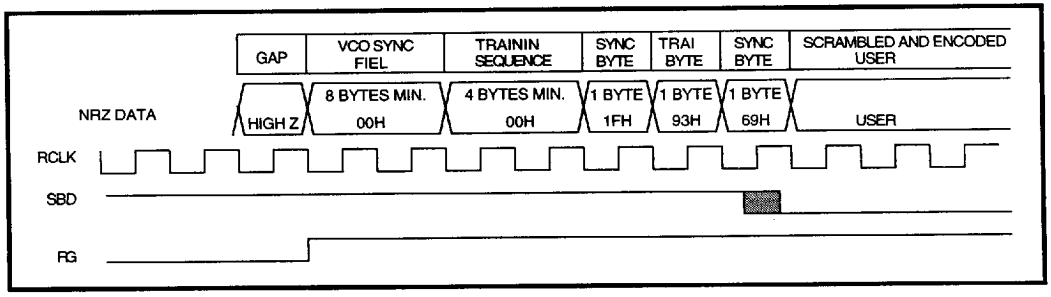

FIGURE 11: Hard Sector Read Sequence

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FUNCTIONAL DESCRIPTION (continued)

POWER DOWN OPERATION

The power management modes of the 34P3500 are determined by the states of the Power Down Register bits and the $\overline{\text{PDWN}}$ and SG inputs. The individual sections of the chip can be powered down or up using the Power Down Register. A high level in a Power Down Register bit disables that section of the circuit. The power down information from the Power Down Register takes effect immediately after the SDEN pin goes low.

When the $\overline{\text{PDWN}}$ input is low, the chip goes into full power down mode regardless of the power down register settings or the state of the SG input.

When $\overline{\text{PDWN}}$ is high, SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the front end register bit. The back end power down register bits, which include the Data Separator and Time Base Generator are not affected by the SG input.

The serial port is active in all power down modes.

The time to restart from a full power down is dependent on the PLL loop filter and the data rate.

The truth table for the various modes of operation is shown below:

SG, $\overline{\text{PDWN}}$	1,1	1,0	0,1	0,0
Front End	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Time Base Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON

R = Controlled by register bit
(Register bit =1 turns circuits OFF,
Register bit = 0 turns circuits ON)

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SERIAL PORT REGISTER DEFINITIONS

COMPLETE REGISTER STRING ID	A3	A2	A1	A0	S2	S1	S0	R/W
Power Down Register	0	0	0	1	0	1	0	0 = 04H
	Bit 7	ATO	Bit set to 1 enables ATO. Set bit to 0 for normal operation.					
	Bit 6	PCD	Bit set to 1 disables the precoder during preamble					
	Bit 5	PCPOL	Precoder preset polarity bit =1 sets precoder, bit = 0 resets it					
	Bit 4	PCDIS	Set to 1 to disable precoder preset function					
	Bit 3	FBYP	Set to 1 to bypass the filter for test purposes					
	Bit 2	TB	Time Base Generator power down					
	Bit 1	DS	Data Separator power down					
	Bit 0	PD	AGC, Filter, TBG, Pulse Detector, and Servo power down 1 = power down; 0 = power up					
Data Filter Cutoff Register	0	0	0	1	0	1	0	0 = 14H
	Bit 7	X	Don't care					
	Bits 6-0	FC6-0	Filter cutoff frequency setting in non-servo mode fc (MHz) = 0.000122 • FC² + 0.1783 • FC - 0.6118 (20 ≤ FC ≤ 127dec)					
Servo Filter Cutoff Register	0	0	1	0	0	1	0	0 = 24H
	Bit 7	X	Don't care					
	Bits 6-0	FCS6-0	Filter cutoff frequency setting in servo mode fc (MHz) = 0.000122•FCS² + 0.1783•FCS - 0.6118 (20 ≤ FC ≤ 127dec)					
Data Filter Boost Register	0	0	1	1	0	1	0	0 = 34H
	Bit 7	X	Don't care					
	Bits 6-0	FB6-0	Filter boost setting in servo mode Boost (dB) = 20 • log[0.02083 • FB + 0.000056•FB•FC - 0.000013•FB² +1] 0 ≤ FB ≤ 127dec					

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SERIAL PORT REGISTER DEFINITIONS (continued)

COMPLETE REGISTER STRING ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$
Servo Filter Boost Register	0	1	0	0	0	1	0	0 = 44H
	Bit 7	X	Don't care					
	Bits 6-0	FBS6-0	Filter boost setting in servo mode Boost (dB) = 20 • log[0.02083 • FBS + 0.000056•FBS•FCS - 0.000013•FBS^2 +1] 0 ≤ FBS ≤ 127dec					
Viterbi Detector Threshold Register	0	1	0	1	0	1	0	0 = 54H
	Bit 7	DS_SE	Disable toggle outputs (turn off CMOS outputs TBG0 and WDSE) 1 = disable					
	Bits 6-0	VD6-0	Viterbi qualification threshold voltage Vth (mV) = 9.94 • VD - 175 45 ≤ VD ≤ 127dec					
Data Level Threshold Register	0	1	1	0	0	1	0	0 = 64H
	Bit 7	X	Don't care					
	Bits 6-0	LD6-0	Data level qualification threshold voltage if WP/LT Register : ALE = 0 (Fixed levels) Prior to SFC : Lth (mV) = 4.784 • LD + 26 After SFC : Lth (mV) = 3.768 • LD + 18 32 ≤ LD ≤ 127dec if WP/LT Register : ALE = 1 (Adaptive levels) After SFC : Lth (%) = 0.787 • LD					
Servo Level Threshold Register	0	1	1	1	0	1	0	0 = 74H
	Bit 7	X	Don't care					
	Bits 6-0	LDS6-0	Servo level qualification threshold voltage LSth (mV) = 4.784 • LDS + 26					

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COMPLETE REGISTER STRING ID	A3	A2	A1	A0	S2	S1	S0	R/W
Control Test Mode Register	1	0	0	0	0	1	0	0 = 84H

Bit 7	EFR	Sample clock source 0 = sample clock is from the DS VCO, normal operation 1 = sample clock is from the TBG output, a test mode
Bit 6	-	Factory reserved bit, must be set to 0 in application
Bits 5-3	TP3-1	Multiplexed test point selection

TP3	TP2	TP1	Function	TPA+, TPA-	TPB+, TPB-
0	0	0	Test Points Off	high impedance	high impedance
0	0	1	Equalizer Outputs	Equalizer A	Equalizer B
0	1	0	Eq Cont/Phase Det	Equalizer Control	Phase Detect Out
0	1	1	Viterbi Survival In	SSIN B+, B-	SSIN A+, A-
1	0	0	Survival Out/In	Registers A, B	SSIN A+, A-
1	0	1	TBG/AGC Control	TBG output	BYP (buffered)
1	1	0	Eq Out/Survival In	Equalizer A	SSIN A+, A-
1	1	1	Eq Out/VCO ÷ 2	Equalizer A	DS VCO ÷ 2

Bit 2	VRDT	Enable VRDT input 1 = digital input to the data decoder, used in testing only 0 = Viterbi survival outputs to the data decoder, normal use
Bit 1	DT	Enable TBG pump down 1 = continuous pump down, for test use only FLTR1+ sinks current FLTR1- sources current 0 = not in pump down test mode
Bit 0	UT	Enable TBG pump up 1 = continuous pump up, for test use only FLTR1+ sources current FLTR1- sinks current 0 = not in pump up test mode

N Counter Register	1	0	0	1	0	1	0	0 = 94H

Bit 7	-	Factory Reserved, set to zero
Bits 6-0	N6-0	N Counter $2 \leq N \leq 127$

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SERIAL PORT REGISTER DEFINITIONS (continued)

COMPLETE REGISTER STRING ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$
M Counter Register	1	0	1	0	0	1	0	0 = A4H
	Bits 7-0	M7-0	M Counter $2 \leq M \leq 255$ FTBG = FREF • [(M+1) + (N+1)]					
Data Rate Register	1	0	1	1	0	1	0	0 = B4H
	Bit 7	X	Don't care					
	Bits 6-0	DR6-0	Fvco (MHz) = 9/8 Data Rate = 0.6685 • DR + 5.1					
Write Precomp / Level Threshold Time Constant Register	1	1	0	0	0	1	0	0 = C4H
	Bits 7-5	TC3-1	Adaptive Level qualification threshold time constant for Decision Directed Phase Detector. (Valid After SFC)					

TC3	TC2	TC1	Time Constant
0	0	0	300 ns
0	0	1	400 ns
0	1	0	500 ns
0	1	1	600 ns
1	0	0	700 ns
1	0	1	800 ns
1	1	0	900 ns
1	1	1	1000 ns

Bit 4	ALE	Enable adaptive level qualification in Decision Directed Phase Detector 1 = adaptive mode 0 = fixed level qualification
Bit 3	FSD	Fail Safe Disable
Bits 2-0	WPC2-0	Write Precomp setting

WPC2	WPC1	WPC0	Write Precomp Magnitude
0	0	0	No precomp
0	0	1	3.3% code period shift
0	1	0	6.6% code period shift
0	1	1	9.9% code period shift
1	0	0	13.2% code period shift
1	0	1	16.5% code period shift
1	1	0	19.8% code period shift
1	1	1	23.1% code period shift

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COMPLETE REGISTER STRING ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$
Control Operating Register	1	1	0	1	0	1	0	0 = D4H
	Bits 7	WGP	Write Gate Polarity 1 = Positive (active high); 0 = Negative (active low)					
	Bit 6	SPDM	Servo Peak Detect Mode 1 = Dual comparator (window); 0 = Hysteresis					
	Bit 5	BP	Enable bypass of write precoder 1 = enabled; 0 = disabled, (normal operation)					
	Bit 4	DB	Enable dual-bit interface 1 = dual-bit DB1-0 interface enabled 0 = dual-bit interface disabled, i.e., byte-wide interface enabled					
	Bit 3	BT	Bypass Time Base Generator 1 = data synchronizer reference frequency is FREF input 0 = data synchronizer reference frequency is TBG output, (normal operation)					
	Bit 2	SD	Disable Data Scrambler/Descrambler 1 = disabled; 0 = enabled, (normal operation)					
	Bit 1	GS	DS Phase Detector gain switching 1 = disabled; 0 = enabled, (normal operation)					
	Bit 0	DW	Enable Direct Write From Byte-wide NRZ (Bypasses scrambler & ENDEC) 1 = enabled; 0 = disabled, (normal operation)					

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SERIAL PORT REREGISTER DEFINITIONS (continued)

Complete Register String ID	A3	A2	A1	A0	S2	S1	S0	R/$\overline{W}$
Sample Loop Control Register	1	1	1	0	0	1	0	0 = E4H
	Bit 7	EHWG	Enable Hold during WG 0 = Typical AGC operation 1 = Hold AGC gain while WG/WG is enabled					
	Bits 6-5	SFC1-0	Sync Field Count					
			SFC1	**SFC0**	**Sync Field Count (code clocks)**			
			0	0	64			
			0	1	80			
			1	0	96			
			1	1	128			
	Bit 4	AEGS	Adaptive Equalizer Loop time constant shift 0 = equalizer loop time constant same in preamble & data fields 1 = equalizer loop time constant is increased to 3X in the data field relative to the preamble field, i.e., loop gain is reduced to 1/3					
	Bit 3	AED	Enable Adaptive Equalizer on Data Field 1 = adaptive equalizer in use after preamble field, if AEE bit = 1 0 = adaptive equalizer disabled after preamble field					
	Bit 2	AEE	Enable Adaptive Equalizer 1 = adaptive equalizer enabled for use in preamble field, and after the preamble field if AED bit = 1 0 = adaptive equalizer disabled					
	Bits 1-0	AGC1-0	AGC charge pump current in Sampled AGC mode AGC charge / discharge current (μA) = 0.28 • AGC • Data Rate (Mbit/s) e.g., for Data Rate = 72 Mbit/s and AGC = 10 = 2_{dec} charge pump current = 40.3 μA					
Damping Ratio Control Register	1	1	1	1	0	1	0	0 = F4H
	Bit 7	GS_10	Gain Shift Ratio 1 = 10x gain shift 0 = 6x gain shift					
	Bits 6-0	D6-0	Damping amplifier gain A = D • (0.7 / 127) Damping Ratio = $\frac{A \bullet KVCO \bullet 0.25}{2 \bullet \omega n}$					

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PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA		AGC / Filter analog circuit supply
VPF		Time Base Generator ECL supply (connect to analog supply)
VPT		Time Base Generator PLL analog circuit supply
VPP		Data Separator PLL analog circuit supply
VPD		TTL Buffer I/O digital supply
VPC		Internal ECL, CMOS logic digital supply
VPS		Sampled data processor supply
VNA		AGC / Filter analog circuit ground
VNF		Time Base Generator ECL ground (connect to analog ground)
VNT		Time Base Generator PLL analog circuit ground
VNP		Data Separator PLL analog circuit ground
VND		TTL Buffer I/O digital ground
VNC		Internal ECL, CMOS logic digital ground
VNS		Sampled data processor ground

ANALOG INPUT PINS

VIA+, VIA-	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator

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PIN DESCRIPTION (continued)

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
TPA+, TPA-	O	TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the Test Point Control Register. The signals include the equalizer control voltage and output, various timing loop control signals and the Viterbi survival register outputs. The test points are provided to show how the signal is being processed. Internal "pull down" resistors to ground are provided. To save power when not in test mode, the Control Test Register bits 3 - 5 must be set to "0".
TPB+, TPB-	O	TEST PINS: Emitter output test points similar to TPA+ and TPA-. The pins are used to look at the other phase of the interleaved signals.
ATO	O	ANALOG TEST OUT: A test point that is enabled by setting bit 7 in the Power Down Register to 1. This test point used to indicate the operation of controlled functions which cannot be easily determined by direct testing of the circuit pins. The selected output is determined by the address in the serial control register.
ATRN	O	ANALOG TEST OUT RETURN: A test point used as the ATO return. Nominal GND.
ON+, ON-	O	FILTER NORMAL OUTPUTS: These are the filter normal low pass output. They should be AC coupled to the data comparator in the pulse qualifier. Emitter output with internal pulldown. If driving more than coupling cap, external pull down resistor to GND may be required.
OD+, OD-	O	FILTER DIFFERENTIATED OUTPUTS: These are the filter time differentiated low pass output. They should be AC coupled, for low DC offset, to the clock comparator in the pulse qualifier. Emitter output with internal pulldown. If driving more than coupling cap, external pull down resistor to GND may be required.
SEROUT	O	MULTIPLEXED OUTPUT: Open Emitter. Full-wave rectified output referenced to SREF. Requires nominal 1 kΩ external pull down to GND.
SREF	O	SERVO REFERENCE OUTPUT: +2.0 VDC reference voltage, baseline for servo bursts. Open Emitter. Requires nominal 1 kΩ external pull down to GND.

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ANALOG CONTROL PINS

NAME	TYPE	DESCRIPTION
BYP		The data AGC integrating capacitor, CBYP, is connected between BYP and VPA. This pin is used when not in servo read mode (SG = 0).
BYPS		The servo AGC integrating capacitor, CBYPS, is connected between BYPS and VPA. This pin is used when in servo read mode (SG = 1).
FLTR1+, FLTR1-		TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2+, FLTR2-		DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR		CURRENT REFERENCE RESISTOR INPUT: An external 1%, 12.1 kΩ resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs.
VRX		FILTER REFERENCE RESISTOR INPUT: An external 1%,12.1 kΩ resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC		AGC REFERENCE VOLTAGE: VRC is derived by a bandgap reference from VPA.

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PIN DESCRIPTION (continued)

DIGITAL INPUT PINS

NAME	TYPE	DESCRIPTION
LOWZ	I	LOW-Z MODE INPUT: TTL compatible CMOS control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic high.
FASTREC	I	FAST RECOVERY: TTL compatible CMOS control pin which, when pulled high, puts the AGC charge pump in the fast decay mode. An open pin is a logic high.
$\overline{\text{AMENB}}$	I	ADDRESS MARK ENABLE: TTL compatible CMOS control pin which, when pulled low, enables the address mark detection and generation circuitry. An open pin is a logic high.
$\overline{\text{PDWN}}$	I	POWER DOWN CONTROL: CMOS power control pin. When set to logic low, the entire chip is in sleep mode with all circuitry, except serial port, shut down. This pin should be set to logic high in normal operating mode. Selected circuitry can also be shut down by the Power Down Register but is overridden by this pin. Do not leave open.
$\overline{\text{HOLD}}$	I	AGC HOLD CONTROL INPUT: TTL compatible CMOS control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
FREF	I	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. When bits 2 or 7 of the Control Test Register are set, FREF replaces the VCO as the input to the data separator.
WCLK	I	WRITE CLOCK: TTL compatible CMOS input that latches in the data at the selected NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG	I	READ GATE: TTL compatible CMOS input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the Read Data input and enables the read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG/$\overline{\text{WG}}$	I	WRITE GATE: TTL compatible CMOS input that enables the write mode. Register selection through serial port for active high or active low. An open pin is at logic high. Setting bit 7 in the Sample Loop Control Register to 1, enables hold on the AGC while WRITE GATE is active.
SG	I	SERVO GATE: TTL compatible CMOS input that, when pulled high, enables the servo read mode. An open pin is at logic high.

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DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
SELVRC	I	SERVO REFERENCE SELECT: TTL compatible CMOS input. When SG is low this input selects between the SREF reference (SELVRC = high) and the SREF + 200 mV level (SELVRC = low) for presentation at the SEROUT output.
VRDT	I	VITERBI READ DATA: A TTL or ac coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the Control Test Register.

DIGITAL BI-DIRECTIONAL PINS

NRZ0-7	I/O	BYTE WIDE NRZ DATA PORT: TTL compatible CMOS bi-directional input / output. Input to the encoder when WG/WG is active. Output from the decoder when RG is high. Can be left open if not used. Active when bit 4 of the Control Operating Register is set to 0.
DB0-1*	I/O	DUAL BIT NRZ DATA PORT: TTL compatible CMOS bi-directional input/ output. Input to the encoder when WG/WG is active. Output from the decoder when RG is high. Can be left open if not used. Active when bit 4 of the Control Operating Register is set to 1.

*Note: dual-bit circuitry is not tested.

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PIN DESCRIPTION (continued)

DIGITAL OUTPUT PINS

NAME	TYPE	DESCRIPTION
RCLK	O	READ REFERENCE CLOCK:A multiplexed clock source used by the controller. When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. CMOS output levels.
TBGO	O	TBG CLOCK: TBG Output gated by RG inactive and Viterbi Detector Threshold Register bit 7 (DS_SE). DS_SE bit = 0 and RG disabled enables this output. TTL output levels.
NCLK	O	NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the frequency of RCLK. NCLK is disabled in dual bit mode. CMOS output levels.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tri-state output pin that is in its high impedance state when WG/$\overline{WG}$ is active or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. CMOS output levels.
$\overline{SBD}$	O	SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte and transitions after positive edge of RCLK. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.
WDSE	O	WRITE DATA: Write data output. The data is automatically re-synchronized (independent of the delay between RCLK and WCLK) to the reference clock F_{TBG}, except in Direct Write mode. WDSE pulses for every 1 bit. TTL output levels. This is also enabled by DS_SE low.
$\overline{RDS}$	O	SERVO READ DATA: Read Data Pulse output for servo read data. Active low CMOS output. Output active when SG is high, and high when SG is low.
PPOL	O	SERVO READ DATA POLARITY: Read Data Pulse polarity output for servo read data. Active high CMOS output. A negative swing servo read data leads to a low output of PPOL and a positive swing servo read data leads to a high output of PPOL. Output active when SG is high.

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SERIAL PORT PINS

NAME	TYPE	DESCRIPTION
SCLK	I	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. CMOS input levels.
SDATA	I	SERIAL DATA: Input pin for serial data; The first bit is the R/$\overline{W}$ bit and is always set to 0. The next three bits are the device select bits and are always written S0 = 0, S1 = 1, S2 = 0. The following four bits are the address bits A0 - A3 and the last 8 are the data bits D0-D7. The bits are entered LSB first, MSB last. CMOS input levels.
SDEN	I	SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. CMOS input levels.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Positive 5.0V Supply Voltage (Vp)	-0.5 to 7V
Storage Temperature	-65 to 150°C
Solder Vapor Bath	215°C, 90 sec, 2 times
Junction Operating Temperature	+130°C
Output Pin	± 10 mA
Analog Pins	± 10 mA
Voltage Applied to other Pins	-0.3V to Vp + 0.3V

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
ICC VPN	Outputs and test point pins open Ta = 27°C		150		mA
PWR Power Dissipation Normal Mode	Outputs and test point pins open Ta = 27°C		750	1200	mW
PWR Data Separator Off	Power Down Register = 2d		325	470	mW
PWR Data Separator & TBG Off	Power Down Register = 6d		310	450	mW
PWR Idle Through Serial Port	Power Down Register = 7d			15	mW
Idle	$\overline{PDWN}$ = low			5	mW

DIGITAL INPUTS

TTL Compatible CMOS Inputs

Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2.0		VPD2 + 0.3	V
Input low current	I_{IL}	V_{IL} = 0.4V	-200			µA
Input high current	I_{IH}	V_{IH} = 2.4V			20	µA
Input Low Current	I_{ILF}	V_{IL} = 0.4V, FREF, VRDT	-250			µA
Input High Current	I_{IHF}	V_{IH} = 2.4V, FREF, VRDT			500	µA

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CMOS Inputs

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage	V_{ILC}	VPC = 5.0V			1.5	V
Input High Voltage	V_{IHC}	VPC = 5.0V	3.5			V

Pseudo ECL Compatible Inputs

Input Low Voltage	V_{IL}		VPD - 2.0		VIH - 0.25	V
Input High Voltage	V_{IH}		VPD - 1.1		VPD - 0.4	V
Input Current			-100		+100	µA

DIGITAL OUTPUTS
CMOS Outputs (RCLK, SBD, NRZ0-7)

Output Low Voltage	I_{OL} = +2 mA			0.45	V
Output High Voltage	I_{OH} = -100 µA	0.7 • VPD			V
Rise Time	C_L = 15 pF			10	ns
Fall Time	C_L = 15 pF			15	ns

Digital Differential Outputs

Output Low Voltage	I_{OL} = 2 ma	VPD - 1.9		VOH - 0.3	V
Output High Voltage	I_{OH} = 2 ma	VPD - 1.4		VPD - 0.5	V
Output Sink Current			3.2		mA

TEST POINT OUTPUT LEVELS

Test Point Output TPA+, TPA- TPB+, TPB-			0.8		Vp-pd
ATO Test Point	$R_{LOAD} \geq 10\ M\Omega$	0		1	V

Serial Port Timing
Refer to Figure 6

SCLK Data Clock Period	TC		100			ns
SCLK Low Time	T_{CKL}		40			ns
SCLK High Time	T_{CKH}		40			ns
Enable to SCLK	T_{SENS}		30			ns
SCLK to Disable	T_{SNEH}		30			ns
Data Set-up Time	T_{DS}		15			ns
Data Hold Time	T_{DH}		15			ns
SDEN Min. Low Time	T_{SL}		200			ns

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ELECTRICAL SPEICIFICATIONS (continued)

AGC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. ON+ and ON- are ac coupled to DP and DN. Integrating capacitor C_{BYP} = 1000 pF, is connected between BYP and VPA. Integrating capacitor C_{BYPS} = 1000 pF, is connected between BYPS and VPA. Unless otherwise specified, the output is measured differentially at DP and DN, Fin = 5 MHz, the filter frequency fc = max and the filter boost at fc = 0 dB. All specifications apply equally to servo and read mode prior to SFC.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Range	Filter Boost = 0 dB @ fc 5 MHz ≤ fc ≤ 18 MHz, Fin = fc	20		250	mVp-pd
Input Range	Filter Boost = 11 dB @ fc 9 MHz ≤ fc ≤ 18 MHz, Fin = fc	20		200	mVp-pd
DP/DN Voltage	VIA = 0.1 Vp-pd 1,1,-1,-1,— pattern	1.19	1.4	1.61	Vp-pd
DP/DN Voltage Variation	20 mVp-pd < VIA < 250 mVp-pd			5.0	%
Maximum Gain		64			V/V
Minimum Gain				1	V/V
Gain Sensitivity	BYP voltage change		38		dB/V
Differential Input Impedance	LOWZ = low	4.0	5.3	7.7	kΩ
	LOWZ = high		280		Ω
Single-ended Input Impedance	LOWZ = low		1.7		kΩ
	LOWZ = high		100		Ω
Output Offset Voltage	Gain = 64 V/V	-300		300	mV
Input Noise Voltage	Gain = 64 V/V, Rs = 0 Ω		15	30	nV/√Hz
CMRR	Gain = 64 V/V Fin = 5 MHz	35			dB
PSRR	Gain = 64 V/V Fin = 5 MHz	40			dB
Gain Decay Time	VIA = 240 to 120 mVp-pd DP/DN > 0.9 Final Value		21.0		µs
Gain Attack Time	VIA = 120 to 240 mVp-pd DP/DN < 1.1 Final Value		3.0		µs

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AGC CONTROL SECTION

The input signals are AC coupled into DP/DN, C_{BYP} = 1000 pF to VPA & C_{BYPS} = 1000 pF to VPA.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Decay current Normal I_D	FASTREC = low, SG = low Data Rate in Mbit/s 24 ≤ Data Rate ≤ 80		$2.8 \cdot 10^{-7} \cdot$ Data Rate		A
Servo Mode Decay current Normal	FASTREC = low, SG = high		8.3		µA
Fast Discharge Current I_{DF}	FASTREC = high		$8 \cdot I_D$		A
Charge Pump Attack Current I_{CH}	TBD≤DP/DN≤TBD Vp-pd FASTREC = low		$17 \cdot I_D$		A
Fast Attack I_{CHF}	|DP - DN| ≥ 0.65V AGC pin open		$8.4 \cdot I_{CH}$		A
Sample Data AGC Peak Charge Current	0 ≤ AGC ≤ 3 Data Rate in Mbit/s		$2.8 \cdot 10^{-7} \cdot$ AGC • Data Rate		A
Sample Data AGC Peak Discharge Current	0 ≤ AGC ≤ 3 Data Rate in Mbit/s		$2.8 \cdot 10^{-7} \cdot$ AGC • Data Rate		A
BYP Pin Leakage Current	$\overline{HOLD}$ = low VBYP = VRC	-50		+50	nA
BYPS Pin Leakage Current	$\overline{HOLD}$ = low VBYP = VRC	-50		+50	nA
VRC Reference Voltage	-100 µA ≤ IO ≤ 500 µA	VPA - 2.55		VPA - 2.15	V

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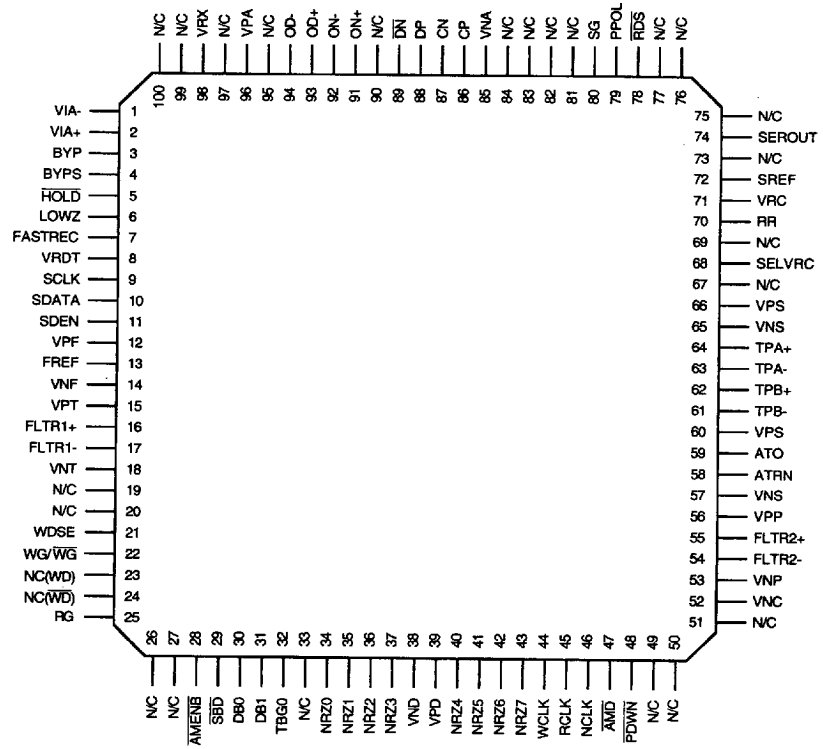
SSI 34P3500
PRML Read Channel with
PR4, 8/9 ENDEC, FWR Servo

PACKAGE PIN DESIGNATIONS
(Top View)



100 Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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