Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

IDT71B88

FEATURES:

- 16K x 4 BiCMOS static RAM
- High-speed address/chip select time
  — Commercial: 10/12ns
- Single chip select
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 22-pin, 300 mil plastic DIP; and 24-pin, 300 mil plastic SOJ packages

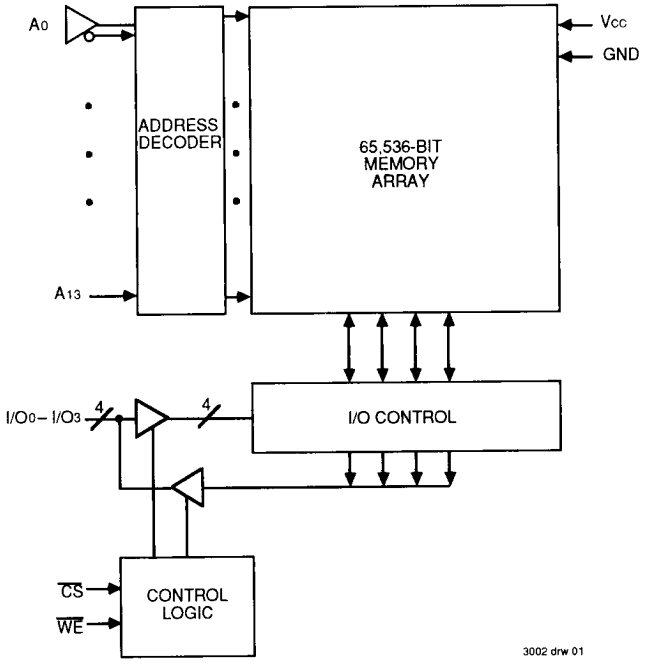
DESCRIPTION:

The IDT71B88 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B88 are TTL-compatible, and operation is from a single 5V supply.

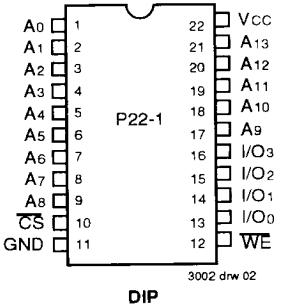
The IDT71B88 is packaged in a 22-pin, 300 mil plastic DIP and a 24-pin, 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



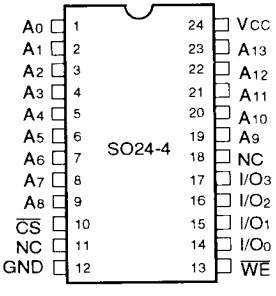
3002 drw 01

PIN CONFIGURATIONS



3002 drw 02

DIP
TOP VIEW



3002 drw 02a

SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3002 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} must not exceed V_{CC} + 0.5V.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	I/O	Function
L	H	$DATA_{OUT}$	Read
L	L	$DATA_{IN}$	Write
H	X	High-Z	Deselect Chip

NOTE: 3002 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, SOJ package only)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3002 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 3002 tbl 04

1. VIL (Min.) = –1.5V for pulse width less than 10ns, once per cycle.

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B88 Min.	IDT71B88 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3002 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B88S10 Com'l.	71B88S12 Com'l.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	180	160	mA

NOTES: 3002 tbl 05

1. All values are maximum guaranteed values.
2. fMAX = 1/tRC, all Address inputs are cycling at f_{MAX}.

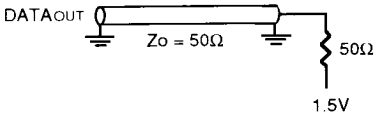
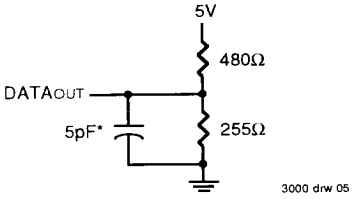


Figure 1. AC Test Load

2962 drw 04



*Including jig and scope capacitance.

Figure 2.

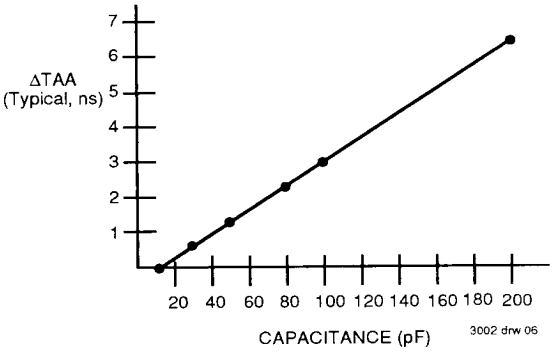


Figure 3. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 & 3

3002 tbl 06

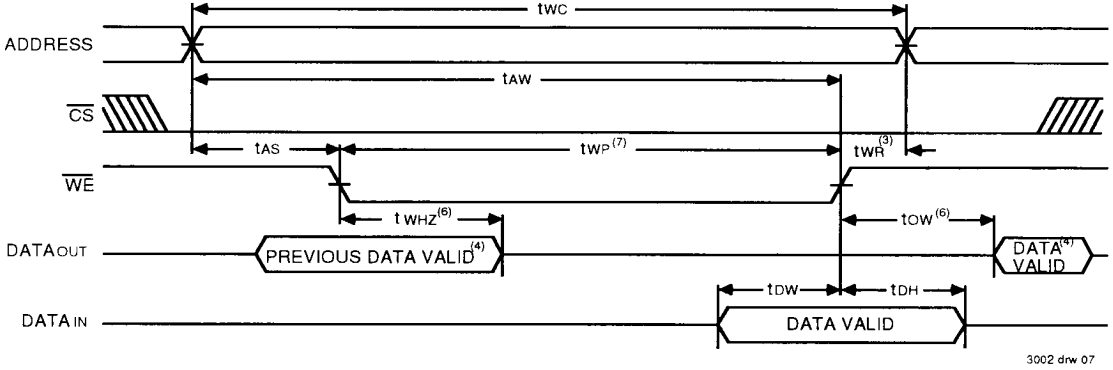
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B88S10 Min.	71B88S10 Max.	71B88S12 Min.	71B88S12 Max.	Unit
Read Cycle						
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{ACS}	$\overline{CS}$ Access Time	—	6	—	7	ns
t_{CLZ}(1)	$\overline{CS}$ to Output in Low-Z	1	—	1	—	ns
t_{CHZ}(1)	$\overline{CS}$ to Output in High-Z	—	6	—	7	ns
t_{OH}	Out Hold from Address Change	3	—	3	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Select to End-of-Write	8	—	9	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	9	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}(1)	$\overline{WE}$ to Output in High-Z	—	3	—	4	ns
t_{DW}	Data Set-Up Time	5	—	6	—	ns
t_{DH}	Data Hold from Write	0	—	0	—	ns
t_{OW}(1)	Out Active from End-of-$\overline{WE}$	3	—	3	—	ns

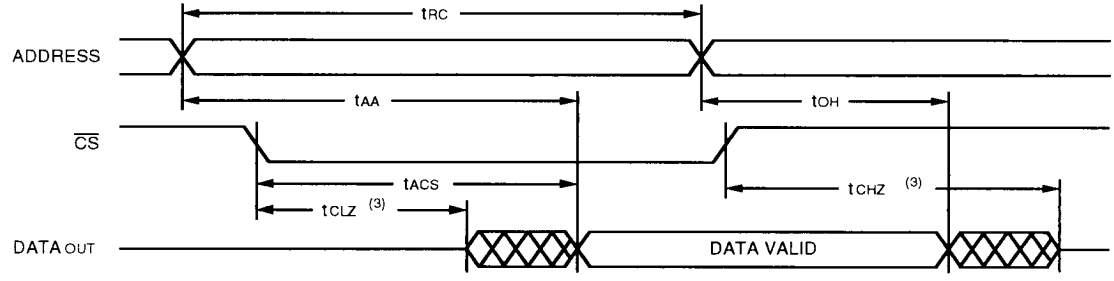
3002 tbl 08

NOTES:
1. This parameter is guaranteed with the AC Load (Figure 2) by device chracterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2)



TIMING WAVEFORM OF READ CYCLE NO.2 (1,2,3)



NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
3. Transition is measured ±200mV from steady state.

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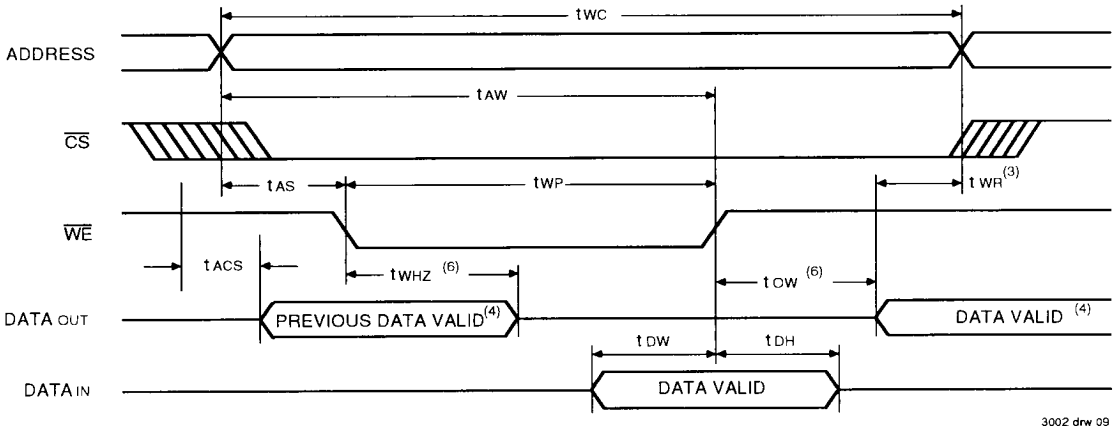
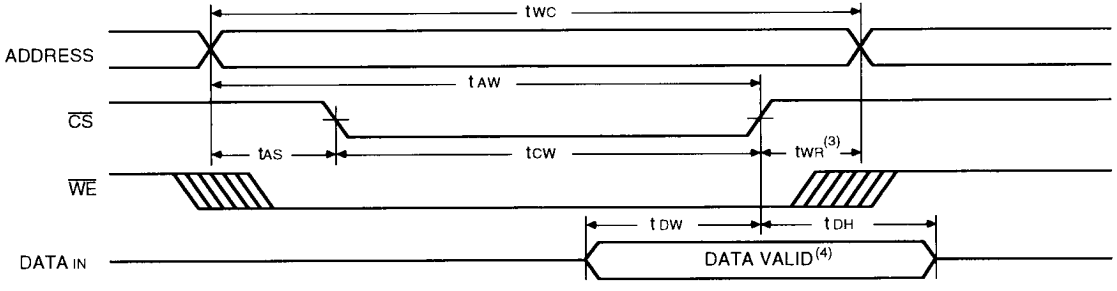
TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,5)



3002 drw 09

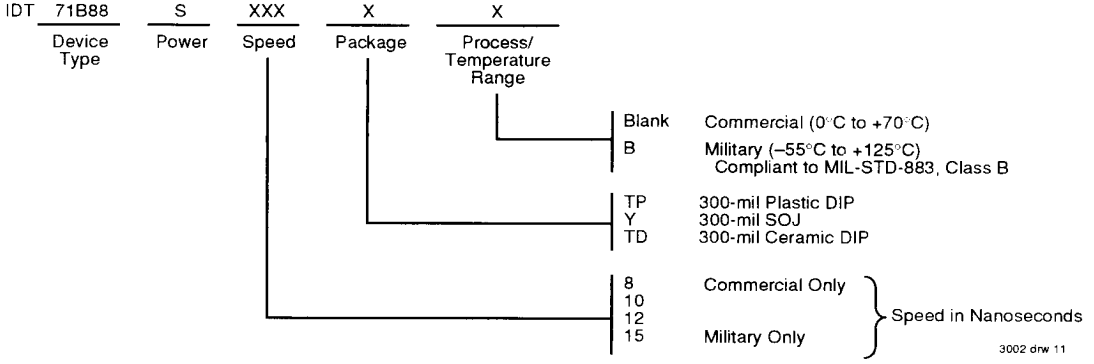
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4)



3002 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state. If CS high transition occurs simultaneously with or before WE high transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



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