Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

T7689 5.0 V T1 Quad Line Interface

Features

- Four fully integrated T1 line interfaces
- Includes all driver, receiver, equalization, clock recovery, and jitter attenuation functions
- Ultralow power consumption
- Robust operation for increased system margin
- High interference immunity
- On-chip transmit equalization for improved sensitivity
- Low-impedance drivers for reduced power consumption
- Selectable transmit or receive, jitter attenuation/ clock smoothing
- 3-state transmit drivers
- High-speed, microprocessor interface
- Automatic transmit monitor function
- Per-channel powerdown
- For use in systems that are compliant with AT&T CB119; TR-TSY-000170, TR-TSY-000009, TR-TSY-000499, TR-TSY-000253; ANSI T1.102 and T1.403
- Common transformer for transmit/receive
- Fine-pitch (25 mil spacing) surface-mount package, 100-pin bumpered quad flat pack
- –40 °C to +85 °C operating temperature range

Applications

- SONET/SDH multiplexers
- Asynchronous multiplexers (M13)
- Digital access cross connects (DACs)
- Channel banks
- Digital radio base stations, remote wireless modules
- PBX interfaces

Description

The T7689 is a fully integrated quad line interface containing four transmit and receive channels for use in North American (T1/DS1) applications. The device has many of the same functions as the Lucent Technologies Microelectronics Group T7290A and provides additional flexibility for the system designer.

Included is a parallel microprocessor interface that allows the user to define the architecture, initiate loopbacks, and monitor alarms. The interface is compatible with many commercially available microprocessors.

The receiver performs clock and data recovery using a fully integrated digital phase-locked loop. This digital implementation prevents false-lock conditions that are common when recovering sparse data patterns with analog phase-locked loops. Equalization circuitry in the receiver guarantees a high level of interference immunity. As an option, the raw sliced data (no retiming) can be output on the receive data pins.

Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. The quad device will interface to the digital cross connect (DSX) at lengths of up to 655 ft. for DS1 operation.

A selectable jitter attenuator may be placed in the receive signal path for low-bandwidth line-synchronous applications, or it may be placed in the transmit path for multiplexer applications where DS1 signals are demultiplexed from higher rate signals. The jitter attenuator will perform the clock smoothing required on the resulting demultiplexed gapped clock.

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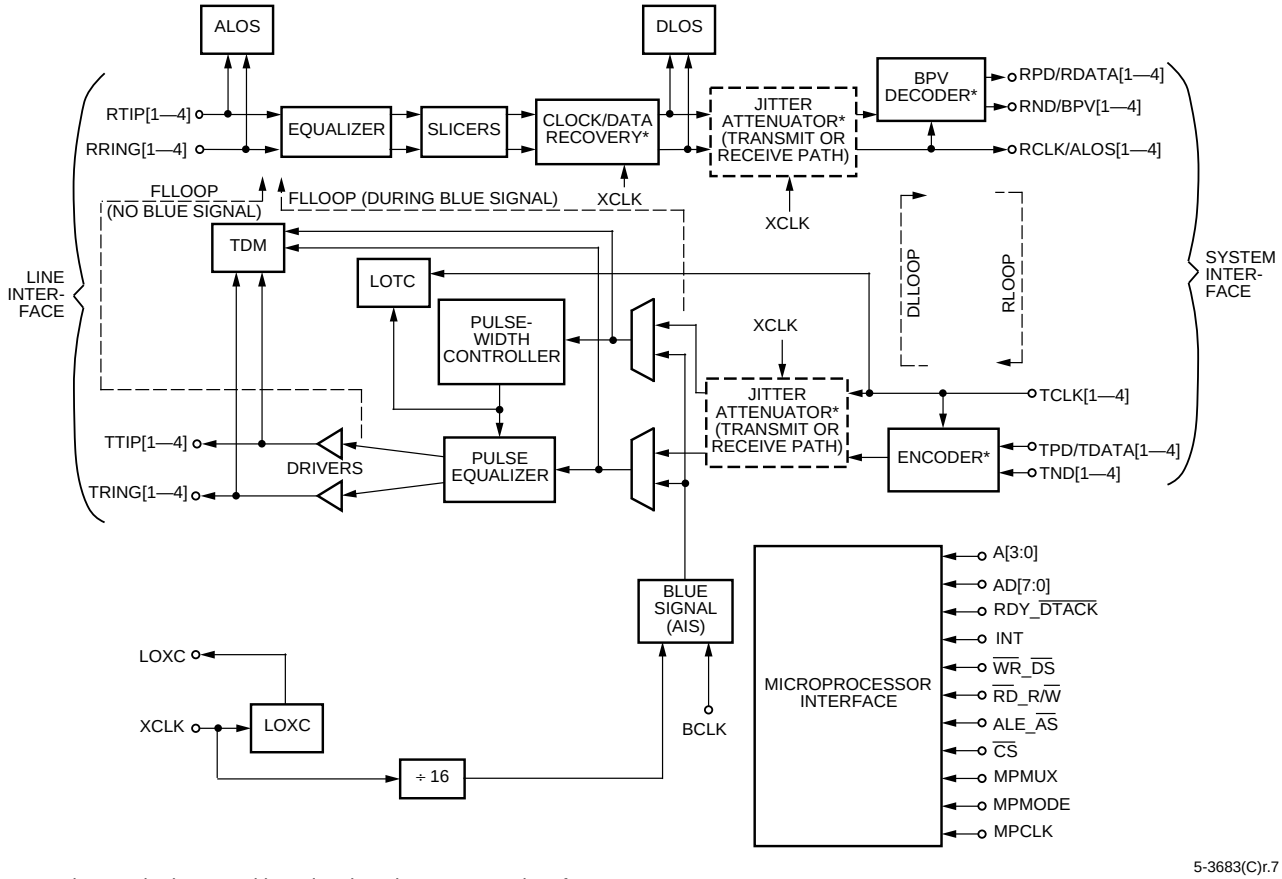
Block Diagram

The T7689 block diagram is shown in Figure 1. For illustration purposes, only one of the four on-chip line interfaces is shown. Pin names that apply to all four channels are followed by the designation [1—4].



* Function can be bypassed by using the microprocessor interface.

Figure 1. Block Diagram (Single Channel)

Pin Information

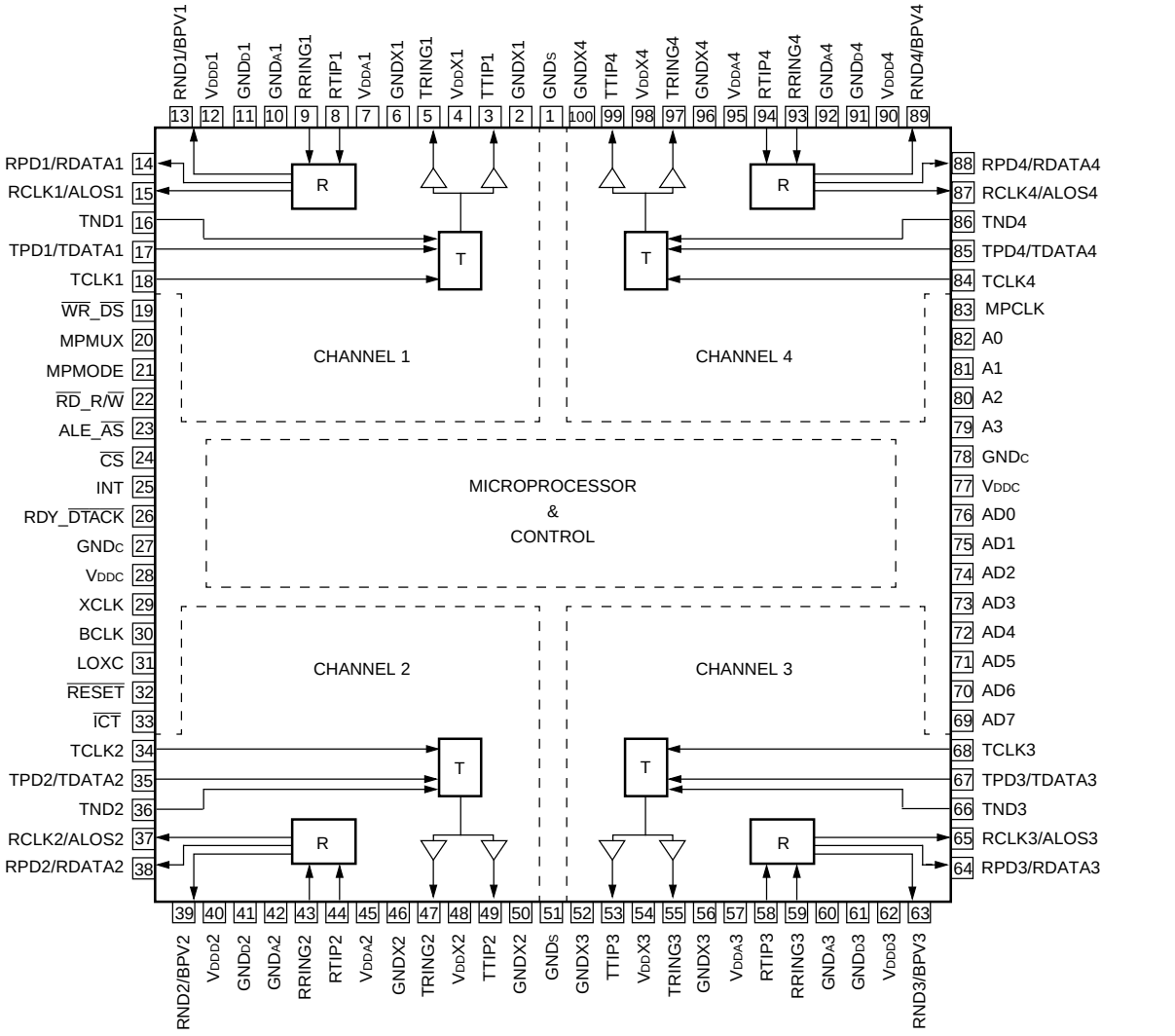


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Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Description
1, 51	GNDS	P	**Ground Reference for Substrate**.
2, 6	GNDX1	P	**Ground Reference for Line Drivers.**
46, 50	GNDX2		
52, 56	GNDX3		
96, 100	GNDX4		
3	TTIP1	O	**Transmit Bipolar Tip**. Positive bipolar transmit output data to the analog line interface.
49	TTIP2		
53	TTIP3		
99	TTIP4		
4	VDDX1	P	**Power Supply for Line Drivers.** The T7689 device requires a 5 V ± 5% power supply on these pins.
48	VDDX2		
54	VDDX3		
98	VDDX4		
5	TRING1	O	**Transmit Bipolar Ring**. Negative bipolar transmit output data to the analog line interface.
47	TRING2		
55	TRING3		
97	TRING4		
7	VDDA1	P	**Power Supply for Analog Circuitry**. The T7689 device requires a 5 V ± 5% power supply on these pins.
45	VDDA2		
57	VDDA3		
95	VDDA4		
8	RTIP1	I	**Receive Bipolar Tip**. Positive bipolar receive input data from the analog line interface.
44	RTIP2		
58	RTIP3		
94	RTIP4		
9	RRING1	I	**Receive Bipolar Ring**. Negative bipolar receive input data from the analog line interface.
43	RRING2		
59	RRING3		
93	RRING4		
10	GNDA1	P	**Ground Reference for Analog Circuitry**.
42	GNDA2		
60	GNDA3		
92	GNDA4		

* P = power, I = input, O = output, and I^U = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
11	GNDD1	P	**Ground Reference for Digital Circuitry**.
41	GNDD2		
61	GNDD3		
91	GNDD4		
12	VDDD1	P	**Power Supply for Digital Circuitry**. The T7689 device requires a 5 V ± 5% power supply on these pins.
40	VDDD2		
62	VDDD3		
90	VDDD4		
13	RND1/BPV1	O	**Receive Negative Data.** When in dual-rail (DUAL = 1: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the receive negative NRZ output data to the terminal equipment. When in data slicing mode (CDR = 0), this signal is the raw sliced negative output data of the front end. **Bipolar Violation.** When in single-rail (DUAL = 0: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), and CODE = 1 (register 5, bit 3), this signal is asserted high to indicate the occurrence of a code violation in the receive data stream. If CODE = 0, this signal is asserted to indicate the occurrence of a bipolar violation in the receive data system.
39	RND2/BPV2		
63	RND3/BPV3		
89	RND4/BPV4		
14	RPD1/ RDATA1	O	**Receive Positive Data.** When in dual-rail (DUAL = 1: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the receive positive NRZ output data to the terminal equipment. When in data slicing mode (CDR = 0), this signal is the raw sliced positive output data of the front-end. **Receive Data.** When in single-rail (DUAL = 0: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the receive NRZ output data.
38	RPD2/ RDATA2		
64	RPD3/ RDATA3		
88	RPD4/ RDATA4		
15	RCLK1/ ALOS1	O	**Receive Clock.** In clock recovery mode (CDR = 1: register 5, bit 0), this signal is the receive clock for the terminal equipment. The duty cycle of RCLK is 50% ± 5%. **Analog Loss of Signal.** In data slicing mode (CDR = 0: register 5, bit 0), this signal is asserted high to indicate low amplitude receive data at the RTIP/RRING inputs.
37	RCLK2/ ALOS2		
65	RCLK3/ ALOS3		
87	RCLK4/ ALOS4		
16	TND1	I	**Transmit Negative Data.** Transmit negative NRZ input data from the terminal equipment.
36	TND2		
66	TND3		
86	TND4		

* P = power, I = input, O = output, and I^u = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
17	TPD1/ TDATA1	I	**Transmit Positive Data.** When in dual-rail mode (DUAL = 1: register 5, bit 4), this signal is the transmit positive NRZ input data from the terminal equipment. **Transmit Data.** When in single-rail mode (DUAL = 0: register 5, bit 4), this signal is the transmit NRZ input data from the terminal equipment.
35	TPD2/ TDATA2		
67	TPD3/ TDATA3		
85	TPD4/ TDATA4		
18	TCLK1	I	**Transmit Clock.** DS1 (1.544 MHz ± 32 ppm). Clock signal from the terminal equipment.
34	TCLK2		
68	TCLK3		
84	TCLK4		
19	$\overline{WR}$_$\overline{DS}$	I	**Write (Active-Low)**. If MPMODE = 1 (pin 21), this pin is asserted low by the microprocessor to initiate a write cycle. **Data Strobe (Active-Low)**. If MPMODE = 0 (pin 21), this pin becomes the data strobe for the microprocessor. When R/$\overline{W}$ = 0 (write), a low applied to this pin latches the signal on the data bus into internal registers.
20	MPMUX	I	**Microprocessor Multiplex Mode**. Setting MPMUX = 1 allows the microprocessor interface to accept multiplexed address and data signals. Setting MPMUX = 0 allows the microprocessor interface to accept demultiplexed (separate) address and data signals.
21	MPMODE	I	**Microprocessor Mode**. When MPMODE = 1, the device uses the address latch enable type microprocessor read/write protocol with separate read and write controls. Setting MPMODE = 0 allows the device to use the address strobe type microprocessor read/write protocol with a separate data strobe and a combined read/write control.
22	$\overline{RD}$_R/$\overline{W}$	I	**Read (Active-Low)**. If MPMOD = 1 (pin 21), this pin is asserted low by the microprocessor to initiate a read cycle. **Read/Write**. If MPMODE = 0 (pin 21), this pin is asserted high by the microprocessor to indicate a read cycle or asserted low to indicate a write cycle.
23	ALE_$\overline{AS}$	I	**Address Latch Enable**. If MPMODE = 1 (pin 21), this pin becomes the address latch enable for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers. **Address Strobe (Active-Low)**. If MPMODE = 0 (pin 21), this pin becomes the address strobe for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers.
24	$\overline{CS}$	I^u	**Chip Select (Active-Low)**. This pin is asserted low by the microprocessor to enable the microprocessor interface. If MPMUX = 1 (pin 20), $\overline{CS}$ can be externally tied low to use the internal chip selection function (see the Internal Chip Select Function section). An internal 100 kΩ pull-up is on this pin.

* P = power, I = input, O = output, and I^u = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
25	INT	O	**Interrupt**. This pin is asserted high to indicate an interrupt produced by an alarm condition in register 0 or 1. The activation of this pin can be masked by microprocessor registers 2, 3, and 4.
26	RDY_$\overline{\text{DTACK}}$	O	**Ready**. If MPMODE = 1 (pin 21), this pin is asserted high to indicate the device has completed a read or write operation. This pin is in a 3-state condition when $\overline{\text{CS}}$ (pin 24) is high. **Data Transfer Acknowledge (Active-Low).** If MPMODE = 0 (pin 21), this pin is asserted low to indicate the device has completed a read or write operation.
27, 78	GND_C	P	**Ground Reference for Microprocessor Interface and Control Circuitry**.
28, 77	V_DDC	P	**Power Supply for Microprocessor Interface and Control Circuitry.** The T7689 device requires a 5 V ± 5% power supply on these pins.
29	XCLK	I^u	**Reference Clock**. A valid reference clock (24.704 MHz ± 100 ppm for DS1 operation) must be provided at this input for certain applications (see the XCLK Reference Clock section). XCLK must be an independent, continuously active, ungapped, and unjittered clock to guarantee device performance specifications. An internal 100 kΩ pull-up is on this pin.
30	BCLK	I^u	**Blue Clock**. Input clock signal used to transmit the blue signal (all 1s data pattern). In DS1 mode, this clock is 1.544 MHz ± 32 ppm. An internal 100 kΩ pull-up is on this pin.
31	LOXC	O	**Loss of XCLK**. This pin is asserted high when the XCLK signal (pin 29) is not present.
32	$\overline{\text{RESET}}$	I^u	**Hardware Reset (Active-Low)**. If $\overline{\text{RESET}}$ is forced low, all internal states in the line interface paths are reset and data flow through each channel will be momentarily disrupted (see the RESET ($\overline{\text{RESET}}$, SWRESET) section). The $\overline{\text{RESET}}$ pin must be held low for a minimum of 10 µs. An internal 50 kΩ pull-up is on this pin.
33	$\overline{\text{ICT}}$	I^u	**In-Circuit Test Control (Active-Low)**. If $\overline{\text{ICT}}$ is forced low, certain output pins are placed in a high-impedance state (see the In-Circuit Testing and Driver 3-State ($\overline{\text{ICT}}$) section). An internal 50 kΩ pull-up is on this pin.
69	AD7	I/O	**Microprocessor Interface Address/Data Bus.** If MPMUX = 0 (pin 20), these pins become the bidirectional, 3-statable data bus. If MPMUX = 1, these pins become the multiplexed address/data bus. In this mode, only the lower 4 bits (AD[3:0]) are used for the internal register addresses.
70	AD6		
71	AD5		
72	AD4		
73	AD3		
74	AD2		
75	AD1		
76	AD0		

* P = power, I = input, O = output, and I^u = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
79	A3	I	**Microprocessor Interface Address.** If MPMUX = 0 (pin 20), these pins become the address bus for the microprocessor interface registers. If MPMUX = 1, A3 (pin 79) can be externally tied high to use the internal chip selection function (see the Internal Chip Select Function section). If this function is not used, A[3:0] must be externally tied low.
80	A2		
81	A1		
82	A0		
83	MPCLK	I	**Microprocessor Interface Clock.** Microprocessor interface clock rates from twice the frequency of the line clock (3.088 MHz for DS1 operation) to 16.384 MHz are supported.

* P = power, I = input, O = output, and I^U = input with internal pull-up.

System Interface Pin Options

The system interface can be configured to operate in a number of different modes, as shown in Table 2. Dual-rail or single-rail operation is possible using the DUAL control bit (register 5, bit 4). Dual-rail mode is enabled when DUAL = 1; single-rail mode is enabled when DUAL = 0. In dual-rail operation, data received from the line interface on RTIP and RRING appears on RPD (pins 14, 38, 64, 88) and RND (pins 13, 39, 63, 89) at the system interface and data transmitted from the system interface on TPD (pins 17, 35, 67, 85) and TND (pins 16, 36, 66, 86) appears on TTIP and TRING at the line interface. In single-rail operation, data received from the line interface on RTIP and RRING appears on RDATA (pins 14, 38, 64, 88) at the system interface and data transmitted from the system interface on TDATA (pins 17, 35, 67, 85) appears on TTIP and TRING at the line interface.

In both dual-rail and single-rail operation, the clock/data recovery mode is selectable via the CDR bit (register 5, bit 0). When CDR = 1, the clock and data recovery is enabled and the system interface operates in a nonreturn to zero (NRZ) digital format. When CDR = 0, the clock and data recovery is disabled and the system interface operates on unretimed sliced data in RZ data format (see the Data Recovery section).

In single-rail mode only, B8ZS encoding/decoding may be selected by setting CODE = 1 (register 5, bit 3). This allows coding violations, such as receiving two consecutive 1s of the same polarity from the line interface, to be output on BPV (pins 13, 39, 63, 89) (see the Zero Substitution Encoding/Decoding (CODE) section).

Table 2. Pin Mapping

Configuration	RCLK/ ALOS	RPD/ RDATA	RND/BPV	TPD/ TDATA	TND
Dual-rail System Interface with Clock Recovery	RCLK	RPD	RND	TPD	TND
Dual-rail System Interface with Data Slicing Only	ALOS	RPD	RND		
Single-rail System Interface with Clock Recovery	RCLK	RDATA	BPV	TDATA	NOT USED
Single-rail System Interface with Data Slicing Only	ALOS	RPD	RND		

Receiver

Data Recovery

The receive line interface transmission format of the device is bipolar alternate mark inversion (AMI). It accepts input data with a frequency tolerance of ±130 ppm (DS1). The receiver first restores the incoming data and detects analog loss of signal. Subsequent processing is optional and depends on the programmable device configuration established within the microprocessor interface registers. The receiver operates with high interference immunity, utilizing an equalizer to restore fast rise/fall times following maximum cable loss. The signal is then peak-detected and sliced to produce digital representations of the data.

Selectable clock recovery of the sliced data, digital loss of signal, jitter attenuation, and data decoding are performed. For applications bypassing the clock recovery function (CDR = 0), the receive digital output format is unretimed sliced data (RZ positive and negative data). For clock recovery applications (CDR = 1), the receive digital output format is nonreturn to zero (NRZ) with selectable dual-rail or single-rail system interface. The recovered clock (RCLK, pins 15, 37, 65, 87) is only provided when CDR = 1 (see Table 2).

Timing recovery is performed by a digital phase-locked loop that uses XCLK (pin 29) as a reference to lock to the incoming data. Because the reference clock is a multiple of the received data rate, the output RCLK (pins 15, 37, 65, 87) will always be a valid DS1 clock that eliminates false-lock conditions. During periods with no input signal, the free-run frequency is defined to be XCLK/16. RCLK is always active with a duty-cycle centered at 50%, deviating by no more than ±5%. Valid data is recovered within the first few bit periods after the application of XCLK. The delay of the data through the receive circuitry is approximately 1 bit to 14 bit periods, depending on the CDR and CODE configurations. Additional delay is introduced if the jitter attenuator is selected for operation in the receive path (see the Data Delay section).

Jitter

The receiver is designed to accommodate large amounts of input jitter. The receiver jitter performance far exceeds the requirements shown in Table 4. Jitter transfer is independent of input ones density on the line interface. High-frequency jitter tolerance is a minimum of 0.4 unit intervals (UI).

Receiver Configuration Modes

Clock/Data Recovery Mode (CDR)

The clock/data recovery function in the receive path is selectable via the CDR bit (register 5, bit 0). If CDR = 1, the clock and data recovery function is enabled and provides a recovered clock (RCLK) with retimed data (RPD/RDATA, RND). If CDR = 0, the clock and data recovery function is disabled, and the RZ data from the slicers is provided over RPD and RND to the system. In this mode, ALOS is available on the RCLK/ALOS pins, and downstream functions selected by microprocessor register 5 (JAR, ACM, LOSSD) are ignored.

Zero Substitution Decoding (CODE)

When single-rail operation is selected with DUAL = 0 (register 5, bit 4), the B8ZS zero substitution decoding can be selected via the CODE bit (register 5, bit 3). If CODE = 1, the B8ZS decoding function is enabled in the receive path and decoded receive data and code violations appear on the RDATA and BPV pins, respectively. If CODE = 0, receive data and any bipolar violations (such as two consecutive 1s of the same polarity) appear on the RDATA and BPV pins, respectively.

Alternate Logic Mode (ALM)

The alternate logic mode (ALM) control bit (register 5, bit 5) selects the receive and transmit data polarity (i.e., active-high vs. active-low). If ALM = 0, the receiver circuitry (and transmit input) assumes the data to be active-low polarity. If ALM = 1, the receiver circuitry (and transmit input) assumes the data to be active-high polarity. The ALM control is used in conjunction with the ACM control (register 5, bit 6) to determine the receive data retiming mode.

Receiver (continued)

Receiver Configuration Modes (continued)

Alternate Clock Mode (ACM)

The alternate clock mode (ACM) control bit (register 5, bit 6) selects the positive or negative clock edge of the receive clock (RCLK) for receive data retiming. The ACM control is used in conjunction with ALM (register 5, bit 5) control to determine the receive data retiming modes. If ACM = 1, the receive data is retimed on the positive edge of the receive clock. If ACM = 0, the receive data is retimed on the negative edge of the receive clock. Note that this control does not affect the timing relationship for the transmitter inputs.

Loss Shut Down (LOSSD)

The loss shut down (LOSSD) control bit (register 5, bit 7) places the digital receiver outputs (RPD, RND) in a predetermined state when a digital loss of signal (DLOS) alarm occurs in register 0 and 1, bits 1 and 5. If LOSSD = 1, the RPD and RND outputs are forced to their inactive states (selected by ALM) and the receive clock (RCLK) free runs during a DLOS alarm condition. If LOSSD = 0, the RPD, RND, and RCLK outputs will remain unaffected during the DLOS alarm condition.

Receiver Alarms

Analog Loss of Signal (ALOS) Alarm

An analog loss of signal (ALOS) detector monitors the incoming signal amplitude and reports its status to the alarm registers 0 and 1. During DS1 operation, analog loss of signal is indicated (ALOS = 1) if the amplitude at the receive input drops below a voltage that is 17 dB below the nominal pulse amplitude. The slicer outputs are clamped to the inactive state, and the clock recovery will provide a free-running RCLK when ALOS = 1. The alarm circuitry also provides 4 dB of hysteresis to eliminate ALOS chattering. The time required to detect ALOS is between 1 ms and 2.6 ms and is timed by the blue clock (see the All Ones (AIS, Blue Signal) Generator (TBS) section). Detection time is independent of signal amplitude before the loss condition occurs.

Digital Loss of Signal (DLOS) Alarm

A digital loss of signal (DLOS) detector guarantees the quality of the signal as defined in standards documents, and reports its status to the alarm registers 0 and 1. Digital loss of signal (DLOS = 1) is indicated if 100 or more consecutive 0s occur in the receive data stream. The DLOS indication is deactivated when the average ones density of at least 12.5% is received in 100 contiguous pulse positions. The LOSSTD control bit (register 4, bit 2) selects the conformance protocols for DLOS per Table 3. TR-TSY-000009 adds the additional constraint of no more than 15 consecutive 0s when determining the 12.5% 1's density.

Table 3. Digital Loss of Signal Standard Select

LOSSTD	DS1 Mode
0	T1M1.3/93-005 ITU-T G.775
1	TR-TSY-000009

Bipolar Violation (BPV) Alarm

The bipolar violation (BPV) alarm is used only in single-rail mode of operation of the device (see the System Interface Pin Options section). When B8ZS(DS1) coding is not used (i.e., CODE = 0), any violations in the receive data (such as two or more consecutive 1s on a rail) are indicated on the RND/BPV pins. When B8ZS(DS1) coding is used (i.e., CODE = 1), the B8ZS code violations are reflected on the RND/BPV pins.

Receiver (continued)

DS1 Receiver Specifications

During DS1 operation, the receiver will perform as specified in Table 4.

Table 4. DS1 Receiver Specifications

Parameter	Min	Typ	Max	Unit	Specification
Analog Loss of Signal:					
Threshold	20	17	—	dB*	—
Hysteresis	—	4	—	dB	—
Maximum Sensitivity†	11	15	—	dB	—
Jitter Transfer:					TR-TSY-000499
3 dB Bandwidth	—	3.84	—	kHz	
Peaking	—	—	0.1	dB	
Generated Jitter	—	0.032	0.04	UI_{pk-pk}	TR-TSY-000499, ITU-T G.824
Jitter Tolerance	—	—	—	—	ITU-T G.823-4, TR-TSY-000009, TR-TSY-000499, TR-TSY-000170
Return Loss‡:					
51 kHz to 102 kHz	14	—	—	dB	—
102 kHz to 1.544 MHz	20	—	—	dB	—
1.544 MHz to 2.316 MHz	16	—	—	dB	—
Digital Loss of Signal:					
Flag Asserted, Consecutive Bit Positions	100	—	—	zeros	—
Flag Deasserted					
Data Density	12.5	—	—	% ones	—
Maximum Consecutive	—	—	15	zeros	TR-TSY-000009
Zeros	—	—	99	zeros	ITU-T G.775, T1M1.3/93-005

* Below the nominal pulse amplitude of 3.0 V using external line interface circuitry described in Figure 12 and Table 21.
† Amount of cable loss.
‡ Using external line interface circuitry described in Figure 12 and Table 21.

Transmitter

Output Pulse Generation

The transmitter accepts a clock with NRZ data in single-rail mode (DUAL = 0: register 5, bit 4) or positive and negative NRZ data in dual-rail mode (DUAL = 1) from the system. The device converts this data to a balanced bipolar signal (AMI format) with optional B8ZS(DS1) encoding and jitter attenuation. Low-impedance output drivers produce these pulses on the line interface. Positive 1s are output as a positive pulse on TTIP, and negative 1s are output as a positive pulse on TRING. Binary 0s are converted to null pulses. The total delay of the data from the system interface to the transmit driver is approximately 3 to 11 bit periods, depending on the CODE (register 5, bit 3) configuration.

Additional delay results if the jitter attenuator is selected for use in the transmit path (see the Data Delay section).

Transmit pulse shaping is controlled by the on-chip pulse-width controller and pulse equalizer. The pulse-width controller produces the high-speed timing signals to accurately control the transmit pulse widths. This eliminates the need for a tightly controlled transmit clock duty cycle that is usually required in discrete implementations. The pulse equalizer controls the amplitudes of these pulse shapes. Different pulse equalizations are selected through proper settings of EQA, EQB, and EQC (registers 6 to 9, bits 5 to 7) as described in Table 5.

Table 5. Equalizer/Rate Control

EQA*	EQB*	EQC*	Service	Clock Rate	Transmitter Equalization†		Maximum Cable Loss‡
					Feet	Meters	dB
0	0	0	DS1	1.544 MHz	0 ft. to 131 ft.	0 m to 40 m	0.6
0	0	1			131 ft. to 262 ft.	40 m to 80 m	1.2
0	1	0			262 ft. to 393 ft.	80 m to 120 m	1.8
0	1	1			393 ft. to 524 ft.	120 m to 160 m	2.4
1	0	0			524 ft. to 655 ft.	160 m to 200 m	3.0

* Other logical settings of EQA, EQB, and EQC should not be used.
† In DS1 mode, the distance to the DSX for 22 gauge PIC (ABAM) cable is specified. Use the maximum cable loss figures for other cable types.
‡ Loss measured at 772 kHz.

Jitter

The intrinsic jitter of the transmit path, i.e., the jitter at TTIP/TRING when no jitter is applied to TCLK (and the jitter attenuator is not selected, JAT = 0), is typically 5 $ns_{pk\text{-}pk}$ and will not exceed 0.02 $UI_{pk\text{-}pk}$.

Transmitter (continued)

Transmitter Configuration Modes

Zero Substitution Encoding/Decoding (CODE)

Zero substitution encoding/decoding (B8ZS) can be activated only in the single-rail system interface mode (DUAL = 0) by setting CODE = 1 (register 5, bit 3). Data received from the line interface on RTIP and RRING will be B8ZS decoded before appearing on RDATA (pins 14, 38, 64, 88) at the system interface. Likewise, data transmitted from the system interface on TDATA (pins 17, 35, 67, 85) will be B8ZS encoded before appearing on TTIP and TRING at the line interface. This mode also allows coding violations, such as receiving two consecutive 1s of the same polarity from the line interface, to be output on BPV (pins 13, 39, 63, 89).

All Ones (AIS, Blue Signal) Generator (TBS)

When the transmit blue signal control is set (TBS = 1) for a given channel (registers 6 to 9, bit 2), a continuous stream of bipolar 1s is transmitted to the line interface (AIS). The TPD/TDATA and TND inputs are ignored during this mode. The TBS input is ignored when a remote loopback (RLOOP) is selected using loopback control bits LOOPA and LOOPB (registers 6 to 9, bits 3 and 4). (See the Loopbacks section.)

To maintain application flexibility, the clock source used for the blue signal is selected by configuring BCLK (pin 30). If a data rate clock is input on the BCLK pin, it will be used to transmit the blue signal. If BCLK = 0, then TCLK is used to transmit the blue signal (the smoothed clock from the jitter attenuator is used if JAT = 1 is selected). If BCLK = 1, then XCLK (after being divided by a factor of 16) is used to transmit the blue signal. After BCLK is established, a minimum of 16 μs is required for the device to properly select the clock. For any of the above options, the clock tolerance must meet the normal line transmission rate (DS1 1.544 MHz ± 32 ppm).

Transmitter Alarms

Loss of Transmit Clock (LOTC) Alarm

A loss of transmit clock alarm (LOTC = 1) is indicated if any of the clocks in the transmit path disappear (registers 0 and 1, bits 3 and 7). This includes loss of TCLK input, loss of RCLK during remote loopback, loss of jitter attenuator output clock (when enabled), or the loss of clock from the pulse-width controller.

For all of these conditions, a core transmitter timing clock is lost and no data can be driven onto the line. Output drivers TTIP and TRING are placed in a high-impedance state when this alarm condition is active. The LOTC interrupt is asserted between 3 μs and 16 μs after the clock disappears, and deasserts immediately after detecting the first clock edge.

Transmit Driver Monitor (TDM) Alarm

The transmit driver monitor detects two conditions: a nonfunctional link due to faults on the primary of the transmit transformer, and periods of no data transmission. The TDM alarm (registers 0 and 1, bits 2 and 6) is the ORed function of both faults and provides information about the integrity of the transmit signal path.

The first monitoring function is provided to detect nonfunctional links and protect the device from damage. The alarm is set (TDM = 1) when one of the transmitter's line drivers (TTIP or TRING) is shorted to power supply or ground, or TTIP and TRING are shorted together. Under these conditions, internal circuitry protects the device from damage and excessive power supply current consumption by 3-stating the output drivers. The monitor detects faults on the transformer primary, but transformer secondary faults may not be detected. The monitor operates by comparing the line pulses with the transmit inputs as in a bit error detect mode. After 32 transmit clock cycles, the transmitter is powered up in its normal operating mode. The drivers attempt to correctly transmit the next data bit. If the error persists, TDM remains active to eliminate alarm chatter and the transmitter is internally protected for another 32 transmit clock cycles. This process is repeated until the error condition is removed and the TDM alarm is deactivated.

The second monitoring function is to indicate periods of no data transmission. The alarm is set (TDM = 1) when 32 consecutive zeros have been transmitted and is cleared on the detection of a single pulse. This alarm condition does not alter the state or functionality of the signal path.

Transmitter (continued)

DS1 Transmitter Pulse Template and Specifications

The DS1 pulse shape template is specified at the DSX (defined by CB119 and ANSI T1.102) and is illustrated in Figure 3. The device also meets the pulse template specified by ITU-T G.703 (not shown).

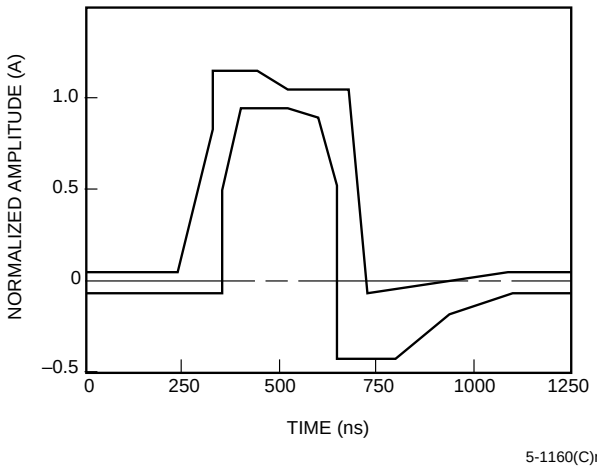


Figure 3. DSX-1 Isolated Pulse Template

Table 6. DSX-1 Pulse Template Corner Points (from CB119)

Maximum Curve		Minimum Curve	
ns	V	ns	V
0	0.05	0	–0.05
250	0.05	350	–0.05
325	0.80	350	0.50
325	1.15	400	0.95
425	1.15	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
725	–0.07	650	–0.45
1100	0.05	800	–0.45
1250	0.05	925	–0.20
		1100	–0.05
		1250	–0.05

During DS1 operation, the transmitter tip/ring (TTIP/TRING pins) will perform as specified in Table 7.

Table 7. DS1 Transmitter Specifications

Parameter	Min	Typ	Max	Unit	Specification
Output Pulse Amplitude at DSX*	2.5	2.8	3.5	V	AT&T CB119, ANSI T1.102
Output Pulse Width	338	350	362	ns	
Positive/Negative Pulse Imbalance†	—	0.1	0.4	dB	
Power Levels:‡					
772 kHz	12.6	—	17.9	dBm	
1.544 MHz§	29	39	—	dB	

* In accordance with the interfaces described in the Absolute Maximum Ratings section and the Handling Precautions section, measured at the transformer secondary.
† Total power difference.
‡ Measured in a 2 kHz band around the specified frequency.
§ Below the power at 772 kHz.

Jitter Attenuator

The selectable jitter attenuator is provided for narrow-bandwidth jitter transfer function applications. The selection is done via control bits which are global and affect all four channels. One application is to provide narrow-bandwidth jitter filtering for line-synchronization in the receive path. Another use of the jitter attenuator is to provide clock smoothing in the transmit signaling path for applications such as synchronous/asynchronous demultiplexers. In these applications, TCLK will have an instantaneous frequency that is higher than the data rate and periods of TCLK are suppressed (gapped) in order to set the average long-term TCLK frequency to within the transmit line rate specification.

The jitter attenuator does not degrade the jitter specifications of the receiver clock/data recovery circuit. In addition, the jitter attenuator must meet the specifications for narrow-bandwidth applications as listed in Table 8.

Table 8. List of Low Bandwidth Jitter Specification Documents

Application
DS1
TR-TSY-000009 TR-TSY-000253 TR-TSY-000499

Data Delay

Providing narrow-bandwidth jitter filtering requires data buffering to increase the data delay through the jitter attenuator. The nominal data delay for the jitter attenuator is 33 bit periods, with a maximum data delay of 66 bit periods. This delay is dependent on the input clock frequency, XCLK frequency, input jitter, and gapped clock patterns.

Generated (Intrinsic) Jitter

Generated jitter is the amount of jitter appearing on the output port when the applied input signal has no jitter. The jitter attenuator of this device outputs a maximum of 0.04 U.I. peak-to-peak intrinsic jitter.

Jitter Transfer Function

The jitter transfer function describes the amount of jitter in specific equipment that is transferred from the input to the output over a frequency range. The jitter attenuator exhibits a single-pole rolloff (20 dB/decade) jitter transfer characteristic that has no peaking and a nominal filter corner frequency (3 dB bandwidth) for DS1 operation of less than 10 Hz. For a given frequency, different jitter amplitudes will cause slight variations in attenuation because of finite quantization effects. Jitter amplitudes of less than approximately 0.2 U.I. will have greater attenuation than the single-pole rolloff characteristic.

Measurement of the jitter transfer function involves stimulating the circuit with a sinusoidal jitter test signal. The difference between the output signal power and the test signal power, at a given frequency, is the jitter transfer. When output signal power is below the noise floor, it cannot be measured. Halting the jitter transfer function measurements because of noise floor limitations is acceptable during conformance testing.

Jitter Tolerance

The minimum jitter tolerance of the jitter attenuator occurs when the XCLK frequency and the long-term average frequency of the input clock are at their extreme frequency tolerances. The minimum tolerance is 28 U.I. peak-to-peak at the highest jitter frequency of 15 kHz.

Jitter Attenuator Enable

The jitter attenuator is selected using the JAR and JAT bits (register 5, bits 1 and 2) of the microprocessor interface. These control bits are global and affect all four channels unless a given channel is in the power-down mode (PWRDN = 1). Because there is only one attenuator function in the device, selection must be made between either the transmit or receive path. If both JAT and JAR are activated at the same time, the jitter attenuator will be disabled. Note that the power consumption increases slightly on a per-channel basis when the jitter attenuator is active, as described in Table 26. If jitter attenuation is selected, a valid XCLK (pin 29) signal must be available.

Jitter Attenuator (continued)

Jitter Attenuator Enable (continued)

Jitter Attenuator Receive Path Enable (JAR)

When the jitter attenuator receive bit is set (JAR = 1), the attenuator is enabled in the receive data path between the clock/data recovery and the decoder (see Figure 1). Under this condition, the jitter characteristics of the jitter attenuator apply for the receiver. When JAR = 0, the clock/data recovery outputs bypass the disabled attenuator and directly enter the decoder function. The receive path will then exhibit the jitter characteristics of the clock recovery function as described in the Jitter section. If CDR = 0 (register 5, bit 0), the JAR bit is ignored because clock recovery will be disabled.

Jitter Attenuator Transmit Path Enable (JAT)

When the jitter attenuator transmit bit is set (JAT = 1), the attenuator is enabled in the transmit data path between the encoder and the pulse-width controller/pulse equalizer (see Figure 1). Under this condition, the jitter characteristics of the jitter attenuator apply for the transmitter. When JAT = 0, the encoder outputs bypass the disabled attenuator and directly enter the pulse-width controller/pulse equalizer. The transmit path will then pass all jitter from TCLK to line interface outputs TTIP/TRING.

Loopbacks

The device has three independent loopback paths that are activated using LOOPA and LOOPB (registers 6 to 9, bits 3 and 4) as shown in Table 9. The locations of these loopbacks are illustrated in Figure 1.

Table 9. Loopback Control

Operation	Symbol	LOOPA	LOOPB
Normal	—	0	0
Full Local Loopback	FLLOOP*	0	1
Remote Loopback	RLOOP†	1	0
Digital Local Loopback	DLLOOP	1	1

* During the transmit blue signal condition, the looped data will be the transmitted data from the system and not the all-1s signal.
† Transmit blue signal request is ignored.

Full Local Loopback (FLLOOP)

A full local loopback (FLLOOP) connects the transmit line driver input to the receiver analog front-end circuitry. Valid transmit output data continues to be sent to the network. If the transmit blue signal (all-1s signal) is sent to the network, the looped data is not affected. The ALOS alarm continues to monitor the receive line interface signal while DLOS monitors the looped data.

Remote Loopback (RLOOP)

A remote loopback (RLOOP) connects the recovered clock and retimed data to the transmitter at the system interface and sends the data back to the line. The receiver front end, clock/data recovery, encoder/decoder (if enabled) jitter attenuator (if enabled), and transmit driver circuitry are all exercised during this loopback. The transmit clock, transmit data, and TBS inputs are ignored. Valid receive output data continues to be sent to the system interface. This loopback mode is very useful for isolating failures between systems.

Digital Local Loopback (DLLOOP)

A digital local loopback (DLLOOP) connects the transmit clock and data through the encoder/decoder pair to the receive clock and data output pins at the system interface. This loopback is operational if the encoder/decoder pair is enabled or disabled. The blue signal can be transmitted without any effect on the looped signal.

Other Features

Powerdown (PWRDN)

Each line interface channel has an independent powerdown mode controlled by PWRDN (registers 6 to 9, bit 0). This provides power savings for systems that use backup channels. If PWRDN = 1, the corresponding channel will be in a standby mode, consuming only a small amount of power. It is recommended that the alarm registers for the corresponding channel be masked with MASK = 1 (registers 6 to 9, bit 1) during powerdown mode. If a line interface channel in powerdown mode needs to be placed into service, the channel should be turned on (PWRDN = 0) approximately 5 ms before data is applied.

If a line interface channel will never be in service, the V_{DDA} and V_{DDD} pins can be connected to the ground plane, resulting in no power consumption.

RESET ($\overline{\text{RESET}}$, SWRESET)

The device provides both a hardware reset ($\overline{\text{RESET}}$; pin 32) and a software reset (SWRESET; register 4, bit 1) that are functionally equivalent. When the device is in reset, all signal-path and alarm monitor states are initialized to a known starting configuration. The status registers and INT (pin 25) are also cleared. The writable microprocessor interface registers are not affected by reset, with the exception of bits in register 4 (see the Global Control Register Overview (0100, 0101) section). During a reset condition, data transmission will be momentarily interrupted and the device will respond to those register bits affected by the reset. On powerup of the device, the software reset bit (register 4, bit 1) is not initialized. It must be written to a zero prior to writing the other bits in register 4.

The reset condition is initiated by setting $\overline{\text{RESET}}$ = 0 or SWRESET = 1 for a minimum of 10 µs. After leaving the reset condition (with $\overline{\text{RESET}}$ = 1 or SWRESET = 0), only the bits in register 4 need to be restored.

Loss of XCLK Reference Clock (LOXC)

The LOXC output (pin 31) is active when the XCLK reference clock (pin 29) is absent. The LOXC flag is asserted between 150 ns and 700 ns after XCLK disappears, and deasserts immediately after detecting the first clock edge of XCLK.

During the LOXC alarm condition, the clock recovery and jitter attenuator functions are automatically disabled. Therefore, if CDR = 1 and/or JAR = 1, the RCLK, RPD, RND, and DLOS outputs will be unknown. If CDR = 0, there will be no effect on the receiver. If the jitter attenuator is enabled in the transmit path (JAT = 1) during this alarm condition, then LOTC = 1 will also be indicated.

In-Circuit Testing and Driver 3-State ($\overline{\text{ICT}}$)

The function of the $\overline{\text{ICT}}$ input (pin 33) is determined by the ICTMODE bit (register 4, bit 3). If ICTMODE = 0 and $\overline{\text{ICT}}$ is activated ($\overline{\text{ICT}}$ = 0), then all output buffers (TTIP, TRING, RCLK, RPD, RND, LOXC, RDY_$\overline{\text{DTACK}}$, INT, AD[7:0]) are placed in a high-impedance state. For in-circuit testing, the $\overline{\text{RESET}}$ pin can be used to activate ICTMODE = 0 without having to write the bit. If ICTMODE = 1 and $\overline{\text{ICT}}$ = 0, then only the TTIP and TRING outputs of all channels will be placed in a high-impedance state. The TTIP and TRING outputs have a limiting high-impedance capability of approximately 8 kΩ.

Microprocessor Interface

Overview

The device is equipped with a microprocessor interface that can operate with most commercially available microprocessors. Inputs MPMUX and MPMODE (pins 20 and 21) are used to configure this interface into one of four possible modes, as shown in Table 10. The MPMUX setting selects either a multiplexed 8-bit address/data bus (AD[7:0]) or a demultiplexed 4-bit address bus (A[3:0]) and an 8-bit data bus (AD[7:0]). The MPMODE setting selects the associated set of control signals required to access a set of registers within the device.

When the microprocessor interface is configured to operate in the multiplexed address/data bus modes (MPMUX = 1), the user has access to an internal chip select function that allows the microprocessor to selectively read/write a specific T7689 in a multiple T7689 environment (see the Internal Chip Select Function section).

The microprocessor interface can operate at speeds up to 16.384 MHz in interrupt-driven or polled mode without requiring any wait-states. For microprocessors operating at greater than 16.384 MHz, the RDY_$\overline{\text{DTACK}}$ output is used to introduce wait-states in the read/write cycles.

In the interrupt-driven mode, one or more device alarms will assert the active-high INT output (pin 25) once per alarm activation. After the microprocessor reads the alarm status registers, the INT output will deassert. In the polled mode, however, the microprocessor monitors the various device alarm status by periodically reading the alarm status registers without the use of INT (pin 25). In both interrupt and polled methods of alarm servicing, the status register will clear on a microprocessor read cycle only when the alarm condition within the signaling channel no longer exists; otherwise, the register bit remains set.

Due to the device flexibility, there are no default power-up or reset states, except for register 4. All read/write registers must be written by the microprocessor on system start-up to guarantee proper device functionality.

Details concerning microprocessor interface configuration modes, pinout definitions, clock specifications, register bank architecture, and the I/O timing specifications and diagrams are described in the following sections.

Microprocessor Configuration Modes

Table 10 highlights the four microprocessor modes controlled by the MPMUX and MPMODE inputs (pins 20 and 21).

Table 10. Microprocessor Configuration Modes

Mode	MPMODE	MPMUX	Address/Data Bus	Generic Control, Data, and Output Pin Names
MODE1	0	0	DEMUXed	$\overline{\text{CS}}$, $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, A[3:0], AD[7:0], INT, $\overline{\text{DTACK}}$
MODE2	0	1	MUXed	$\overline{\text{CS}}$, $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, AD[7:0], INT, $\overline{\text{DTACK}}$
MODE3	1	0	DEMUXed	$\overline{\text{CS}}$, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A[3:0], AD[7:0], INT, RDY
MODE4	1	1	MUXed	$\overline{\text{CS}}$, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD[7:0], INT, RDY

Microprocessor Interface (continued)

Microprocessor Interface Pinout Definitions

The MODE1 through MODE4 specific pin definitions are given in Table 11. Note that the microprocessor interface uses the same set of pins in all modes.

Table 11. MODE [1—4] Microprocessor Pin Definitions

Configuration	Pin Number	Device Pin Name	Generic Pin Name	Pin_Type	Assertion Sense	Function
MODE1	19	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	I	Active-Low	Data Strobe
	22	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	I	—	Read/Write $R/\overline{W}$ = 1 => Read $R/\overline{W}$ = 0 => Write
	23	ALE_$\overline{AS}$	$\overline{AS}$	I	—	Address Strobe
	24	$\overline{CS}$	$\overline{CS}$	I	Active-Low	Chip Select
	25	INT	INT	O	Active-High	Interrupt
	26	RDY_$\overline{DTACK}$	$\overline{DTACK}$	O	Active-Low	Data Acknowledge
	69—76	AD[7:0]	AD[7:0]	I/O	—	Data Bus
	79—82	A[3:0]	A[3:0]	I	—	Address Bus
	83	MPCLK	MPCLK	I	—	Microprocessor Clock
MODE2	19	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	I	Active-Low	Data Strobe
	22	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	I	—	Read/Write $R/\overline{W}$ = 1 => Read $R/\overline{W}$ = 0 => Write
	23	ALE_$\overline{AS}$	$\overline{AS}$	I	—	Address Strobe
	24	$\overline{CS}$	$\overline{CS}$	I	Active-Low	Chip Select
	25	INT	INT	O	Active-High	Interrupt
	26	RDY_$\overline{DTACK}$	$\overline{DTACK}$	O	Active-Low	Data Acknowledge
	69—76	AD[7:0]	AD[7:0]	I/O	—	Address/Data Bus
	83	MPCLK	MPCLK	I	—	Microprocessor Clock
MODE3	19	$\overline{WR}\_\overline{DS}$	$\overline{WR}$	I	Active-Low	Write
	22	$\overline{RD}\_R/\overline{W}$	$\overline{RD}$	I	Active-Low	Read
	23	ALE_$\overline{AS}$	ALE	I	—	Address Latch Enable
	24	$\overline{CS}$	$\overline{CS}$	I	Active-Low	Chip Select
	25	INT	INT	O	Active-High	Interrupt
	26	RDY_$\overline{DTACK}$	RDY	O	Active-High	Ready
	69—76	AD[7:0]	AD[7:0]	I/O	—	Data Bus
	79—82	A[3:0]	A[3:0]	I	—	Address Bus
	83	MPCLK	MPCLK	I	—	Microprocessor Clock
MODE4	19	$\overline{WR}\_\overline{DS}$	$\overline{WR}$	I	Active-Low	Write
	22	$\overline{RD}\_R/\overline{W}$	$\overline{RD}$	I	Active-Low	Read
	23	ALE_$\overline{AS}$	ALE	I	—	Address Latch Enable
	24	$\overline{CS}$	$\overline{CS}$	I	Active-Low	Chip Select
	25	INT	INT	O	Active-High	Interrupt
	26	RDY_$\overline{DTACK}$	RDY	O	Active-High	Ready
	69—76	AD[7:0]	AD[7:0]	I/O	—	Address/Data Bus
	83	MPCLK	MPCLK	I	—	Microprocessor Clock

Microprocessor Interface (continued)

Microprocessor Clock (MPCLK) Specifications

The microprocessor interface is designed to operate at clock speeds up to 16.384 MHz without requiring any wait-states. Wait-states may be needed if higher microprocessor clock speeds are required. The microprocessor clock (MPCLK, pin 83) specification is shown in Table 12. This clock must be supplied only if the RDY_$\overline{\text{DTACK}}$ and INT outputs are required to be synchronous to MPCLK. Otherwise, the MPCLK pin must be connected to ground (GND_D).

Table 12. Microprocessor Input Clock Specifications

Name	Symbol	Period and Tolerance	T_{rise} Typ	T_{fall} Typ	Duty Cycle		Unit
					Min High	Min Low	
MPCLK	t1	61 to 323	5	5	27	27	ns

Internal Chip Select Function

When the microprocessor interface is configured to operate in the multiplexed address/data bus modes (MPUX = 1), the user has access to an internal chip select function. This function allows a microprocessor to selectively read or write a specific quad line interface device in a system of up to eight devices on the microprocessor bus. Externally tying $\overline{\text{CS}}$ = 0 (pin 24) and A3 = 1 (pin 79) on every line interface device enables the internal chip select function. Individual device addresses are established by externally connecting the other three address pins A[2:0] to a unique address value in the range of 000 through 111. In order for a line interface device to respond to the register read or write request from the microprocessor, the address data bus AD[6:4] (pins 70, 71, 72) must match the specific address defined on A[2:0]. If $\overline{\text{CS}}$ and A3 pins are tied low, the internal chip select function is disabled and all line interface devices will respond to a microprocessor write request. However, if $\overline{\text{CS}}$ = 1, none of the line interface devices will respond to the microprocessor read/write request.

Microprocessor Interface Register Architecture

The register bank architecture of the microprocessor interface is shown in Table 13. The register bank consists of sixteen 8-bit registers classified as alarm registers, global control registers, and channel configuration/maintenance registers. Registers 0 and 1 are the alarm registers used for storing the various device alarm status and are read-only. All other registers are read/write. Registers 2 and 3 contain the individual mask bits for the alarms in registers 0 and 1. Registers 4 and 5 are designated as the global control registers used to set up the functions for all four channels. The channel configuration registers in registers 6 through 9 are used to configure the individual channel functions and parameters. Registers 10 and 11 must be cleared by the user after a powerup for proper device operation. Registers 12 through 15 are reserved for proprietary functions and must not be addressed during operation. The following sections describe these registers in detail.

Microprocessor Interface (continued)

Microprocessor Interface Register Architecture (continued)

Table 13. Register Set

Designation	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Alarm Registers (Read Only)									
0	0000	LOTC2	TDM2	DLOS2	ALOS2	LOTC1	TDM1	DLOS1	ALOS1
1	0001	LOTC4	TDM4	DLOS4	ALOS4	LOTC3	TDM3	DLOS3	ALOS3
Alarm Mask Registers (Read/Write)									
2	0010	MLOTC2	MTDM2	MDLOS2	MALOS2	MLOTC1	MTDM1	MDLOS1	MALOS1
3	0011	MLOTC4	MTDM4	MDLOS4	MALOS4	MLOTC3	MTDM3	MDLOS3	MALOS3
Global Control Registers (Read/Write)									
4	0100	HIGHZ4 (1)	HIGHZ3 (1)	HIGHZ2 (1)	HIGHZ1 (1)	ICTMODE (0)	LOSSTD	SWRESET	GMASK (1)
5	0101	LOSSD	ACM	ALM	DUAL	CODE	JAT	JAR	CDR
Channel Configuration Registers (Read/Write)									
6	0110	EQA1	EQB1	EQC1	LOOPA1	LOOPB1	TBS1	MASK1	PWRDN1
7	0111	EQA2	EQB2	EQC2	LOOPA2	LOOPB2	TBS2	MASK2	PWRDN2
8	1000	EQA3	EQB3	EQC3	LOOPA3	LOOPB3	TBS3	MASK3	PWRDN3
9	1001	EQA4	EQB4	EQC4	LOOPA4	LOOPB4	TBS4	MASK4	PWRDN4
10	1010	0	0	0	0	0	0	0	0
11	1011	0	0	0	0	0	0	0	0
12—15	1100—1111	RESERVED							

Notes:
A numerical suffix appended to the bit name identifies the channel number.

Bits shown in parentheses indicate the state forced during a reset condition.

All registers must be configured by the user before the device can operate as required for the particular application.

Registers 10 and 11 MUST be written to zero after powerup of the device.

It is recommended that registers 12—15 should be written to 0 after powerup of the device.

Microprocessor Interface (continued)

Microprocessor Interface Register Architecture (continued)

Alarm Register Overview (0000, 0001)

The bits in the alarm registers represent the status of the transmitter and receiver alarms LOTC, TDM, DLOS, and ALOS for all four channels as shown in Table 14. The alarm indicators are active-high and automatically clear on a microprocessor read if the corresponding alarm condition no longer exists. Persistent alarm conditions will cause the bit to remain set. These are read-only registers.

Table 14. Alarm Registers

Bits	Symbol*	Description
Alarm Register (0)		
0, 4	ALOS[1:2]	Analog loss of signal alarm for channels 1 & 2.
1, 5	DLOS[1:2]	Digital loss of signal alarm for channels 1 & 2.
2, 6	TDM[1:2]	Transmit driver monitor alarm for channels 1 & 2.
3, 7	LOTC[1:2]	Loss of transmit clock alarm for channels 1 & 2.
Alarm Register (1)		
0, 4	ALOS[3:4]	Analog loss of signal alarm for channels 3 & 4.
1, 5	DLOS[3:4]	Digital loss of signal alarm for channels 3 & 4.
2, 6	TDM[3:4]	Transmit driver monitor alarm for channels 3 & 4.
3, 7	LOTC[3:4]	Loss of transmit clock alarm for channels 3 & 4.

* The numerical suffix identifies the channel number.

Alarm Mask Register Overview (0010, 0011)

The bits in the alarm mask registers in Table 15 allow the microprocessor to selectively mask each channel alarm and prevent it from generating an interrupt. The mask bits correspond to the alarm status bits in the alarm registers and are active-high to disable the corresponding alarm from generating an interrupt. These registers are read/write registers.

Table 15. Alarm Mask Registers

Bits	Symbol*	Description
Alarm Mask Register (2)		
0, 4	MALOS[1:2]	Mask analog loss of signal alarm for channels 1 & 2.
1, 5	MDLOS[1:2]	Mask digital loss of signal alarm for channels 1 & 2.
2, 6	MTDM[1:2]	Mask transmit driver monitor alarm for channels 1 & 2.
3, 7	MLOTC[1:2]	Mask loss of transmit clock alarm for channels 1 & 2.
Alarm Mask Register (3)		
0, 4	MALOS[3:4]	Mask analog loss of signal alarm for channels 3 & 4.
1, 5	MDLOS[3:4]	Mask digital loss of signal alarm for channels 3 & 4.
2, 6	MTDM[3:4]	Mask transmit driver monitor alarm for channels 3 & 4.
3, 7	MLOTC[3:4]	Mask loss of transmit clock alarm for channels 3 & 4.

* The numerical suffix identifies the channel number.

Microprocessor Interface (continued)

Microprocessor Interface Register Architecture (continued)

Global Control Register Overview (0100, 0101)

The bits in the global control registers in Table 16 and Table 17 allow the microprocessor to configure the various device functions over all the four channels. All the control bits (with the exception of LOSSTD and ICTMODE) are active-high. These are read/write registers.

Table 16. Global Control Register (0100)

Bits	Symbol	Description
Global Control Register (4)		
0	GMASK	The GMASK bit globally masks all the channel alarms when GMASK = 1, preventing all the receiver and transmitter alarms from generating an interrupt. GMASK = 1 after a device reset.
1	SWRESET	The SWRESET provides the same function as the hardware reset. It is used for device initialization through the microprocessor interface. The software reset bit does not have a powerup default state; therefore, the first write to the device must clear this bit.
2	LOSSTD	The LOSSTD bit selects the conformance protocol for the DLOS receiver alarm function.
3	ICTMODE	The ICTMODE bit changes the function of the $\overline{\text{ICT}}$ pin. ICTMODE = 0 after a device reset.
4—7	HIGHZ[1:4]	A HIGHZ bit is available for each individual channel. When HIGHZ = 1, the TTIP and TRING transmit drivers for the specified channel are placed in a high-impedance state. HIGHZ[1:4] = 1 after a device reset.

Table 17. Global Control Register (0101)

Bits	Symbol	Description
Global Control Register (5)		
0	CDR	The CDR bit is used to enable and disable the clock/data recovery function.
1	JAR	The JAR is used to enable and disable the jitter attenuator function in the receive path. The JAR and JAT control bits are mutually exclusive; i.e., either JAR or the JAT control bit can be set, but not both.
2	JAT	The JAT is used to enable and disable the jitter attenuator function in the transmit path. The JAT and JAR control bits are mutually exclusive; i.e., either JAT or the JAR control bit should be set, but not both.
3	CODE	The CODE bit is used to enable and disable the B8ZS/HDB3 zero substitution coding (decoding) in the transmit (receive) path. It is used in conjunction with the DUAL bit and is valid only for single-rail operation.
4	DUAL	The DUAL bit is used to select single or dual-rail mode of operation.
5	ALM	The ALM bit selects the transmit and receive data polarity (i.e., active-low or active-high). The ALM and ACM bits are used together to determine the transmit and receive data retiming modes.
6	ACM	The ACM bit selects the positive or negative edge of the receive clock (RCLK[1:4]) for receive data retiming. The ACM and ALM bits are used together to determine the transmit and receive data retiming modes.
7	LOSSD	The LOSSD bit selects the shutdown function for the digital loss of signal alarm (DLOS).

Microprocessor Interface (continued)

Microprocessor Interface Register Architecture (continued)

Channel Configuration Register Overview (0110—1001)

The control bits in the channel configuration registers in Table 18 are used to select equalization, loopbacks, AIS generation, channel alarm masking, and the channel powerdown mode for each channel (1—4). The PWRDN[1—4], MASK[1—4], and TBS[1—4] bits are active-high. These are read/write registers.

Table 18. Channel Configuration Registers

Bits	Symbol*	Description†
Channel Configuration Registers (6—9)		
0	PWRDN[1:4]	The PWRDN bit powers down a channel when not used.
1	MASK[1:4]	The MASK bit masks all interrupts for the channel.
2	TBS[1:4]	The TBS bit enables transmission of an all 1s signal to the line interface.
3, 4	LOOPB[1:4], LOOPA[1:4]	The LOOPB and LOOPA bits select the channel loopback modes.
5, 6, 7	EQC[1:4], EQB[1:4], EQA[1:4]	The EQC, EQB, and EQA bits select the associated transmitter cable equalization/termination impedances.

* A numerical suffix identifies the channel number.
† Channel suffix not shown in the description.

Other Registers

The software reset bit must be cleared after powerup prior to writing any other bits in register 4.

The bits in registers 10 and 11 must be written to all zeros after a device powerup.

Microprocessor Interface (continued)

I/O Timing

The I/O timing specifications for the microprocessor interface are given in Table 19. The microprocessor interface pins use CMOS I/O levels. All outputs, except the address/data bus AD[7:0], are rated for a capacitive load of 50 pF. The AD[7:0] outputs are rated for a 100 pF load. The minimum read and write cycle time is 200 ns for all device configurations.

Table 19. Microprocessor Interface I/O Timing Specifications

Symbol	Configuration	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t1	Modes 1 & 2	Address Valid to $\overline{AS}$ Asserted (Read, Write)	15	—	—
t2		$\overline{AS}$ Asserted to Address Invalid (Read, Write)	—	10	—
t3		$\overline{AS}$ Asserted to $\overline{DS}$ Asserted	50	—	—
t4		R/$\overline{W}$ High (Read) to $\overline{DS}$ Asserted	25	—	—
t5		$\overline{DS}$ Asserted (Read, Write) to $\overline{DTACK}$ Asserted	—	—	20
t6		$\overline{DTACK}$ Asserted to Data Valid (Read)	—	—	70
t7		$\overline{DS}$ Asserted (Read) to Data Valid	—	—	90
t8		$\overline{DS}$ Negated (Read, Write) to $\overline{AS}$ Negated	—	—	25
t9		$\overline{DS}$ Negated (Read) to Data Invalid	—	—	15
t10		$\overline{DS}$ Negated (Read) to $\overline{DTACK}$ Negated	—	—	15
t11		$\overline{AS}$ (Read, Write) Asserted Width	—	150	—
t12		$\overline{DS}$ (Read) Asserted Width	—	100	—
t13		$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	25	—	—
t14		R/$\overline{W}$ Low (Write) to $\overline{DS}$ Asserted	25	—	—
t15		Data Valid to $\overline{DS}$ Negated (Write)	25	—	—
t16		$\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Write)	—	—	20
t17		$\overline{DS}$ Negated to Data Invalid (Write)	—	25	—
t18		$\overline{DS}$ (Write) Asserted Width	—	100	—
t19	Modes 3 & 4	Address Valid to ALE Asserted Low (Read, Write)	15	—	—
t20		ALE Asserted Low (Read, Write) to Address Invalid	—	10	—
t21		ALE Asserted Low to $\overline{RD}$ Asserted (Read)	30	—	—
t22		$\overline{RD}$ Asserted (Read) to Data Valid	—	—	90
t23		$\overline{RD}$ Asserted (Read) to RDY Asserted	—	—	75
t24		$\overline{RD}$ Negated to Data Invalid (Read)	—	—	20
t25		$\overline{RD}$ Negated to RDY Negated (Read)	—	—	25
t26		ALE Asserted Low to $\overline{WR}$ Asserted (Write)	30	—	—
t27		$\overline{CS}$ Asserted to RDY Asserted Low	—	—	16
t28		Data Valid to $\overline{WR}$ Negated (Write)	25	—	—
t29		$\overline{WR}$ Asserted (Write) to RDY Asserted	—	—	73
t30		$\overline{WR}$ Negated to RDY Negated (Write)	—	—	22
t31		$\overline{WR}$ Negated to Data Invalid	—	25	—
t32		ALE Asserted (Read, Write) Width	—	150	—
t33		$\overline{RD}$ Asserted (Read) Width	—	100	—
t34		$\overline{WR}$ Asserted (Write) Width	—	100	—

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 4—11.

Microprocessor Interface (continued)

I/O Timing (continued)

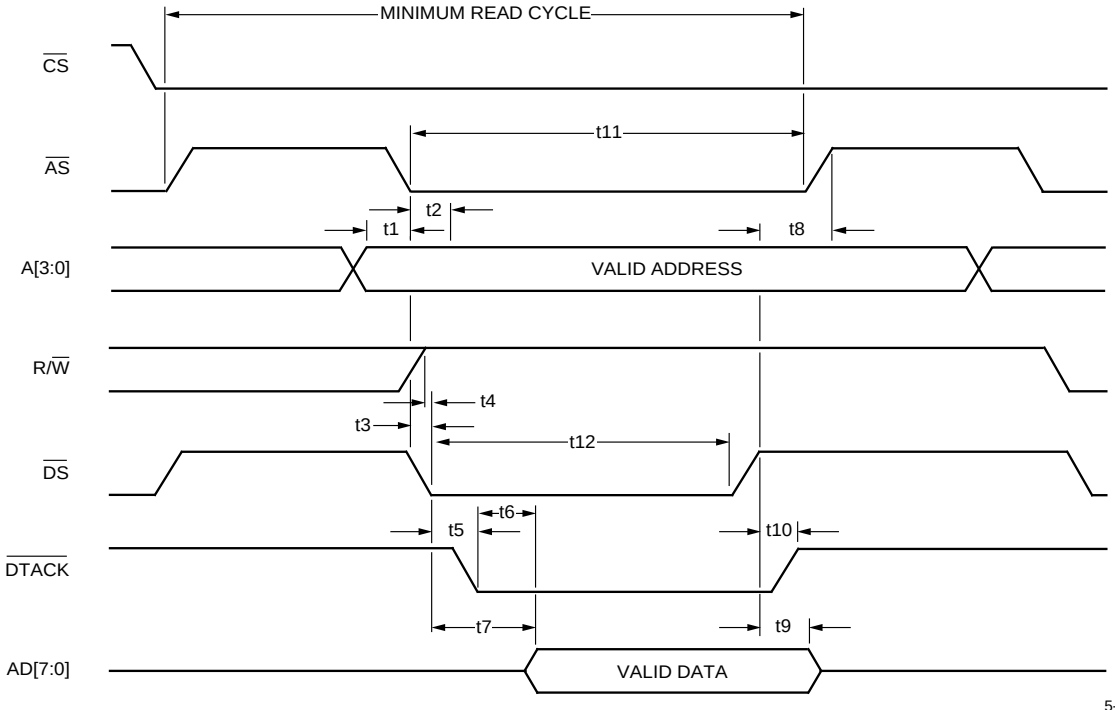


Figure 4. Mode1—Read Cycle Timing (MPMODE = 0, MPMUX = 0)

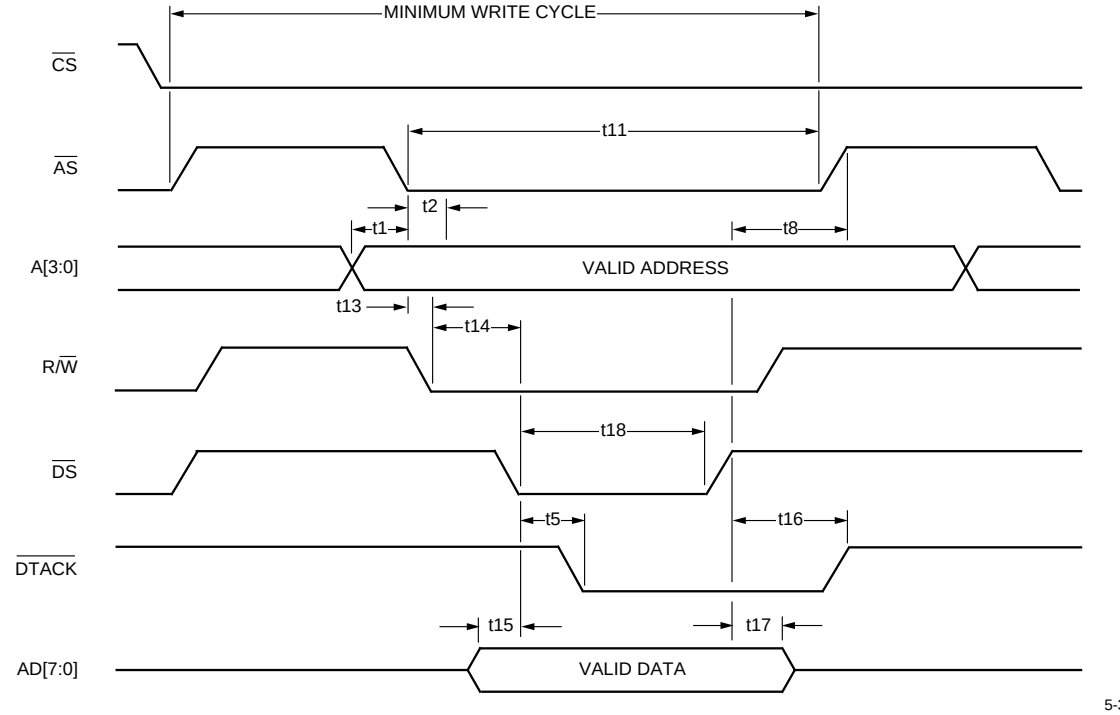


Figure 5. Mode1—Write Cycle Timing (MPMODE = 0, MPMUX = 0)

Microprocessor Interface (continued)

I/O Timing (continued)

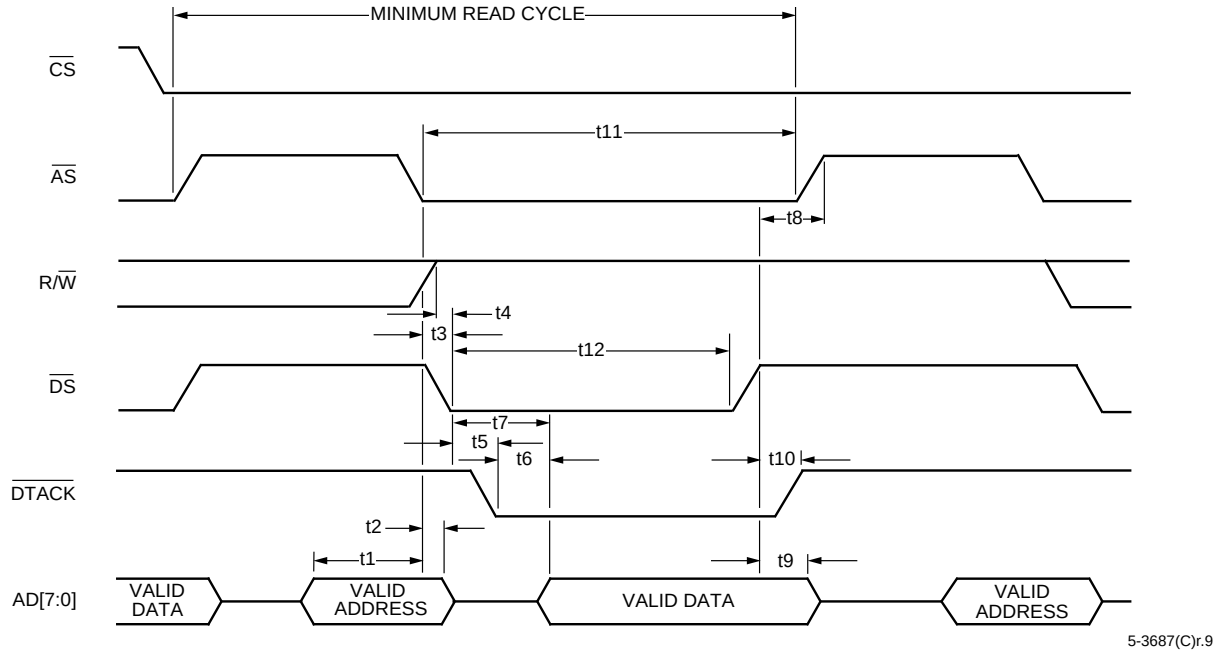


Figure 6. Mode2—Read Cycle Timing (MPMODE = 0, MPMUX = 1)

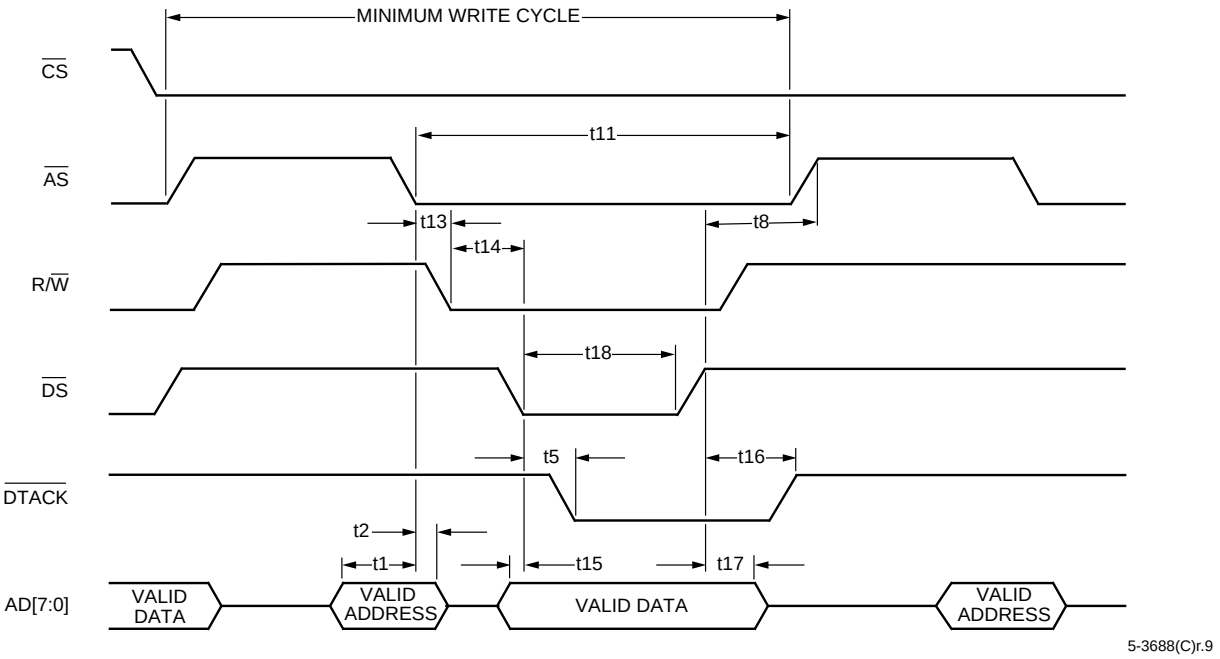


Figure 7. Mode2—Write Cycle Timing (MPMODE = 0, MPMUX = 1)

Microprocessor Interface (continued)

I/O Timing (continued)

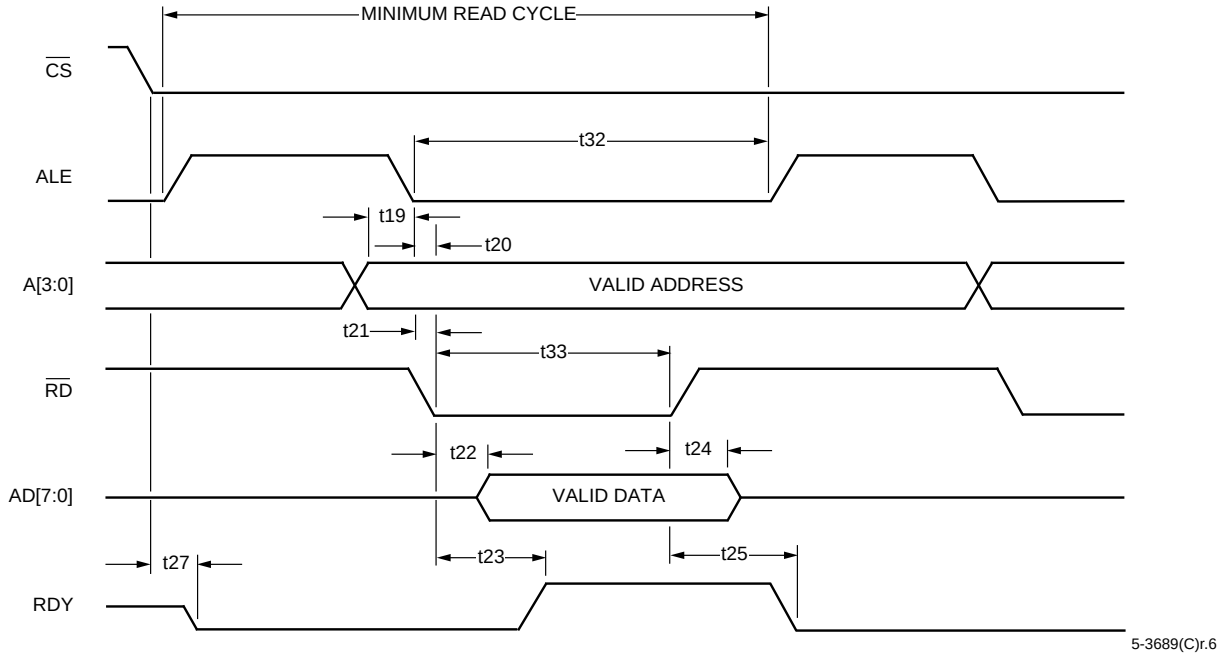


Figure 8. Mode3—Read Cycle Timing (MPMODE = 1, MPMUX = 0)

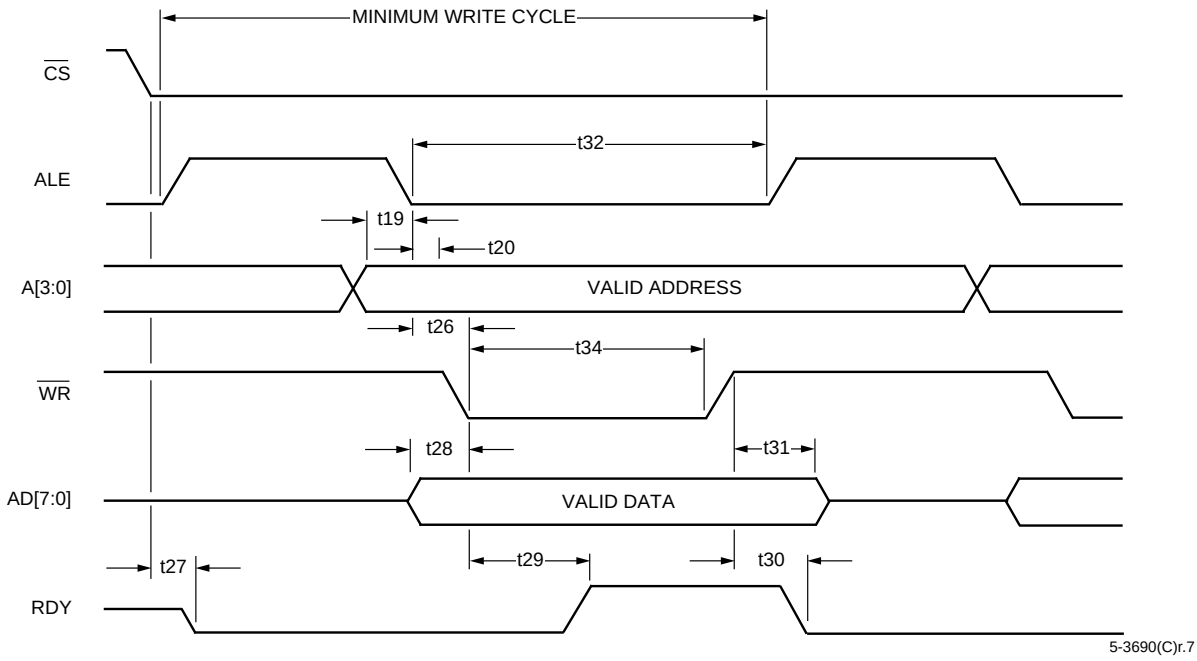


Figure 9. Mode3—Write Cycle Timing (MPMODE = 1, MPMUX = 0)

Microprocessor Interface (continued)

I/O Timing (continued)

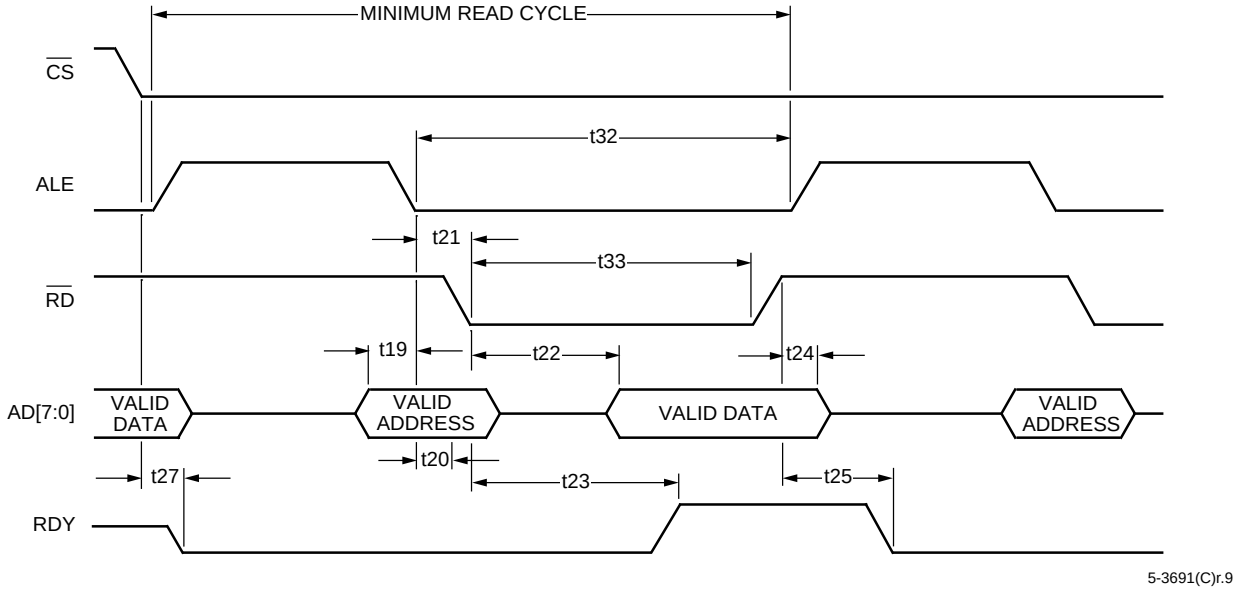


Figure 10. Mode4—Read Cycle Timing (MPMODE = 1, MPMUX = 1)

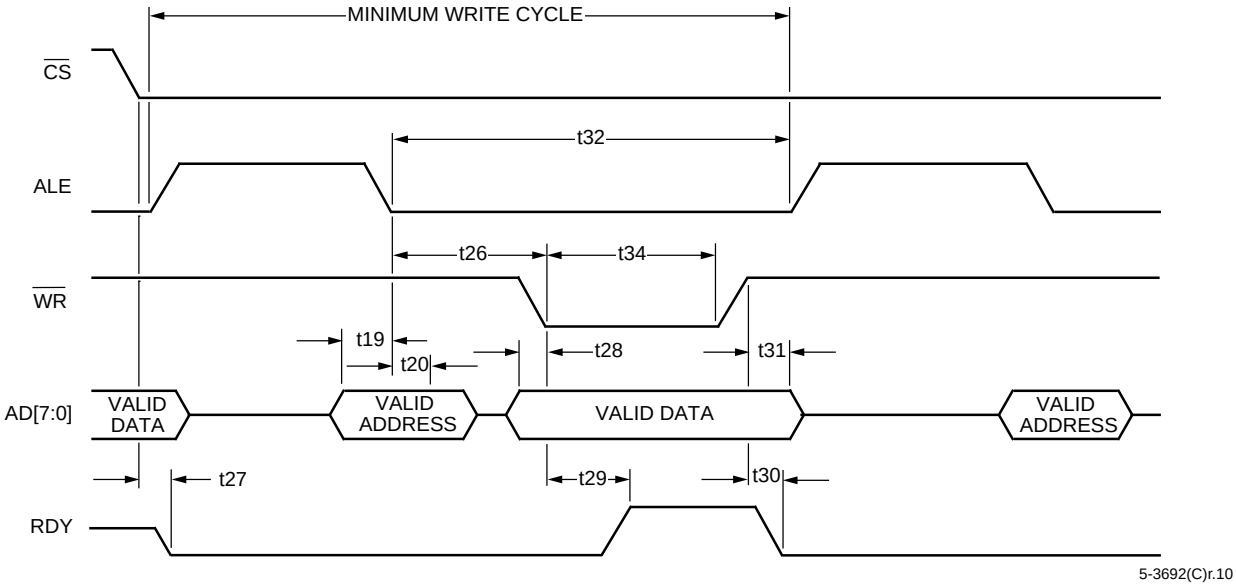


Figure 11. Mode4—Write Cycle Timing (MPMODE = 1, MPMUX = 1)

XCLK Reference Clock

The device requires a high-frequency reference clock for both clock/data recovery and jitter attenuation options (CDR = 1, JAR = 1, or JAT = 1). The XCLK signal (pin 29) is conditionally required if the MPCLK signal (pin 83) is not supplied for interrupt generation in the microprocessor interface. For any other device configuration, XCLK is not required. If it is required, XCLK must be a continuously active (i.e., ungapped, unjittered, and unswitched) and an independent reference clock, such as an external system oscillator or system clock, for proper operation. It must not be derived from any recovered line clock (i.e., from RCLK or any synthesized frequency of RCLK). The specifications for XCLK are defined in Table 20.

Table 20. XCLK Timing Specifications

Parameter	Value			Unit
	Min	Typ	Max	
Frequency: DS1	—	24.704	—	MHz
Range	–100	—	100	ppm
Duty Cycle	40	—	60	%

Power Supply Bypassing

External bypassing is required for all channels. A 1.0 µF capacitor must be connected between $V_{DD}X$ and GNDX. In addition, a 0.1 µF capacitor must be connected between V_{DDD} and GND_D, and a 0.1 µF capacitor must be connected between V_{DDA} and GND_A. Ground plane connections are required for GNDX, GND_D, and GND_A. Power plane connections are also required for $V_{DD}X$ and V_{DDD}. The need to reduce high-frequency coupling into the analog supply (V_{DDA}) may require an inductive bead to be inserted between the power plane and the V_{DDA} pin of every channel.

External bypassing is also required for the microprocessor power supply pins. A 0.1 µF capacitor must be connected between every pair of V_{DDC} and GND_C pins. V_{DDC} and GND_C are connected directly to the power and ground planes, respectively.

Capacitors used for power supply bypassing should be placed as close as possible to the device pins for maximum effectiveness.

External Line Interface Circuitry

The transmit and receive tip/ring connections provide a matched interface to the cable (i.e., terminating impedance matches the characteristic impedance of the cable). The diagram in Figure 12 shows the appropriate external components to interface to the cable for a single transmit/receive channel. The component values are summarized in Table 21, based on the specific application.

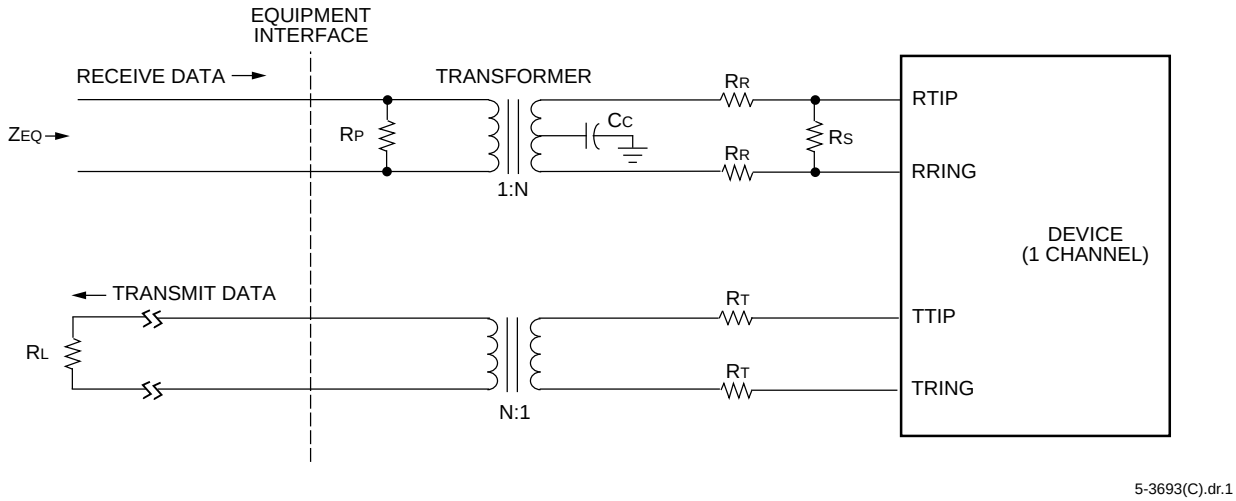


Figure 12. External Line Termination Circuitry

Table 21. Termination Components by Application*

Symbol	Name	Cable Type	Unit
		Twisted Pair	
C_C	Center Tap Capacitor	0.1	µF
R_P	Receive Primary Impedance	200	Ω
R_R	Receive Series Impedance	71.5	
R_S	Receive Secondary Impedance	113	
Z_{EQ}	Equivalent Line Termination	100	
	Tolerance	±4	%
R_T	Transmit Series Impedance	0	Ω
R_L	Transmit Load Termination†	100	
N	Transformer Turns Ratio	1.14	—

* Resistor tolerances are ±1%. Transformer turns ratio tolerances are ±2%.
† A ±5% tolerance is allowed for the transmit load termination.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 22. Absolute Maximum Ratings

Parameter	Min	Max	Unit
dc Supply Voltage	–0.5	6.5	V
Storage Temperature	–65	125	°C
Maximum Voltage (digital pins) with Respect to V_{DDD}	—	0.5	V
Minimum Voltage (digital pins) with Respect to GND_D	–0.5	—	V
Maximum Allowable Voltages (RTIP[1—4], RRING[1—4]) with Respect to V_{DD}	—	0.5	V
Minimum Allowable Voltages (RTIP[1—4], RRING[1—4]) with Respect to GND	–0.5	—	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 23. HBM ESD Threshold Voltage

Device	Voltage
T7689	>1500 V

Table 24. CDM ESD Threshold Voltage

Device	Voltage
T7689	>1500 V

Operating Conditions

Table 25. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	—	85	°C
Power Supply	V_{DD}	4.75	5.0	5.25	V

Operating Conditions (continued)

Table 26. Power Specifications (V_{DD} = 5 V and T_A = 25 °C; Device power specification includes power to the line for a specified data ones density.)

Parameter	T7689	Unit
Per Channel*: (typical)		
CDR = 0, JAx = 0 (transmit, receiver in data slicing mode, no jitter attenuator)	83	mW
CDR = 1, JAx = 0 (transmit, receiver in clock recovery mode, no jitter attenuator)	97	mW
CDR = 1, JAx = 1 (transmit, receiver in clock recovery mode, jitter attenuator active)	100	mW
During Powerdown Mode (PWRDN = 1)†	2.5	mW
Quad Total:		
Typical‡	412	mW
Max	780§	mW

* A single channel (receive and transmit paths) for 50% ones density data.
† For standby purposes. If a channel will never be used, connecting all V_{DD} pins to the ground plane is recommended, resulting in no power consumption.
‡ For nominal V_{DD}, T_A = 25 °C. Every function and channel operational with 50% ones density.
§ For V_{DD} = 5.25 V and T_A = 25 °C. Every function and channel operational with 100% ones density.

Timing Characteristics

Table 27. Logic Interface Characteristics

An internal 50 kΩ pull-up is provided on the $\overline{ICT}$ and $\overline{RESET}$ pins. An internal 100 kΩ pull-up is provided on the $\overline{CS}$, XCLK, and BCLK pins. This requires these input pins to sink no more than 20 µA. All buffers use CMOS levels.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:					
Low	V_{IL}	—	GND_D	1.0	V
High	V_{IH}	—	V_{DDD} – 1.0	V_{DDD}	V
Input Leakage	I_L	—	—	1.0	µA
Output Voltage:					
Low	V_{OL}	–5.0 mA	GND_D	0.5	V
High	V_{OH}	5.0 mA	V_{DDD} – 1.0	V_{DDD}	V
Input Capacitance	C_I	—	—	3.0	pF
Load Capacitance*	C_L	—	—	50	pF

* 100 pF allowed for AD[7:0] (pins 69 to 76).

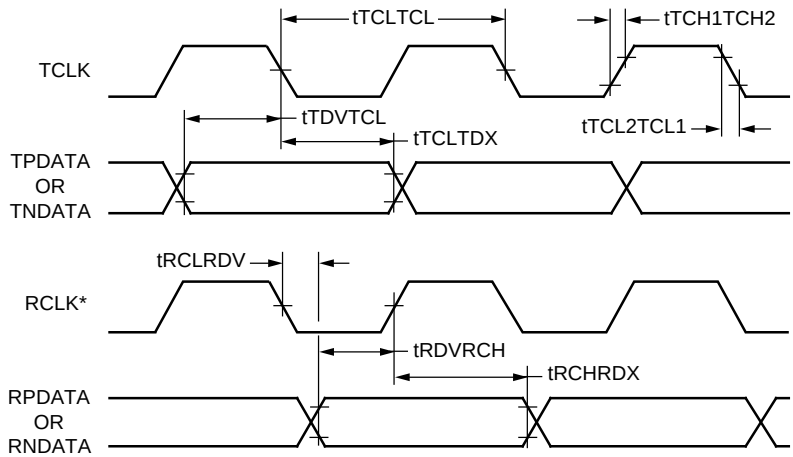
Timing Characteristics (continued)

Table 28. Interface Data Timing

The digital system interface timing is shown in Figure 13 for ACM = 0. If ACM = 1, then the RCLK signal in Figure 13 will be inverted.

Symbol	Parameter	Min	Typ	Max	Unit
tTCLTCL	Average TCLK Clock Period: DS1	 —	 647.7	 —	 ns
tTDC	TCLK Duty Cycle* TCLK Minimum High/Low Time†	30 100	— —	70 —	% ns
tTDVTCL	Transmit Data Setup Time	50	—	—	ns
tTCLTDX	Transmit Data Hold Time	40	—	—	ns
tTCH1TCH2	Clock Rise Time (10%/90%)	—	—	40	ns
tTCL2TCL1	Clock Fall Time (90%/10%)	—	—	40	ns
tRCHRCL	RCLK Duty Cycle	45	50	55	%
tRDVRCH	Receive Data Setup Time	140	—	—	ns
tRCHRDX	Receive Data Hold Time	180	—	—	ns
tRCLRDV	Receive Propagation Delay	—	—	40	ns

* Refers to each individual bit period for JAT = 0 applications.
† Refers to each individual bit period for JAT = 1 applications using a gapped TCLK.



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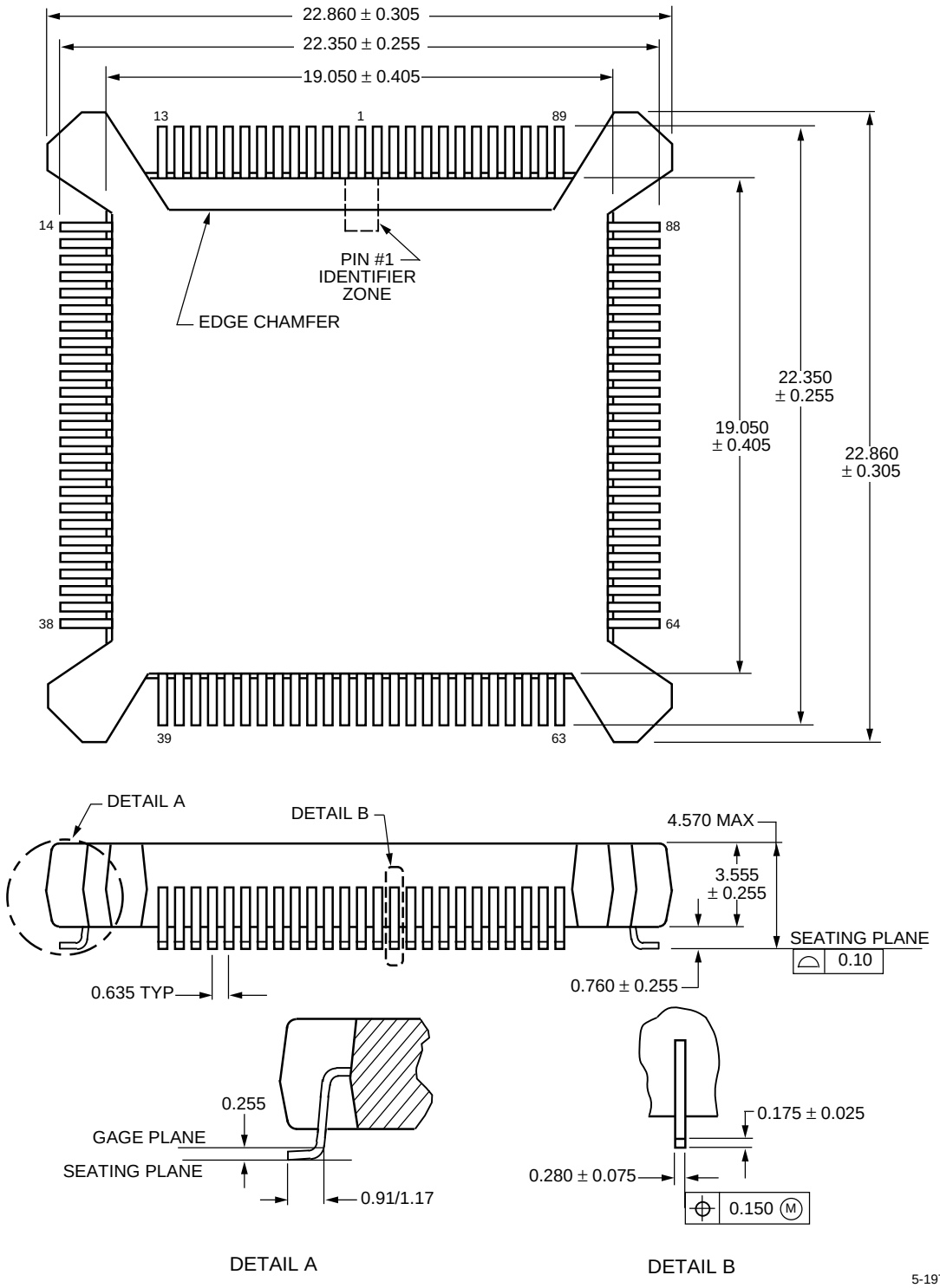
* Invert RCLK for ACM = 1.

Figure 13. Interface Data Timing (ACM = 0)

Outline Diagram

100-Pin BQFP

Dimensions are in millimeters.



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Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T-7689 - - - FL - DB	100-Pin BQFP	–40 °C to +85 °C	107579625

DS98-232TIC Replaces DS96-185TIC to Incorporate the Following Updates

1. Title corrected.
2. Page 3, Figure 1, corrected Block Diagram (Single Channel).
3. Page 24, Table 16, Global Control Register (0100), added register address in table title.
4. Page 24, Table 17, Global Control Register (0101), added register address in table title.
5. Page 25, Channel Configuration Register Overview (0110—1001), corrected register address in section heading.
6. Page 32, Figure 12, External Line Termination Circuitry, updated transformer.

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