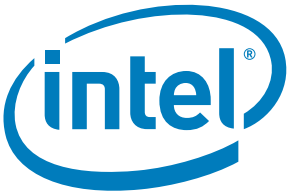
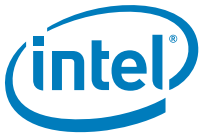


Intel® Xeon® Processor E7-8800/4800/2800 Product Families

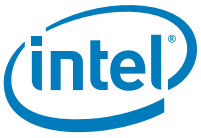
Datasheet Volume 1 of 2

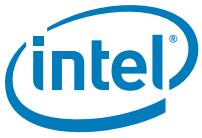
April 2011

Reference Number: 325119-001

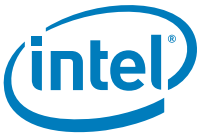


Contents

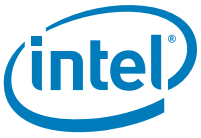




Figures



Tables



Revision History

Document Number	Revision Number	Description	Date
325119	001	• Public release	April 2011

§

1 Introduction

The Intel® Xeon® Processor E7-8800/4800/2800 Product Families are a next-generation Intel® Xeon® multi-core MP family processor. The processor uses Intel® QuickPath Interconnect (Intel® QPI) technology, implementing up to four high-speed serial point-to-point links. It is optimized for MP configurations targeted at enterprise and technical computing applications, delivering server-class RAS and performance.

Intel Xeon Processor E7-8800/4800/2800 Product Families are multi-core processors, based on 32-nm process technology. The processors feature Intel QuickPath Interconnect point-to-point links capable of up to 6.4 GT/s, up to 30 MB of shared cache, and an integrated memory controller. The processors support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4). The processors support several Advanced Technologies: Execute Disable Bit, Intel® 64 technology, Enhanced Intel SpeedStep® technology, Intel® Virtualization technology (Intel® VT), and Simultaneous Multi-Threading.

Feature	Intel® Xeon® Processor E7-8800/4800/2800 Product Families
Cache Sizes	Instruction Cache (L1) = 32 KB/core (I) and16 KB/core (D) Data Cache (L2) = 256 KB/core Last Level Cache (L3) = 30 MB shared among cores
Data Transfer Rate	Up to four full-width Intel QuickPath Interconnect links, up to 6.4 GT/s in each direction
Multi-Core Support	Up to 10 cores per processor
Multiple Processor Support	Dependent on SKU, and supporting silicon. Minimum of two CPUs.
Package	1567-land FCLGA

1.1 Terminology

A '_N' after a signal name refers to an active low signal, indicating that a signal is in the asserted state when driven to a low level. For example, when RESET_N is low (that is, when RESET_N is asserted), a reset has been requested. Conversely, when TCK is high (that is, when TCK is asserted), a test clock request has occurred.

- **Enhanced Intel SpeedStep technology** — Enhanced Intel SpeedStep technology allows the O/S to reduce power consumption when performance is not needed.
- **Eye Definitions** — The eye at any point along the data channel is defined to be the creation of overlapping of a large number of UI of the data signal and timing width measured with regards to the edges of a separate clock signal at any other point. Each differential signal pair by combining the D+ and D- signals produces a signal eye. A _DN and _DP after a signal name refers to a differential pair.
- **FCLGA-1567** — The Intel Xeon Processor E7-8800/4800/2800 Product Families are available in a Flip-Chip Land Grid Array (FC-LGA) package, consisting of 10 processor cores mounted on a pinned substrate with an integrated heat spreader (IHS).
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.

- **Integrated Heat Spreader (IHS)** — A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Intel® QuickPath Interconnect (Intel® QPI)** — Intel QuickPath Interconnect is a cache-coherent, links-based interconnect specification for Intel® processor, chipset, and I/O bridge components.
- **Jitter** — Any timing variation of a transition edge or edges from the defined UI.
- **MP** — Multi-processor system consisting of more than two processors.
- **OEM** — Original Equipment Manufacturer.
- **Processor Information ROM (PIROM)** — A memory device located on the processor and accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. This device is shared with the Scratch EEPROM, is programmed during manufacturing, and is write-protected.
  - **Scratch EEPROM (Electrically Erasable, Programmable Read-Only Memory)** — A memory device located on the processor and addressable via the SMBus which can be used by the OEM to store information useful for system management.
- **SMBus** — System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I^2C* two-wire serial bus developed by Phillips Semiconductor. SMBus is a subset of the I^2C bus/protocol developed by Intel. Implementations of the I^2C bus/protocol or the SMBus bus/protocol may require licensing from various entities, including, but not restricted to, Philips Electronics N.V. and North American Philips Corporation.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor pins should not be connected to any supply voltages, have any I/Os biased, or receive any clocks.
- **Intel® Xeon® Processor E7-8800/4800/2800 Product Familie**s — The entire product, including processor core, die, substrate and integrated heat spreader (IHS).
- **Unit Interval (UI)** — Intel QPI signaling convention is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as:

$$UI_n = t_n - t_{n-1}$$

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1-1. References

Document	Location	Notes
Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet Volume 2 of 2	325120	1
AP-485, Intel® Processor Identification and the CPUID Instruction	241618	1
Intel® 64 and IA-32 Architecture Software Developer's Manual Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide, Part 1 Volume 3B: Systems Programming Guide, Part 2	 253665 253666 253667 253668 253669	1
Intel® 64 and IA-32 Architectures Optimization Reference Manual	248966	1
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001	1
Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines	321736	1

Notes:
1. Document is available publicly at http://developer.intel.com.

1.3 State of Data

The data contained within this document is production data.

1.4 Statement of Volatility

No Intel® Xeon® E7-8800/4800/2800 Product Families processors retain any end user data when powered down and/or when the parts are physically removed from the socket.

§

2 Electrical Specifications

The Intel Xeon Processor E7-8800/4800/2800 Product Families package pin electrical specification is outlined in this section. The Intel Xeon E7-8800/4800/2800 Product Families processor interfaces to other components of the platform via connections established at Intel® QuickPath Interconnect (Intel® QPI), Intel® Scalable Memory Interconnect (Intel® SMI), system management interfaces, power, reset, clock and debug signals. The electrical characteristics of all such signals, categorized per the I/O type, are documented in this section.

2.1 Processor Maximum Ratings

Table 2-1 specifies absolute maximum and minimum ratings. Within operational maximum and minimum limits, functionality and long-term reliability can be expected. Processor maximum ratings outlined in Table 2-1 are applicable for all Intel Xeon E7-8800/4800/2800 Product Families processor SKUs.

At conditions outside operational maximum ratings, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within operational maximum and minimum ratings after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, then when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-1. Processor Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes 1, 2
Vcc	Processor core supply voltage with respect to VSS	–0.3	1.42	V	
V_{CACHE}	Processor cache voltage with respect to VSS	–0.3	1.55	V	
V_{REG}	Processor Analog Supply Voltage with respect to VSS	–0.3	1.89	V	
V_{IOC}	Processor Intel QPI I/O Supply Voltage with respect to VSS	–0.3	1.55	V	
V_{IOF}	Processor I/O Supply Voltage for SMI with respect to VSS	–0.3	1.55	V	
V_{CC33}	Processor 3.3V Supply Voltage with respect to VSS	3.135	3.465	V	

Table 2-1. Processor Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes 1, 2
V(ISENSE)	Analog input voltage with respect to Vss for sensing current consumption	-0.25	1.15	V	
T_{CASE}	Processor case temperature	See Chapter 6	See Chapter 6		
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	3, 4

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any packaging or trays.

2.2 Socket Voltage Identification

The VID[7:0], CVID[7:1], and VIO_VID[4:1] pins identify encoding that determine the voltage to be supplied by the VR to the socket Vcore, Vcache and VIO (the core, cache & system interface voltages for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor) voltage regulators. The CoreVID and CacheVID specifications for the Intel Xeon Processor E7-8800/4800/2800 Product Families processors are defined by VR 11.1. VIO_VID specifications for the Intel Xeon Processor E7-8800/4800/2800 Product Families processors are defined by VR 11.0.

For CoreVID and CacheVID, individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. Furthermore, any Intel Xeon Processor E7-8800/4800/2800 Product Families processor can drive different VID settings during normal operation. For VIO_VID, all processors of a given stepping will have the same values.

The Voltage Identification (VID) specification for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor Vcc pins. VID signals are CMOS push/pull drivers. Please refer to Table 2-24 for the DC specifications for these signals. A voltage range is provided in Table 2-5 and changes with frequency. The specifications have been set such that one voltage regulator can operate with all supported frequencies.

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor uses eight voltage identification signals, VID[7:0], to support automatic selection of power supply voltages. Table 2-2 specifies the voltage level corresponding to the state of VID[7:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (SKTOCC# high), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. See the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for further details.

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (Vcc). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the

maximum specified VID are not permitted. Table 2-5 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-6.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-5 and Table 2-6, while AC specifications are included in Table 2-28. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for further details.

The VIO_VID[4:1] pins identify encoding that determine the voltage to be supplied by the VR 11.1 to the socket Vio voltage regulators. In all cases, when reading from Table 2-2, assume VID7=0, VID6=1, VID5=0, and VID0=0. Note that all Intel Xeon Processor E7-8800/4800/2800 Product Families processor SKUs will have the same setting.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-2. Voltage Identification Definition (Sheet 1 of 5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000

Table 2-2. Voltage Identification Definition (Sheet 2 of 5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750

Table 2-2. Voltage Identification Definition (Sheet 3 of 5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500

Table 2-2. Voltage Identification Definition (Sheet 4 of 5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250

Table 2-2. Voltage Identification Definition (Sheet 5 of 5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Notes:
1. When the "11111111" VID pattern is observed, or when the SKTOCC# pin is deasserted, the voltage regulator output should be disabled.
2. Shading denotes the expected VID range of the Intel Xeon Processor E7-8800/4800/2800 Product Families processor.
3. The VID range includes VID transitions that may be initiated by thermal events, Extended HALT state transitions, higher C-States or Enhanced Intel® SpeedStep technology transitions. **The Extended HALT state must be enabled for the processor to remain within its specifications**
4. Once the VRM/EVRD is operating after power-up, if either the Output Enable signal is de-asserted or a specific VID off code is received, the VRM/EVRD must turn off its output (the output should go to high impedance) within 500 ms and latch off until power is cycled. Refer to *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines.*

2.3 Signal Groups

The signals are grouped by buffer type and similar characteristics, as listed in Table 2-3. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals have On Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board. The signals which have ODT are listed in Table 2-4.

Table 2-3. Signal Groups (Sheet 1 of 2)

Signal Group	Type	Signals[1]
System Reference Clock		
Differential	Differential Pair, HSTL	SYSCLK_DP, SYSCLK_DN, SYSCLK_LAI_N, SYSCLK_LAI
Intel® QPI Interface Signal Groups		
Differential	SCiD 2 Input	QPI[3:0]_DRX_D[n/p][19:0], QPI[3:0]_CLKRX_D[p/n]
Differential	SCiD 2 Output	QPI[3:0]_DTX_D[n/p][19:0], QPI[3:0]_CLKTX_D[p/n]
Intel® SMI Signals		
Differential	Inputs	FBD0NBICLK[A/B][P/N]0 FBD1NBICLK[C/D][P/N]0
Differential	Output	FBD0SBOCLK[A/B][P/N]0 FBD1SBOCLK[C/D][P/N]0
Differential	Input	FBD0NBI[A/B][P/N][13:0] FBD1NBI[C/D][P/N][13:0]
Differential	Output	FBD0SBO[A/B][P/N][10:0], FBD1SBO[C/D][P/N][10:0]
TAP		
Single ended	GTL	TCK, TDI,TMS, TRST_N
Single ended	GTL-Open Drain	TDO
PECI		
Single ended	CMOS	PECI
SMBus		
Single ended	CMOS	SMBCLK, SMBDAT, SM_WP
SPD Bus		
Single ended	CMOS I/OD	SPDCLK, SPDDAT
Strap Pins		
Single ended	GTL	BOOTMODE[1:0]
Single ended	CMOS	SKTID[2:0]
Flash ROM Port		
Single ended	GTL - OD	FLASHROM_CFG[2:0], FLASHROM_DATI FLASHROM_CS[3:0]_N, FLASHROM_CLK, FLASHROM_DATO, FLASHROM_WP_N
ERROR Bus		
Single ended	GTL Input, GTL Open Drain Output	ERROR[0]_N, ERROR[1]_N
Power Up, RESETs		
Single ended	CMOS Input	PWRGOOD, VIOPWRGOOD,
Single ended	GTL Input	RUNBIST, RESET_N
Thermal		
Single ended	GTL Input	Force_PR_N
Single ended	GTL	MEM_Throttle[1]_N,MEM_Throttle[0]_N
Single ended	GTL-Open Drain	PROCHOT_N, THERMTRIP_N
Single ended	CMOS - Open Drain	Thermalert_N

Table 2-3. Signal Groups (Sheet 2 of 2)

Signal Group	Type	Signals[1]
VID		
Single ended	CMOS Output	VID[7:0], CVID[7:1]
Single ended	Open/Ground	VIO_VID[4:1]
Voltage, and Voltage Regulator		
Differential	Power	ISENSE_DN, ISENSE_DP
Single ended	Power	Vcc, VREG, VCACHE, VCACHESENSE, VCC33,VCORESENSE, VIO, PSI_CACHE_N,PSI_N, VSSCACHESENSE,VSSCORESENSE,
Debug		
Single ended	GTL I/O-OD	MBP[7:0]_N, PRDY_N,PREQ_N

Notes:

1. See Chapter 5 for signal descriptions.

Table 2-4. Signals with R_{TT}

Signals with RTT
• QPI[3:0]R[P/N]Dat[19:0], QPI[5:4]R[P/N]CLK0, QPI[3:0]T[P/N]Dat[19:0], QPI[5:4]T[P/N]CLK0 • FBD0NBICLK[A/B][P/N]0, FBD1NBICLK[C/D][P/N]0, FBD0SBOCLK[A/B][P/N]0, FBD1SBOCLK[C/D][P/N]0, FBD0NBI[A/B][P/N][12:0], FBD1NBI[C/D][P/N][12:0], FBD0SBO[A/B][P/N][9:0], FBD1SBO[C/D][P/N][9:0].

2.4 Processor DC Specifications

Voltage and current specifications are detailed in Table 2-5. For platform planning refer to Table 2-6, which provides Vcc static and transient tolerances.

Differential SYSCLK specifications are found in Table 2-26. Control Sideband and Test Access Port (TAP) are listed in Table 2-24.

Table 2-5 through Table 2-24 list the DC specifications for the processor and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Chapter 6, "Thermal Specifications"), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 2-5. Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes 1
VID	VCore VID range	N/A	0.60		1.35	V	4,5
Vcc	V_{CC} for processor core Launch - FMB	See Table 2-6				V	4,5,6
Vcc LL	Vcc Load Line			0.8		mΩ	
CVID	VCache VID range		0.7		1.35	V	4,5
V_{CACHE}	Vcc for cache	See Table 2-7				V	4,5,7
V_{CACHE} LL	V_{CACHE} Load Line			1.4		mΩ	
V_{VID_STEP}	Vcc VID step size during a transition	N/A	±6.25			mV	

Table 2-5. Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes 1
V_{VID_SHIFT}	Total allowable DC load line shift from VID steps	N/A			LLType +/ -15mV	mV	
VIO_VID	Processor I/O supply voltage		1.053	1.0875	1.1		1,3
V_{REG}	PLL supply voltage (DC + AC specification)	N/A		1.8		V	1,2
Vcc33	Package component voltage		3.135	3.3	3.465	V	
Icc_Max Vcc33	IccMax for Vcc33				75	mA	
I_{CC_MAX}	I_{CC} for Intel Xeon Processor E7-8800/4800/2800 Product Families processor 130W TDP with multiple VID Launch - FMB	Vcc Vcache V_{IO} V_{REG}			120 75 18.1 1.5	A	
	I_{CC} for Intel Xeon Processor E7-8800/4800/2800 Product Families processor 105W TDP with multiple VID Launch - FMB	Vcc Vcache V_{IO} V_{REG}			115 70 17.6 1.5	A	
	I_{CC} for Intel Xeon Processor E7-8800/4800/2800 Product Families processor 95W TDP with multiple VID Launch - FMB	Vcc Vcache V_{IO} V_{REG}			115 70 17.6 1.5	A	
I_{CC_TDC}	Thermal Design Current (TDC) Intel Xeon Processor E7-8800/4800/2800 Product Families processor 130W TDP Launch - FMB	Vcc Vcache V_{IO} V_{REG}			110 55 16.0 1.3	A	
	Thermal Design Current (TDC) Intel Xeon Processor E7-8800/4800/2800 Product Families processor 105W TDP Launch - FMB	Vcc Vcache V_{IO} V_{REG}			90 50 16.0 1.3	A	
	Thermal Design Current (TDC) Intel Xeon Processor E7-8800/4800/2800 Product Families processor 95W TDP Launch - FMB	Vcc Vcache V_{IO} V_{REG}			85 50 15.5 1.3	A	
PSI TDC	Thermal Design Current Launch - FMB	130W 105W 95W			22 25 21	A	
PSI_CACHE TDC	Thermal Design Current Launch - FMB	130W 105W 95W			45 45 45	A	

Notes:
1. DC for a power supply is defined as any variation less than 1 MHz.
2. ±1% tolerance
3. ±1% ripple, ±2% total as measured at VR remote sense point
4. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
5. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different settings.
6. The V_{CC} voltage specification requirements are measured across vias on the platform for the VCORESENSE and VSSCORESENSE pins close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum

probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

7. The V_{CACHE} voltage specification requirements are measured across vias on the platform for the VCACHESENSE and VSSCACHESENSE pins close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

Table 2-6. Processor Vcc Static and Transient Tolerance

I_{CC} (A)	$Vcc_{\_Max}$ (V)	$Vcc_{\_Typ}$ (V)	$Vcc_{\_Min}$ (V)	Notes
0	VID - 0.000	VID - 0.015	VID - 0.030	-
5	VID - 0.004	VID - 0.019	VID - 0.034	
10	VID - 0.008	VID - 0.023	VID - 0.038	
15	VID - 0.012	VID - 0.027	VID - 0.042	
20	VID - 0.016	VID - 0.031	VID - 0.046	
25	VID - 0.020	VID - 0.035	VID - 0.050	
30	VID - 0.024	VID - 0.039	VID - 0.054	
35	VID - 0.028	VID - 0.043	VID - 0.058	
40	VID - 0.032	VID - 0.047	VID - 0.062	
45	VID - 0.036	VID - 0.051	VID - 0.066	
50	VID - 0.040	VID - 0.055	VID - 0.070	
55	VID - 0.044	VID - 0.059	VID - 0.074	
60	VID - 0.048	VID - 0.063	VID - 0.078	
65	VID - 0.052	VID - 0.067	VID - 0.082	
70	VID - 0.056	VID - 0.071	VID - 0.086	
75	VID - 0.060	VID - 0.075	VID - 0.090	
80	VID - 0.064	VID - 0.079	VID - 0.094	
85	VID - 0.068	VID - 0.083	VID - 0.098	
90	VID - 0.072	VID - 0.087	VID - 0.102	
95	VID - 0.076	VID - 0.091	VID - 0.106	
100	VID - 0.080	VID - 0.095	VID - 0.110	
105	VID - 0.084	VID - 0.099	VID - 0.114	
110	VID - 0.088	VID - 0.103	VID - 0.118	
115	VID - 0.092	VID - 0.107	VID - 0.122	
120	VID - 0.096	VID - 0.111	VID - 0.126	
125	VID - 0.100	VID - 0.115	VID - 0.130	
130	VID - 0.104	VID - 0.119	VID - 0.134	
135	VID - 0.108	VID - 0.123	VID - 0.138	
140	VID - 0.112	VID - 0.127	VID - 0.142	
145	VID - 0.116	VID - 0.131	VID - 0.146	
150	VID - 0.120	VID - 0.135	VID - 0.150	

Notes:

1. The $Vcc_{\_MIN}$ and $Vcc_{\_MAX}$ loadlines represent static and transient limits. Please see Table 2-8 and Figure 2-3 for Vcc overshoot specifications.
2. The loadlines specify voltage limits at the die. Die Vcc voltage is available at the Vcoresense and Vsscoresense lands and should be measured there. Voltage regulation feedback for voltage regulator circuits must be taken from the processor VCORESENSE and VSSCORESENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCCCORESENSE and VSSCORESENSE lands. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.1 Design Guidelines* for socket load line guidelines and VR implementation

Figure 2-1. VCC Static and Transient Tolerance

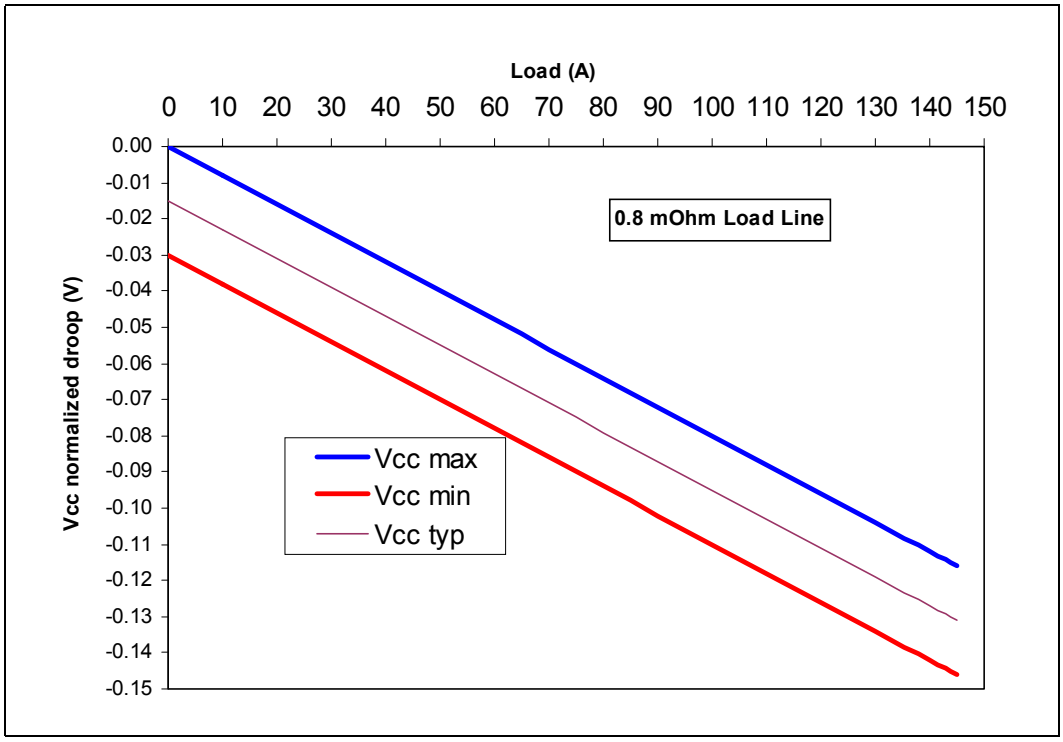


Table 2-7. Processor VccCache Static and Transient Tolerance

I_{CC} (A)	$Vcc_{\_Max}$ (V)	$Vcc_{\_Typ}$ (V)	$Vcc_{\_Min}$ (V)	Notes
0	VID - 0.000	VID - 0.015	VID - 0.030	
5	VID - 0.007	VID - 0.022	VID - 0.037	
10	VID - 0.014	VID - 0.029	VID - 0.044	
15	VID - 0.021	VID - 0.036	VID - 0.051	
20	VID - 0.028	VID - 0.043	VID - 0.058	
25	VID - 0.035	VID - 0.050	VID - 0.065	
30	VID - 0.042	VID - 0.057	VID - 0.072	
35	VID - 0.049	VID - 0.064	VID - 0.079	
40	VID - 0.056	VID - 0.071	VID - 0.086	
45	VID - 0.063	VID - 0.078	VID - 0.093	
50	VID - 0.070	VID - 0.085	VID - 0.100	
55	VID - 0.077	VID - 0.092	VID - 0.107	
60	VID - 0.084	VID - 0.099	VID - 0.114	
65	VID - 0.091	VID - 0.106	VID - 0.121	
70	VID - 0.098	VID - 0.113	VID - 0.128	
75	VID - 0.105	VID - 0.120	VID - 0.135	
80	VID - 0.112	VID - 0.127	VID - 0.142	

Notes:
1. The $Vcc_{\_MIN}$ and $Vcc_{\_MAX}$ loadlines represent static and transient limits. Please see Table 2-8 and Figure 2-3 for Vcc overshoot specifications.

2. The loadlines specify voltage limits at the die. Die VccCache voltage is available at the Vcachesense and Vsscachesense lands and should be measured there. Voltage regulation feedback for voltage regulator circuits must also be taken from the processor VCACHESENSE and VSSCACHESENSE lands. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.1 Design Guidelines* for socket load line guidelines and VR implementation.

Figure 2-2. Vcache Static and Transient Tolerance

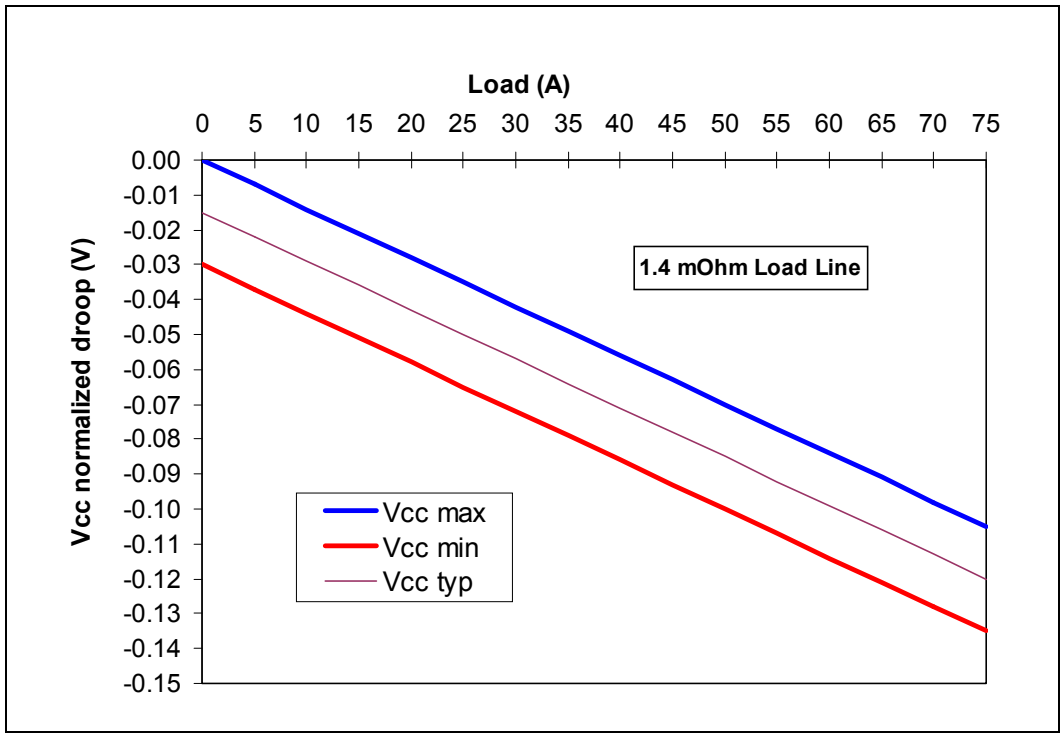
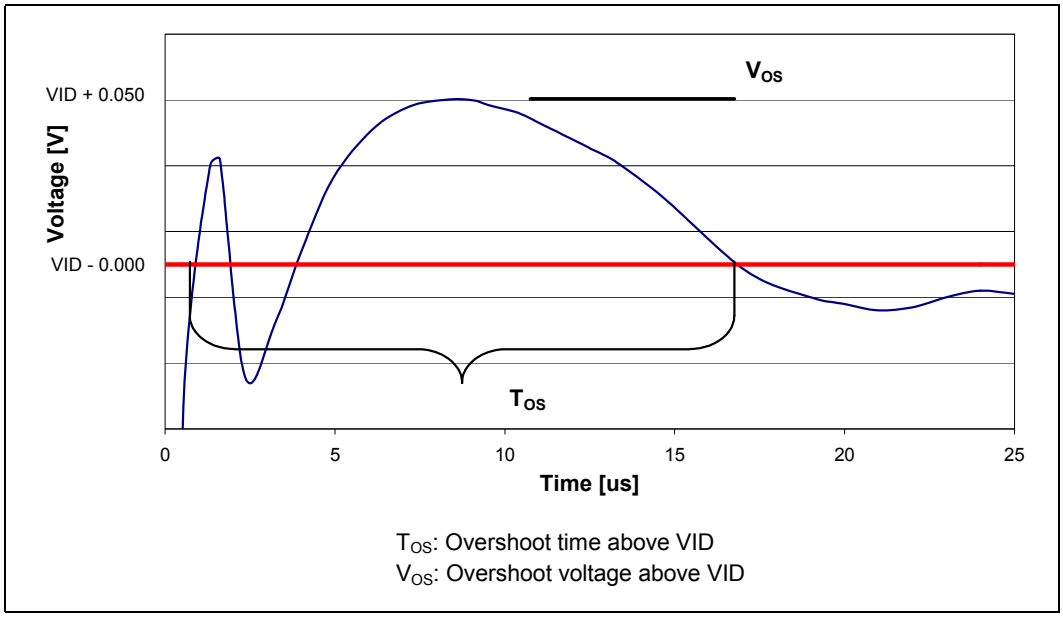


Table 2-8. V_{CC} and Vcache overshoot Specification

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of Vcc Overshoot above VID		0.05	V	2-3	
T_{OS_MAX}	Time duration of V_{CC} Overshoot above VID		25	µs	2-3	

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor can tolerate short transient overshoot events where supplied voltage exceeds the VID/CVID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID/CVID + V_{OS_MAX}. (V_{OS_MAX} is the maximum allowable overshoot above VID/CVID). These specifications apply to the processor die voltages, as measured with respect to VSSCORESENSE, and VSSCACHESENSE.

Figure 2-3. Overshoot Example Waveform



2.5 Intel® QPI and Intel® Scalable Memory Interconnect (Intel® SMI) Interface Differential Signaling

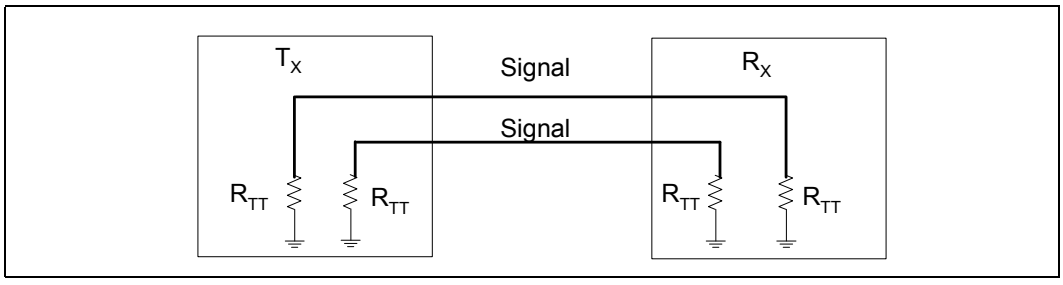
The Intel Xeon Processor E7-8800/4800/2800 Product Families processor Intel QPI and Intel® Scalable Memory Interconnect (Intel® SMI) signals use differential links. The termination voltage level for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor for uni-directional serial differential links, each link consisting of a pair of opposite-polarity (D+, D-) signals is V_{SS}.

Termination resistors are provided on the processor silicon and are terminated to V_{SS}. Intel chipsets also provide on-die termination (ODT), thus eliminating the need to terminate the links on the system board for the Intel QPI and Intel SMI signals.

Figure 2-4 illustrates the active ODT. Signal listings are included in Table 2-3 and Table 2-4.

See Chapter 5 for the pin signal definitions. All of the signals on the processor Intel QPI and Intel SMI signals are in the differential signal group.

Figure 2-4. Active ODT for a Differential Link Example



2.5.1 Intel QPI Signaling Specifications

Intel QPI electrical specifications call out specifications that are common across all platforms and specifications that target Intel QPI within Enterprise MP class server systems.

2.5.1.1 Intel QPI Reference Clocking Specifications

Reference clock requirements required by the PLL as measured at the package pin. Table 2-9 provides a list of system clock specifications.

Figure 2-5. Validation Topology for Testing Specifications of the Reference Clock

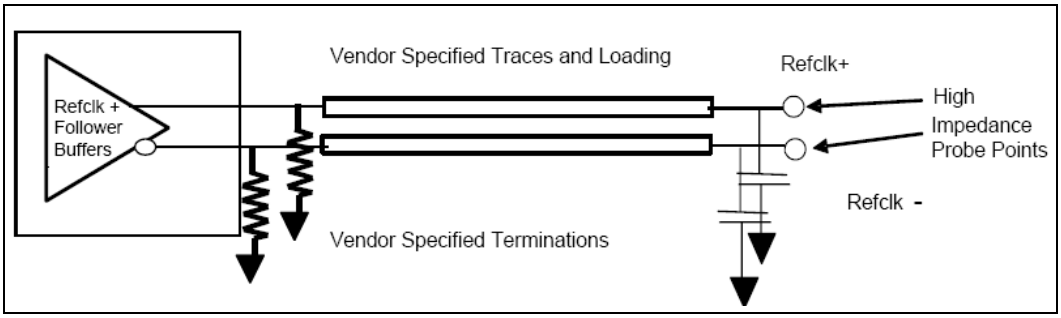


Figure 2-6. Differential Waveform Measurement Points

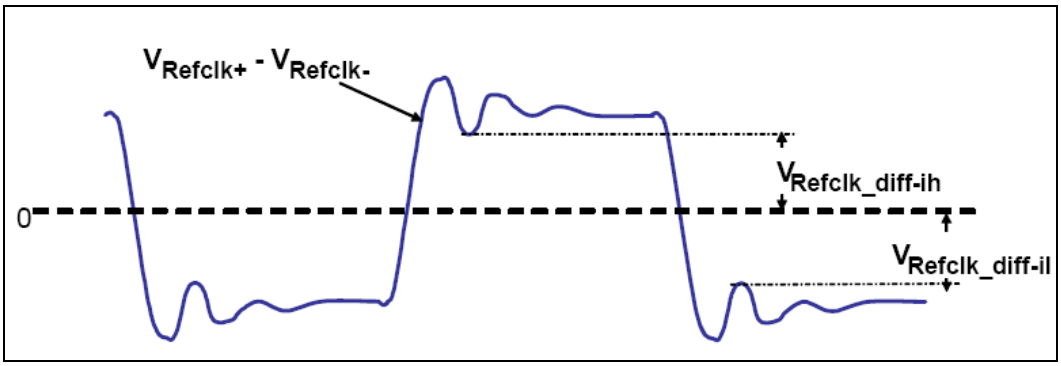


Table 2-9. System Clock Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
f_{Refclk}	System clock frequency		133.33		MHz	
$ER_{Refclk-diffRise}$, $ER_{Refclk-diffFall}$	Rise and fall slope parameter	1.0		4.0	V/nsec	
$V_{Refclk-max}$	Single ended maximum voltage with overshoot			1150	mV	
$V_{Refclk-min}$	Single ended minimum voltage with overshoot	-350			mV	
V_{Cross}	Absolute crossing point limits between Refclk+ and Refclk- waveforms	250		550	mV	See Figure 2-6
V_{Cross_delta}	Peak-peak variation in crossing points			140		See Figure 2-6
$V_{Refclk\_diff-ih}$	High of the differential voltage (V_{Refclk}+ - V_{Refclk}-) above zero	150			mV	

Table 2-9. System Clock Specifications (Sheet 2 of 2)

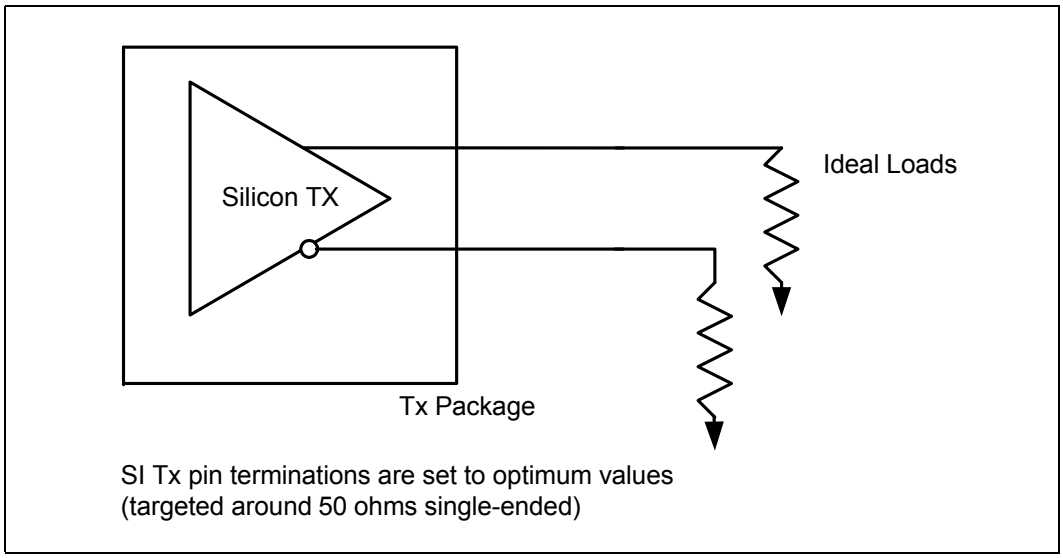
Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Refclk\_diff-il}$	Low of the differential voltage (V_{Refclk}+ - V_{Refclk}-) above zero			-150	mV	
$T_{Refclk-Dutycycle}$	Duty cycle of reference clock.	40	50	60	%	
$T_{Refclk-jitter-rms-onepll}$	Accumulated rms jitter over n UI of a given PLL model output in response to the jittery reference clock input. The PLL output is generated by convolving the measured reference clock phase jitter with a given PLL transfer function. Here n=12.			0.5	psec	1
TRefclk-diff-jit	Phase Drift between clocks at two connected ports			500	psec	
TRefclk-C2C-jit	Short term difference in the period of any two adjacent clock cycles			100	psec	At via

Note:
1. The given PLL parameters are: Underdamping (z) = 0.8 and natural frequency = fn = 7.86E6 Hz; w_n = 2 * fn. N_minUI = 12 for Intel QPI Phy 1 channel.

2.5.1.2 Link Speed Independent Specifications

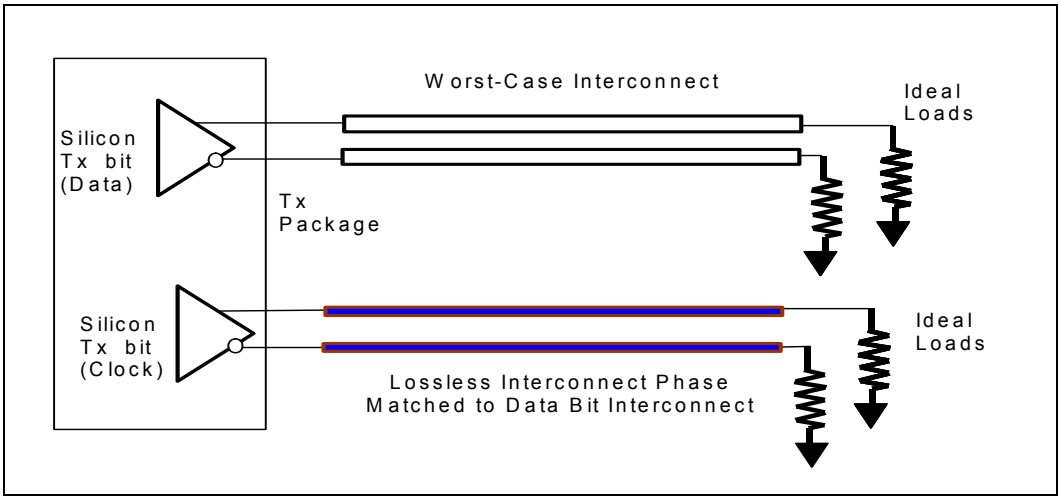
Link speed independent specifications call out the transmitter and receiver parameters required at all link speeds. The transmitter specifications are for stand-alone, individual transmitters (Tx). The validation setup for Tx is called out in Figure 2-7.

Figure 2-7. Setup for Validating Standalone Tx Voltage and Timing Parameters



The parameters for the receiver (Rx) couple the transmitter with the worst-case interconnect. The validation setup for Rx is called out in Figure 2-8.

Figure 2-8. Setup for Validating Tx + Worst-Case Interconnect Specifications



Specifications for link speed independent specifications are called out in Table 2-10.

Table 2-10. Link Speed Independent Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
UIavg	Average UI size at "G" GT/s (Where G = 4.8, 6.4, and so on)	0.999 * nominal	1000/G	1.001 * nominal	psec	
$T_{rise-fall-pin-20-80}$	+/- 100mV@crossing	25 psec		0.25 UI		
$\Delta Z_{TX\_LOW\_CM\_DC}$	Defined as: (max($Z_{TX\_LOW\_CM\_DC}$) - min($Z_{TX\_LOW\_CM\_DC}$)) / $Z_{TX\_LOW\_CM\_DC}$ expressed in %, over full range of Tx single ended voltage	-6		6	% of $Z_{TX\_LOW\_CM\_DC}$	
$\Delta Z_{RX\_LOW\_CM\_DC}$	Defined as: (max($Z_{TX\_LOW\_CM\_DC}$) - min($Z_{TX\_LOW\_CM\_DC}$)) / $Z_{TX\_LOW\_CM\_DC}$ expressed in %, over full range of Tx single ended voltage	-6	0	6	% of $Z_{TX\_LOW\_CM\_DC}$	
RL_{RX}	Return Loss of Receiver Package measured at any data or clock signal inputs			See note		1
$N_{MIN-UI-Validation}$	# of UI over which the eye mask voltage and timing spec needs to be validated	1,000,000				
$Z_{RX\_HIGH\_CM\_DC}$	Single ended DC impedance to GND for either D+ or D- of any data bit at Tx	40k			Ω	2
$Z_{TX\_LINK\_DETECT}$	Link Detection Resistor	500		2000	Ω	
$V_{TX\_LINK\_DETECT}$	Link Detection Resistor Pull-up Voltage			1.5	V	
V_{DIFF_IDLE}	Voltage difference between D+ and D- when lanes are either in Electrical Idle or $V_{TX\_LINK\_DETECT}$			0.1 * $V_{Rx-diff-pp-pin}$	V	

Table 2-10. Link Speed Independent Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$T_{DATA\_TERM\_SKEW}$	Skew between first to last data termination meeting $Z_{RX\_LOW\_CM\_DC}$			128	UI	
$T_{INBAND\_RESET\_SENSE}$	Time taken by inband reset detector to sense Inband Reset			1.5	µs	
$Tclk_{\_DET}$	Time taken by clock detector to observe clock stability			20K	UI	
$T_{CLK\_FREQ\_DET}$	Time taken by clock frequency detector to decide slow vs. operational clock after stable clock			32	Reference Clock Cycles	
$T_{Refclk\text{-}Tx\text{-}Variability}$	Phase variability between reference Clk (at Tx input) and Tx output.			500	psec	
$T_{Refclk\text{-}Rx\text{-}Variability}$	Phase variability between reference Clk (at Rx input) and Rx output.	1000			psec	
$L_{D+/D\text{-}RX\text{-}Skew}$	Phase skew between D+ and D- lines for any data bit at Rx			0.03	UI	
BER_{Lane}	Bit Error Rate per lane valid for 4.8 and 6.4 GT/s			1.0E-14	Events	
Voh_bscan	Output high during boundary scan	VIO-100		VIO	mV	
Vol_bscan	Output low during boundary scan	0		100	mV	
Vih_bcan	Input high during boundary scan	0.86 * VIO			V	
Vil_bscan	Output low during boundary scan			0.40 * VIO	V	

Notes:
1. Return loss specifications for receiver package are not provided. However, maintaining a well impedance matched and low loss receiver package is crucial for a successful silicon operation, including maintaining as low as possible on-die capacitance.
2. Used during initialization. It is the state of "OFF" condition for the receiver when only the minimum termination is connected

2.5.2 Intel QPI Electrical Specifications

The applicability of this section applies to Intel QPI within a links-based Enterprise MP class server platform. This section contains information for slow boot up speed (1/4 frequency of the reference clock), 4.8 GT/s, and 6.4 GT/s.

The transfer rates available for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor are shown in Table 2-11.

Table 2-11. Clock Frequency Table

Intel QPI System Interface Forwarded Clock Frequency	Intel QPI System Interface Data Transfer Rate
33.33 MHz	66.66 MT/s[1]
2.40 GHz	4.8 GT/s
3.20 GHz	6.4 GT/s

Notes:

1. This speed is the 1/4 RefClk Frequency.

2.5.2.1 Requirements at 1/4 RefClk Signaling Rate

The signaling rate is defined as 1/4 the rate of the System Reference Clock. For example, a 133 MHz System Reference Clock would have a forwarded clock frequency of 33.33 MHz and the signaling rate would be 66.66 MT/s.

Table 2-12. Parameter Values for Intel® QPI Phy1 Channel at 1/4 RefClk Frequency

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800		1500	mV	1
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	5
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as ((V_{D+} + V_{D-})/2 - $V_{Tx\text{-}cm\text{-}dc\text{-}pin}$)	-0.0375		0.0375	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	2
$TX_{duty\text{-}pin}$	Average of absolute UI-UI jitter	-0.002		0.0025	UI	1
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7\text{-}pin}$	Absolute value of UI-UI jitter measured at Tx output pins with 1E-7 probability.	-0.007		0.0075	UI	3
$V_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Voltage eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	150		$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	mV	
$T_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Timing eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	0.9		1	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	0.48		0.52	UI	
VRx-CLK	Forward CLK Rx input voltage sensitivity (differential pp)			150	mV	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel	75		400	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: ((V_{D+} + V_{D-}/2 - $V_{RX\text{-}cm\text{-}dc\text{-}pin}$)	-50		50	mV	2

Notes:
1. The UI size is dependent upon the reference clock frequency
2. 1300mVpp swing is recommended when CPU to CPU length is within 2” of PDG max trace length. Note that default value is 1100mVpp.
3. Measure AC CM noise at the TX and decimate to its spectral components. For all spectral components above 3.2GHz, apply the attenuation of the channel at the appropriate frequency. If the resultant AC CM at the receiver is met after taking out the appropriate spectral component and it meets the RX AC CM spec then we can allow the transmitter AC CM noise to pass.
4. DC CM can be relaxed to 0.20 min and 0.30 max Vdiffp-p swing if RX has wide DC common mode range.

2.5.2.2 Requirements for 4.8 GT/s and 6.4 GT/s

Electrical specifications for Tx and Rx for 4.8 GT/s are captured in Table 2-13 and for 6.4 GT/s are captured in Table 2-14.

Table 2-13. Parameter Values for Intel QPI Channel at 4.8 GT/s (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800		1500	mV	1
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as ((V_{D+} + V_{D-})/2 - $V_{Tx\text{-}cm\text{-}dc\text{-}pin}$)	-0.0375		0.0375	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	2
$TX_{duty\text{-}pin}$	Average of UI-UI jitter.	-0.025		0.03	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability.	-0.065		0.07	UI	3
$TX_{jitUI\text{-}UI\text{-}1E\text{-}9\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability.	-0.07		0.076	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}7}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-7 probability.	0		0.15	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}9}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-9 probability.	0		0.17	UI	
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$V_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Voltage eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	225		1200	mV	
$T_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Timing eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI)	0.63		1	UI	

Table 2-13. Parameter Values for Intel QPI Channel at 4.8 GT/s (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		3	UI	
VRx-CLK	Forward CLK Rx input voltage sensitivity (differential pp)			180	mV	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel	125		350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$	-50		50	mV	2

Notes:
1. 1300mVpp swing is recommended when CPU to CPU length is within 2” of PDG max trace length. Note that default value is 1100mVpp.
2. Measure AC CM noise at the TX and decimate to its spectral components. For all spectral components above 3.2GHz, apply the attenuation of the channel at the appropriate frequency. If the resultant AC CM at the receiver is met after taking out the appropriate spectral components meets the RX AC CM spec then we can allow the transmitter AC CM noise to pass.
3. Measured with victim lane running clock pattern, neighboring aggressor lanes running DC pattern and far aggressor lanes running PRBS pattern.

Table 2-14. Parameter Values for Intel QPI at 6.4 GT/s (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800		1500	mV	1
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually $0.25*V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	38		47	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually $0.25*V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	38		47	Ω	
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.23		0.27	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	4
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as $((V_{D+} + V_{D-})/2 - V_{Tx\text{-}cm\text{-}dc\text{-}pin})$	-0.065		0.065	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	2
$TX_{duty\text{-}pin}$	Average of absolute UI-UI jitter	-0.0325		0.0325	UI	
$TX_{jitUI\text{-}UI\text{-}1E\text{-}7\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-7 probability.	-0.12		0.12	UI	3
$TX_{jitUI\text{-}UI\text{-}1E\text{-}9\text{-}pin}$	UI-UI jitter measured at Tx output pins with 1E-9 probability.	-0.137		0.137	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}7}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-7 probability.	0		0.2	UI	
$TX_{clk\text{-}acc\text{-}jit\text{-}N\_UI\text{-}1E\text{-}9}$	p-p accumulated jitter out of transmitter over 0 <= n <= N UI where N=12, measured with 1E-9 probability.	0		0.23	UI	

Table 2-14. Parameter Values for Intel QPI at 6.4 GT/s (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$V_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Voltage eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI).	155		1200	mV	2
$T_{Rx\text{-}diff\text{-}pp\text{-}pin}$	Timing eye opening at the end of Tx+ channel for any data or clock channel measured with a cumulative probability of 1E-9 (UI)	0.61		1	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		3	UI	
VRx-CLK	Forward CLK Rx input voltage sensitivity (differential pp)			150	mV	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel	90		350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$	-50		50	mV	

Notes:
1. 1300 mVpp swing is recommended when CPU to CPU length is within 2” of PDG max trace length. Note that default value is 1100mVpp.
2. Measure AC CM noise at the TX and decimate to its spectral components. For all spectral components above 3.2 GHz, apply the attenuation of the channel at the appropriate frequency. If the resultant AC CM at the receiver is met after taking out the appropriate spectral components meets the RX AC CM spec then we can allow the transmitter AC CM noise to pass.
3. Measured with victim lane running clock pattern, neighboring aggressor lanes running DC pattern and far aggressor lanes running PRBS pattern.
4. DC CM can be relaxed to 0.20 and 0.30 Vdiffp-p swing if RX has wide DC common mode range.

2.5.3 Intel SMI Signaling Specifications

This section defines the high-speed differential point-to-point signaling link for Intel SMI. The link consists of a transmitter and a receiver and the interconnect in between them. The specifications described in this section covers 6.4 Gb/s operation.

Reference Intel SMI high-speed differential PTP link is at 1.5 V.

2.5.4 Intel SMI Transmitter and Receiver Specifications

All TX-RX links are DC-coupled and the TX and RX pins adhere to the return loss specifications for continuous transmission operation.

Table 2-15. Parameter Values for Intel SMI at 6.4 GT/s and lower (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	Transmitter differential swing	800		1200	mV	
$Z_{TX\_LOW\_CM\_DC}$	DC resistance of Tx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
$Z_{RX\_LOW\_CM\_DC}$	DC resistance of Rx terminations at half the single ended swing (which is usually 0.25*$V_{Tx\text{-}diff\text{-}pp\text{-}pin}$) bias point	37		47	Ω	
VTx-diff-pp-CLK-pin	Transmitter differential swing using a CLK like pattern	0.9*min(VTx-diff-pp pin)		max(VTxdiff-pp-pin)	mV	1
$V_{Tx\text{-}cm\text{-}dc\text{-}pin}$	Transmitter output DC common mode, defined as average of V_{D+} and V_{D-}	0.20		0.30	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	3
$V_{Tx\text{-}cm\text{-}ac\text{-}pin}$	Transmitter output AC common mode, defined as ((V_{D+} + V_{D-})/2 - $V_{Tx\text{-}cm\text{-}dc\text{-}pin}$)	-0.20		0.20	Fraction of $V_{Tx\text{-}diff\text{-}pp\text{-}pin}$	
$TX_{duty\text{-}UI\text{-}pin}$	This is computed as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.	-0.0325		0.0325	UI	
TX1UI-Rj-NoXtalk-pin	Rj value of 1-UI jitter, using setup of Figure 2-7. With X-talk off, but on-die system like noise present. This extraction is to be done after software correction of DCD	0		0.008	UI	2
TX1UI-Dj-NoXtalk--pin	pp Dj value of 1-UI jitter With X-talk off, but on-die system like noise present.	-0.01		0.01	UI	2
TXN-UI-Rj-NoXtalkpin	Rj value of N-UI jitter. With X-talk off, but on-die system like noise present. Here 1 < N < 9.This extraction is to be done after software correction of DCD	0		0.012	UI	2
TXN-UI-Dj-NoXtalkpin	pp Dj value of N-UI jitter. With X-talk off, but on-die system like noise present. Here 1 < N < 9.Dj here indicated Djdd of dual-dirac fitting, after software correction of DCD	-0.04	0.04	0.2	UI	2
$T_{Tx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to clock lane, as measured at Tx output	-0.5		0.5	UI	
$T_{Rx\text{-}data\text{-}clk\text{-}skew\text{-}pin}$	Delay of any data lane relative to the clock lane, as measured at the end of Tx+ channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.	-1		3.5	UI	
VRx-CLK	Forward CLK Rx input voltage sensitivity (differential pp)			150	mV	
VRx-Vmargin	Any data lane Rx input voltage (differential pp) measured at BER=1E-9			100	mV	

Table 2-15. Parameter Values for Intel SMI at 6.4 GT/s and lower (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$T_{Rx\text{-}Tmargin}$	Timing width for any data lane using repetitive patterns (check validation conditions) and clean forwarded CLK, measured at BER=1E-9	0.8			UI	
$\Delta_{TRx\text{-}Tmargin\text{-}DCD\text{-}CLK}$	Magnitude of degradation of timing width for any data lane using repetitive patterns with DCD injection in forwarded CLK measured at BER=1E-9, compared to TRx-Tmargin. The magnitude of DCD is specified under validation conditions.			0.02	UI	
$\Delta_{TRx\text{-}Tmargin\text{-}Rj\text{-}CLK}$	Magnitude of degradation of timing width for any data lane using repetitive patterns with only Rj injection in forwarded CLK measured at BER=1E-9, compared to TRx-Tmargin. The magnitude of Rj is specified under validation conditions.			0.11	UI	
$\Delta_{TRx\text{-}Tmargin\text{-}DCD\text{-}Rj\text{-}CLK}$	Magnitude of degradation of timing width for any data lane using repetitive patterns with DCD and Rj injection in forwarded CLK measured at BER=1E-9, compared to TRx-Tmargin. The magnitude of DCD and Rj is specified under validation conditions.			0.12	UI	
$V_{Rx\text{-}cm\text{-}dc\text{-}pin}$	DC common mode ranges at the Rx input for any data or clock channel, defined as average of VD+ and VD-.	125		350	mV	
$V_{Rx\text{-}cm\text{-}ac\text{-}pin}$	AC common mode ranges at the Rx input for any data or clock channel, defined as: $((V_{D+} + V_{D-}/2 - V_{RX\text{-}cm\text{-}dc\text{-}pin})$	-50		50	mV	

Notes:

1. This is the swing specification for the forwarded CLK output. Note that this specification will also have to be suitably de-embedded for package/PCB loss to translate the value to the pad, since there is a significant variation between traces in a setup.
2. While the X-talk is off, on-die noise similar to that occurring with all the transmitter and receiver lanes toggling will still need to be present. When a socket is not present in the transmitter measurement setup, in many cases the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. Therefore for all Tx measurements, use of a socket should be avoided. The contribution of cross-talk may be significant and should be done using the same setup at Tx and compared against the expectations of full link signaling. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3. DC CM can be relaxed to 0.20 and 0.30 Vdiffp-p swing if RX has wide DC common mode range.

2.5.4.1 Summary of Transmitter Amplitude Specifications

Table 2-16. PLL Specification for TX and RX

Symbol	Parameter	Min	Max	Units	Notes
$F_{PLL\text{-}BW\_TX\text{-}RX}$	-3dB bandwidth	4	16	MHz	
$JitPk_{TX\text{-}RX}$	Jitter Peaking		3	dB	

Table 2-17. Transmitter Voltage Swing

Voltage Swing Setting	Mean $V_{TX-diffp-p-min}$	Mean $V_{TX-diffp-p-max}$	Units
110 (L)	850	1200	mV
100 (M)	700	1000	mV
010 (S)	600	850	mV

Table 2-18. Transmitter De-emphasis (Swing Setting 110: Large)

De-emphasis Range			Measured Values After Inverse Equalization			
De-emphasis Setting	$V_{TX-DE-ratio-min}$	$V_{TX-DE-ratio-max}$	Minimum Swing	Maximum Swing	Units	Normalized swing delta (max)
10.1 dB	9.3	11.0	680	1315	mV	0.450
8.5 dB	7.8	9.3	685	1305	mV	0.400
7.2 dB	6.6	7.8	700	1300	mV	0.390
6.0 dB	5.5	6.6	700	1285	mV	0.300
5.0 dB	4.5	5.5	700	1285	mV	0.290

Table 2-19. Transmitter De-emphasis (Swing Setting 100: Medium)

De-emphasis Range			Measured Values After Inverse Equalization			
De-emphasis Setting	$V_{TX-DE-ratio-min}$	$V_{TX-DE-ratio-max}$	Minimum Swing	Maximum Swing	Units	Normalized swing delta (max)
8.5 dB	7.8	9.3	555	1100	mV	0.420
7.2 dB	6.6	7.8	570	1095	mV	0.410
6.0 dB	5.5	6.6	570	1095	mV	0.320
5.0 dB	4.5	5.5	570	1095	mV	0.315
4.1 dB	3.7	4.5	570	1090	mV	0.295
3.3 dB	2.9	3.7	570	1090	mV	0.270

Table 2-20. Transmitter De-emphasis (Swing Setting 010: Small)

De-emphasis Range			Measured Values After Inverse Equalization			
De-emphasis Setting	$V_{TX-DE-ratio-min}$	$V_{TX-DE-ratio-max}$	Minimum Swing	Maximum Swing	Units	Normalized swing delta (max)
6.0 dB	5.5	6.6	485	930	mV	0.345
5.0 dB	4.5	5.5	485	930	mV	0.335
4.1 dB	3.7	4.5	485	930	mV	0.320
3.3 dB	2.9	3.7	485	930	mV	0.295
2.5 dB	2.1	2.9	485	930	mV	0.290
1.8 dB	1.5	2.1	485	930	mV	0.285

2.5.4.2 Summary of Transmitter Output Specifications

Table 2-21. Summary of Differential Transmitter Output Specifications

Symbol	Parameter	Min	Max	Units	Comments
$V_{TX-CM-Ratio}$	Ratio of V_{TX-CM} to measured $V_{TX-DIFFp-p\ (DC)}$	23	27	%	
$V_{TX-CM-AC-Ratio}$	Ratio of $V_{TX-CM-ACp-p}$ to measured $V_{TX-DIFFp-p\ (DC)}$		7.5	%	
V_{TX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D-	-75	750	mV	1, 2
T_{TX_TJ}	Transmitter total jitter		0.25		
T_{TX_DJ}	Transmitter dual-dirac deterministic jitter		0.15	UI	
T_{TX_PWS}	Transmitter pulse width shrinkage (data)		0.05		
$T_{TX\_CLK\_PWS}$	Transmitter pulse width shrinkage (forwarded clock)		0.018	UI	
$ER_{TX-RISE}$, $ER_{TX-FALL}$	Differential TX output edge rates	10	30	V/ns	Differential voltage levels at ±100 mV Measured as: Note 1
$RL_{TX-DIFF}$	Differential return loss	8		dB	Measured relative to 50 ohms over 0.1 GHz to 3.2 GHz.
RL_{TX-CM}	Common mode return loss	6		dB	Measured relative to 50 ohms over 0.1 GHz to 3.2 GHz.
R_{TX}	Transmitter termination resistance	37.4	47.6	Ω	
$L_{TX-SKEW}$	Lane-to-lane skew at TX		100 + 2 UI	ps	
$L_{TX-SKEW-CLK-DAT}$	TX clock-to-data skew	-0.2	0.2	ns	Forwarded clock delay - data delay
$L_{TOT-SKEW-CLK-DAT}$	Total system clock-to-data skew	-1.5	1.5	ns	
$T_{TX-DRIFT}$	Maximum TX Drift		240	ps	3
BER	Bit Error Ratio		10^{-12}		

Notes:
1. Specified at the package pins into a timing and voltage compliance test load.
2. The maximum value is specified to be at least $(V_{TX-DIFFp-p\ L} / 4) + V_{TX-CM\ L} + (V_{TX-CM-ACp-p} / 2)$
3. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.

2.5.4.3 Intel® SMI Differential Receiver Input Specifications

The receiver definition starts from the input pin of the receiver end package and therefore includes the package and the receiver end device.

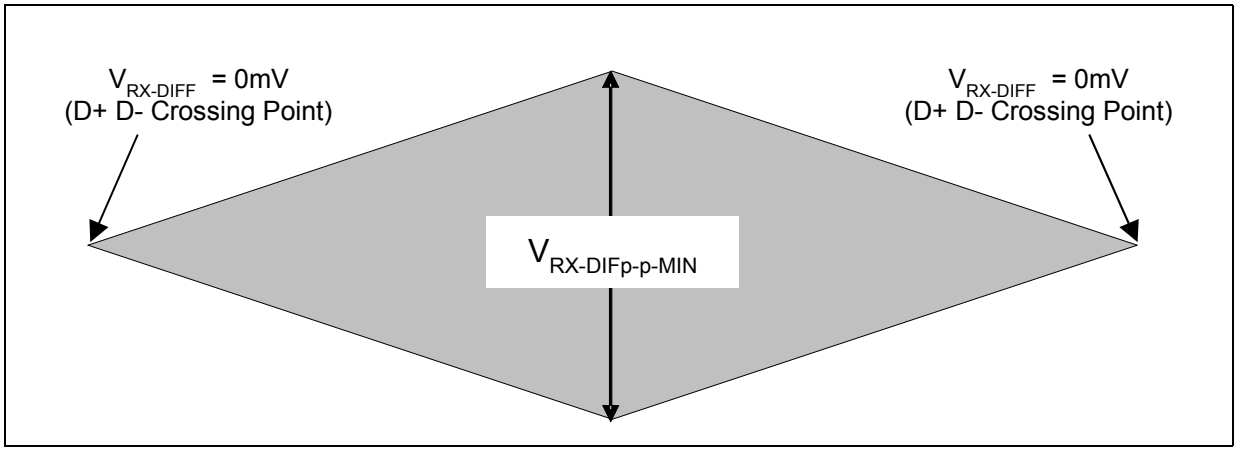
2.5.4.3.1 Receiver Input Compliance Eye Specification

Following the specification of the transmitter, the receiver is specified in terms of the minimum input eye height that must be maintained at the input to the receiver, and under which the receiver must function at the specified data rates. In addition to eye height, there are timing specifications that must also be met for both the data lanes and the forwarded clock.

The receiver eye is referenced to V_{SS} and all input terminations at the receiver must be referenced to V_{SS}. This input eye must be maintained for the entire duration of the RX test pattern. An appropriate average transmitter UI must be used as the interval for

measuring the eye diagram. The eye diagram is created using all edges of the RX test pattern. The eye diagrams shall be measured by observing a continuous pattern at the pin of the device. Note that the persistent eye diagram is used for determining conformance to voltage level specifications only.

Figure 2-9. Required Receiver Input Eye (Differential) Showing Minimum Voltage Specs



2.5.4.4 Receiver Input Timing

The figure of merit for receiver input timing is the RX eye width, represented by the symbol $T_{RX-Eye-Min}$. The receiver eye width is measured with respect to a delayed version of the transmitted forwarded clock, as described in Section 2.5.4.5.

2.5.4.5 Summary of Receiver Input Specifications

Table 2-22. Summary of Differential Receiver Input Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	115	1200	mV	$V_{RX-DIFFp-p}$ = 2*|V_{RX-D+} - V_{RX-D-}| Measured as: Note 1; see also Note 2
V_{RX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D-	-200	750	mV	3
$V_{RX-DIFF-PULSE}$	Single-pulse peak differential input voltage	85		mV	3, 4
$V_{RX-DIFF-ADJ-RATIO}$	Amplitude ratio between adjacent symbols, $V_{RX-DIFFp-p}$ <= 1100 mV		4.0		3, 5
$T_{RX-Eye-MIN}$	Minimum RX Eye Width	0.50		UI	3, 6, 7
$T_{RX-DJ-DD}$	Max RX eye closure due to dual-dirac deterministic jitter		0.40	UI	3, 6, 8, 9
$T_{RX-PW-ZC}$	Single-pulse width at zero-voltage crossing	0.55		UI	3, 4
$T_{RX-PW-ML}$	Single-pulse width at minimum-level crossing	0.2		UI	3, 4
$V_{RX-CM-MinEH}$	Common mode of the input voltage ($V_{RX-DIFFp-p}$ = $V_{RX-DIFFp-p-min}$)	120	310	mV	V_{RX-CM} = $DC_{(avg)}$ of |V_{RX-D+} + V_{RX-D-}|/2
$V_{RX-CM-EH-Ratio}$	Ratio of $V_{RX-DIFFp-p}$ increase to max DC common mode increase ($V_{RX-DIFFp-p}$ > $V_{RX-DIFFp-p-min}$)	1			$V_{RX-DIFFp-p}$ >= $V_{RX-DIFFp-p-min}$ + $V_{RX-CM-EH-Ratio}$ * (V_{RX-CM} - 310 mV)

Table 2-22. Summary of Differential Receiver Input Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{RX-CM-ABS}$	Common mode of the input voltage (Absolute max)		375	mV	V_{RX-CM} = $DC_{(avg)}$ of $\|V_{RX-D+} + V_{RX-D-}\|/2$
$V_{RX-CM-ACp-p}$	AC peak-to-peak common mode of input voltage		270	mV	$V_{RX-CM-AC}$ = Max $\|V_{RX-D+} + V_{RX-D-}\|/2$ – Min $\|V_{RX-D+} + V_{RX-D-}\|/2$ Measured as: Note 1
$V_{RX-CM-AC-EH-Ratio}$	Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$		45	%	11
$RL_{RX-DIFF}$	Differential return loss	9		dB	Measured over 0.1GHz to 3.2 GHz. See also Note 12
RL_{RX-CM}	Common mode return loss	6		dB	Measured over 0.1GHz to 3.2 GHz. See also Note 12
R_{RX}	RX termination resistance	37.4	47.6	Ohm	
$T_{RX-SKEW-CLK-DATA}$	RX skew between clock and data	0.0	1.0	ns	Forwarded clock delay - data delay
$T_{RX-DRIFT}$	Minimum RX Drift Tolerance	600		ps	14
$T_{FR-ENTRY -DETECT}$	Fast reset entry detect time		240	UI	
BER	Bit Error Ratio		10^{-12}		

Notes:
1. Specified at the package pins into a timing and voltage compliant test setup.
2. The $V_{RX-DIFFp-p}$ pin specification reflects a target eye height at the pad equal to 70 mV.
3. Specified at the package pins into a timing and voltage compliance test setup.
4. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eye mask.
5. The relative amplitude ratio limit between adjacent symbols prevents excessive inter-symbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
6. This number does not include the effects of SSC or reference clock jitter.
7. The $T_{RX-Eye-MIN}$ pin specification reflects a target eye width at the pad equal to 0.45 UI.
8. The $T_{RX-DJ-DD}$ pin specification reflects a target max deterministic jitter at the pad equal to 0.45 UI.
9. Defined as the dual-dirac deterministic jitter at the receiver input.
10. Allows for 15 mV DC offset between transmit and receive devices.
11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if $V_{RX-DIFFp-p}$ is 200 mV, the maximum AC peak-to-peak common mode is the lesser of (200 mV * 0.45 = 90 mV) and $V_{RX-CM-ACp-p}$.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance; tolerance over the entire signaling voltage range shall not exceed ± 5 Ω.
14. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.

2.6 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external thermal monitoring devices. The Intel Xeon Processor E7-8800/4800/2800 Product Families processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from T_{CC}

activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor die and DRAM temperatures, perform processor manageability functions, and manage processor interface tuning and diagnostics.

2.6.1 DC Characteristics

The PECI interface operates at a nominal voltage set by V_{IOC}. The set of DC electrical specifications shown in Table 2-23 is used with devices normally operating from a V_{IOC} interface supply. V_{IOC} nominal levels will vary between processor families. All PECI devices will operate at the V_{IOC} level determined by the processor installed in the system. For specific nominal V_{IOC} levels, refer to Table 2-23.

Table 2-23. PECI DC Electrical Limits

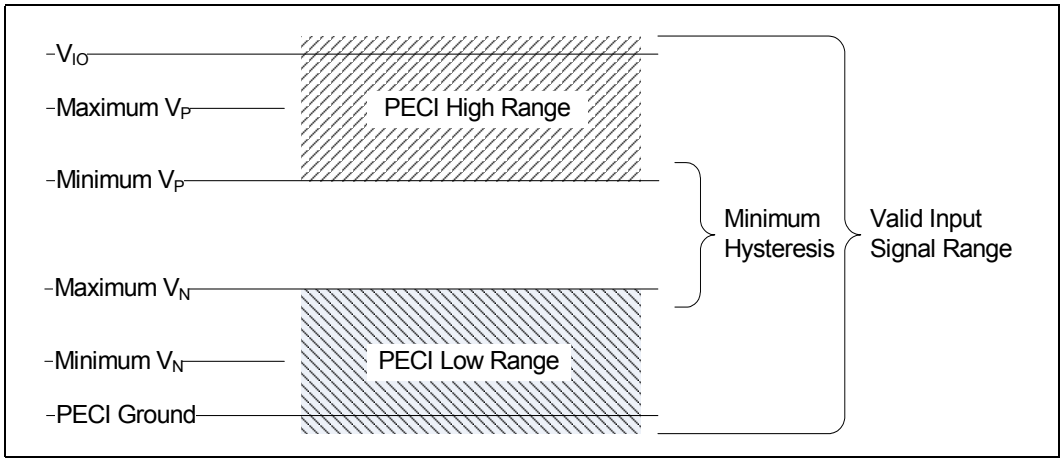
Symbol	Definition and Conditions	Min	Max	Units	Notes 1
V_{in}	Input Voltage Range	-0.150	V_{IOC} + 0.15	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{IOC}		V	
V_n	Negative-edge threshold voltage	0.275 * V_{IOC}	0.50 * V_{IoC}	V	2
V_p	Positive-edge threshold voltage	0.55 * V_{IOC}	0.725 * V_{IOC}	V	2
I_{sink}	Low level output sink (V_{OL} = 0.25 * V_{IOC})	0.5	1.0	mA	
I_{leak+}	High impedance state leakage to V_{IOC} (V_{leak} = V_{OL})	N/A	50	µA	3
I_{leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	25	µA	3
C_{bus}	Bus capacitance per node	N/A	10	pF	4,5
V_{noise}	Signal noise immunity above 300 MHz	0.1 * V_{IOC}	N/A	V_{p-p}	

Note:
1. V_{IOC} supplies the PECI interface. PECI behavior does not affect V_{IOC} min/max specifications.
2. It is expected that the PECI driver will take in to account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.15V to 0.275*V_{IOC} for the low level and 0.725*V_{IOC} to V_{IOC}+0.15 for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

2.6.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 2-10 as a guide for input buffer design.

Figure 2-10. Input Device Hysteresis



2.7 DC Specifications

Table 2-24. TAP, Strap Pins, Error, Powerup, RESET, Thermal, VID Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes 1
V_{IL}	Input Low Voltage	-0.1		0.54 * V_{IOF}	V	2,3
V_{IH}	Input High Voltage	0.86 * V_{IOF}			V	2
V_{OL}	Output Low Voltage			V_{IOC}* R_{ON} / (R_{ON} + R_{sys_term})	V	2,5
V_{OH}	Output High Voltage	V_{IOC}			V	2
Rtt	On Die Pull Up Termination	42.5	50	57.5	Ohm	
T_{CO}	T_{CO} time from SYSCLK pin till signal valid at output	0.5		2.9	ns	3
Setup Time	Control Sideband Input signals with respect to SYSCLK	900			ps	4
Hold Time	Control Sideband Input signals with respect to SYSCLK	900			ps	4
POC/ Reset Setup Time	Power-On Configuration Setup Time	2			SYSCLK	
POC/ Reset Hold Time	Power-On Configuration Hold Time	108			SYSCLK	
R_{ON}	Control Sideband Buffer on Resistance	8		18	Ohm	
I_{LI}	Input Leakage Current			± 200	µA	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{IO} referred to in these specifications refers to instantaneous V_{IO}.
3. Based on a test load of 50Ω to V_{IOC}.
4. Specified for synchronous signals.
5. R_{SYS_TERM} is the termination on the system, not part of the processor.
6. Intel® Trusted Execution Technology for Servers Input Leakage Current Maximum is ±50 uA.

Table 2-25. Miscellaneous DC Specifications

Pin	Parameter	Min	Typ	Max	Units	Notes 1
SKTID[2:0]	Input Low Voltage	<0.54 V_{IOC}			V	3
	Input High Voltage			>0.7 V_{CC}	V	2
	Leakage limit low			5	uA	3
	Leakage limit high			4.2	mA	2
THERMALERT	Leakage limit low			2.6	mA	3
	Leakage limit high			5	uA	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Recommended strapping high is 1K - 10K Ω.
3. Recommended strapping low is <100 Ω.

2.8 AC Specifications

The processor timings specified in this section are defined at the processor pads. Therefore, proper simulation of the signals is the only means to verify proper timing and signal quality.

Table 2-26 through Table 2-28 list the AC specifications associated with the processor. See Chapter 5 for signal definitions.

The timings specified in this section should be used in conjunction with the processor signal integrity models provided by Intel. Intel QPI, SMI and sideband layout guidelines are also available in the appropriate platform design guidelines.

Note: Care should be taken to read all notes associated with a particular timing parameter.

Table 2-26. System Reference Clock AC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Figure	Notes
f_{REFCLK} (SSC-off)	System Reference Clock frequency	133.29	133.33	133.37	MHz		
f_{REFCLK} (SSC-on)	System Reference Clock frequency	132.62	133.33	133.37	MHz		
T_{Rise}, T_{Fall}	Rise time, fall time.	175		700	ps		1, 2
$T_{Refclk\text{-}Dutycycle}$	Duty cycle of reference clock.	40	50	60	% period		3
$ER_{Refclk\text{-}diff\text{-}Rise}$, $ER_{Refclk\text{-}diff\text{-}Fall}$	Differential Rising and falling edge rates	1		4	V/ns		3, 4
C_I-CK	Clock Input Capacitance	0.2		1.0	pF		
VL	Differential Input Low Voltage			-0.15	V		3
VH	Differential Input High Voltage	0.15			V		3
V_{cross}	Absolute Crossing Point	0.25	0.35	0.55	V		1, 5, 6
V_{cross}(rel)	Relative Crossing Point	0.25 + 0.5*(VH_{avg} - 0.700)		0.55 + 0.5*(VH_{avg} - 0.700)			5, 7
V_{cross} Delta	V_{cross} variation	-	-	0.14	V		1, 5, 8
V_{max} (Absolute Overshoot)	Single-ended maximum voltage	-	-	1.15	V		1, 9

Table 2-26. System Reference Clock AC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Unit	Figure	Notes
V_{min} (Absolute Undershoot)	Single-ended minimum voltage	-0.3	-	-	V		1, 10
VRB-Diff	Differential ringback voltage threshold	-100		100	mV		3, 11
T_{Stable}	Allowed time before ringback	500			ps		3, 11

Notes:
1. Measurement taken from single ended waveform.
2. Rise and Fall times are measured single ended between 245 mV and 455 mV of the clock swing.
3. Measurement taken from differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFLCLK). The signal must be monotic through the measurement region for rise and fall time. The 300 mV measurement window is centred on the differential zero crossing. See Figure 2-25
5. Measured at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge REFCLK-. See Figure 2-26.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-26.
7. VHavg is the statistical average of the VH measured by the oscilloscope. The purpose of defining relative crossing point voltages is to prevent a 250 mV Vcross with a 850 mV VH. Also this prevents the case of a 550 mV Vcross with a 660 mV VH. See Figure 2-21.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in Vcross for any particular system. See Figure 2-27.
9. Defined as the maximum instantaneous voltage including overshoot. See Figure 2-26.
10. Defined as the minimum instantaneous voltage including overshoot. See Figure 2-26.
11. TStable is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV range. See Figure 2-22.

Table 2-27. Miscellaneous GTL AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1, 2
Asynchronous GTL input pulse width	8		SYSCLKs		
ERROR[0]_N, ERROR[1]_N, THERMTRIP_N, PROCHOT_N Output Edge Rate	0.7	2.3	V/ns		1, 3
ERROR[0]_N pulse width	16	16	b-clocks		
MEM_THROTTLE0_N, MEM_THROTTLE1_N, Intel TXT, RUNBIST, Input Edge Rate	0.5		V/ns		
FORCE_PR_N pulse width	500		µs	2-18	
PROCHOT_N pulse width	500		µs	2-18	
PWRGOOD rise time		20	ns		
PWRGOOD, RESET_N, FORCE_PR_N, ERROR[0]_N, ERROR[1]_N, SKTDIS_N Input Edge Rates	0.1		V/ns		2, 3, 4
RESET_N hold time w.r.t SYSCLK/SYSCLK_N		0.5	ns	2-11	5
RESET_N pulse width while PWRGOOD is active	1		ms		
SYSCLK stable to PWRGOOD assertion	10		SYSCLK		
THERMTRIP_N assertion until Vcc, and VCCCACHE removal		500	ms	2-12	
Vcc stable to PWRGOOD assertion	0.05	500	ms		
V_{REG} stable to PWRGOOD assertion	1		ms		
V_{IO} stable to VIOPWRGOOD assertion	1	500	ms		
VIOPWRGOOD de-assertion to V_{io} outside specification	100		ns		
VIOPWRGOOD rise time		20	ns		
PWRGOOD assertion to RESET_N de-assertion	34		ms		

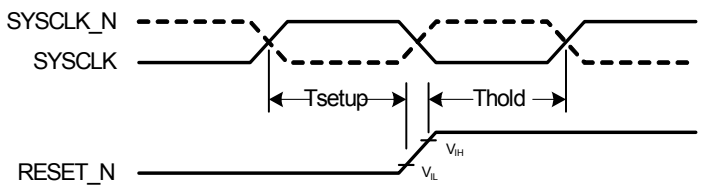
Notes:
1. These values are based on driving a 50Ω transmission line into a 50Ω pullup.
2. Deterministic reset.
3. Inspection range is VIL Max to VIH Min. When a signal ledge presents between VIL and VIH region, measure the first edge rate from VIL (or VIH) to the first inflection point, then measure the second edge rate from the second inflection point to VIH (or VIL) and divide the sum of the two edge rates by two, to generate the final edge rate number.
4. Error signals are 0.1 V/ns if non-monotonic, and 0.05 V/ns if monotonic.
5. For production platforms, reset determinism is not required.

Table 2-28. VID Signal Group AC Specifications

T # Parameter	Min	Max	Unit	Figure	Notes 1, 2
VID Step Time	-	-	µs	2-29	
VID Down Transition to Valid V_{CCP} (min)	-	-	µs	2-28,2-29	
VID Up Transition to Valid V_{CCP} (min)	-	-	µs	2-28,2-29	
VID Down Transition to Valid V_{CCP} (max)	-	-	µs	2-28,2-29	
VID Up Transition to Valid V_{CCP} (max)	-	-	µs	2-28,2-29	

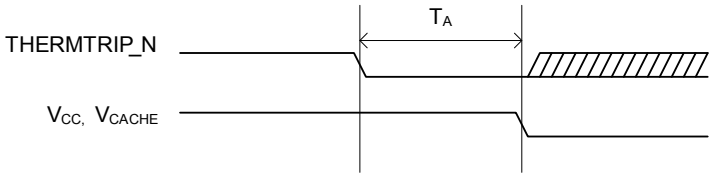
Notes:
1. See *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for addition information.
2. Platform support for VID transitions is required for the processor to operate within specifications.

Figure 2-11. RESET_N SEtup/Hold Time for Deterministic RESET_N Deassertion



Note: Deterministic RESET_N is defined for RESET_N deassertion only (coming out of RESET_N)

Figure 2-12. THERMTRIP_N Power Down Sequence



T_A = THERMTRIP_N assertion until V_{CC} and V_{CACHE} removal

Figure 2-13. VID Step Times

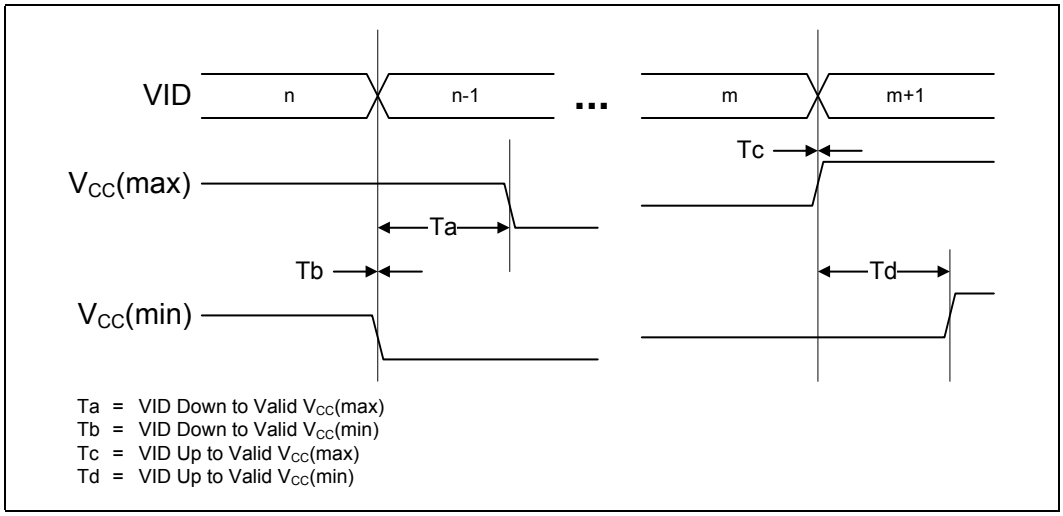


Table 2-29. SMBus and SPDBus Signal Group AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes 1, 2
Transmitter and Receiver Timings						
F_{SMB}	SMBCLK Frequency	10	100	kHz		
TCK	SMBCLK Period	10	100	µs		
t_{LOW}	SMBCLK High Time	4		µs	2-14	
t_{HIGH}	SMBCLK Low Time	4.7		µs	2-14	
t_R	SMBus Rise Time		1	µs	2-14	3
t_F	SMBus Fall Time		0.3	µs	2-14	3
T_{AA}	SMBus Output Valid Delay	0.1	4.5	µs	2-15	
$t_{SU;DAT}$	SMBus Input Setup Time	250		ns	2-14	
$t_{HD;DAT}$	SMBus Input Hold Time	0		ns	2-14	
Vil, SMBus	SMBus Vil	-0.3	Vcc33 x 0.3	V		
Vih, SMBus	SMBus Vih	Vcc33 x 0.7	Vcc33 + 0.5	V		
Vol, SMBus	SMBus Vol Vcc >2.5		0.4	V		
	SMBus Vol Vcc <= 2.5		0.2	V		
t_{BUF}	Bus Free Time between Stop and Start Condition	4.7		µs	2-14	4, 5
$t_{HD;STA}$	Hold Time after Repeated Start Condition	4.0		µs	2-14	
$t_{SU;STA}$	Repeated Start Condition Setup Time	4.7		µs	2-14	
$t_{SU;STD}$	Stop Condition Setup Time	4.0		µs	2-14	

Notes:
1. These parameters are based on design characterization and are not tested.
2. All AC timings for the SMBus signals are referenced at V_{IL_MAX} or V_{IL_MIN} and measured at the processor pins. Refer to Figure 2-14.
3. Rise time is measured from (V_{IL_MAX} - 0.15V) to (V_{IH_MIN} + 0.15V). Fall time is measured from (0.9 * VCC33) to (V_{IL_MAX} - 0.15V).
4. Minimum time allowed between request cycles.
5. Following a write transaction, an internal write cycle time of 10ms must be allowed before starting the next transaction.

Figure 2-14. SMBus Timing Waveform

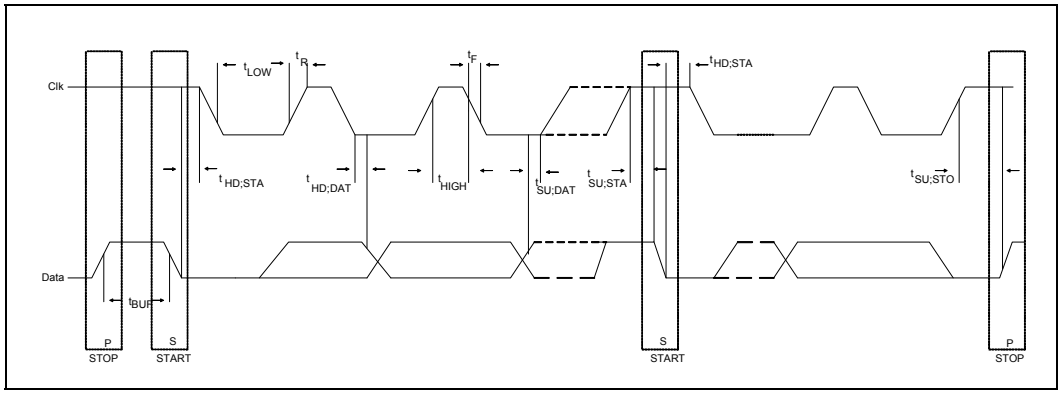


Figure 2-15. SMBus Valid Delay Timing Waveform

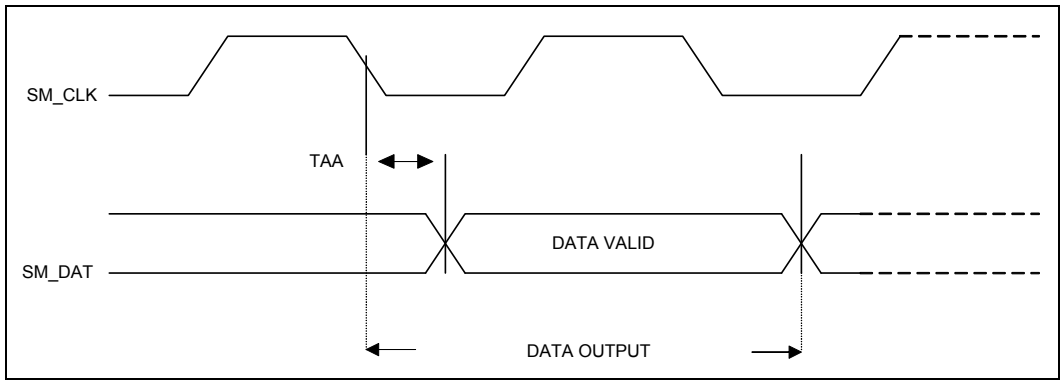


Table 2-30. FLASHROM Signal Group AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
$F_{FLASHROM}$	FLASHROM_CLK Frequency	0	66.67	MHz		
$Slew_{DATAI}$	FLASHROM_DATI Edge Rate	0.5		V/ns		1
$Slew_{DATAO}$	FLASHROM_DATO Edge Rate	0.7	2.3	V/ns		2
t_{CS_AS}	FLASHROM_CS[3:0]_N assertion before first FLASHROM_CLK	10		ns	2-16	
t_{CS_DE}	FLASHROM_CS[3:0]_N deassertion after last FLASHROM_CLK	12		ns	2-16	
t_{SETUP}	FLASHROM_DATI setup time	6		ns	2-16	
t_{HOLD}	FLASHROM_DATI hold time	0		ns	2-16	
t_{DELAY}	FLASHROM_DATO Valid Delay	–2.0	2.0	ns	2-16	

Notes:
1. All input edge rates are specified between V_{IL}(max) and V_{IH}(min), and output edge rates are specified between V_{OL}(max) and V_{OH}(min).
2. These values are based on driving a 50Ω transmission line into a 50Ω pullup.

Figure 2-16. FLASHROM Timing Waveform

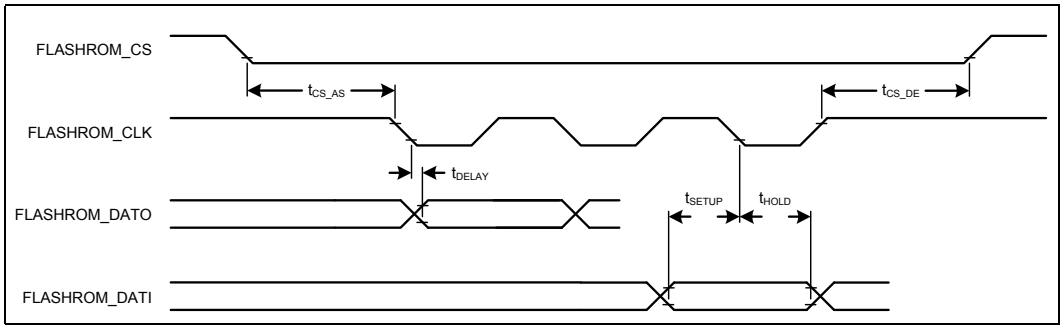


Table 2-31.TAP Signal Group AC Timing Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes 1, 2
Transmitter and Receiver Timings						
F_{TAP}	TCK Frequency		66	MHz	2-17	3
T_p	TCK Period	15		ns		
T_S	TDI, TMS Setup Time	7.5		ns	2-17	4, 5
T_H	TDI, TMS Hold Time	7.5		ns	2-17	4, 6
T_X	TDO Clock to Output Delay	7.5	24	ns	2-17	6
	TRST_N Assert Time	30		ns	2-18	7

Notes:
1. Not 100% tested. These parameters are based on design characterization.
2. It is recommended that TMS be asserted while TRST_N is being deasserted.
3. This specification is based on the capabilities of the ITP-XDP debug port tool, not on processor silicon.
4. Referenced to the rising edge of TCK.
5. Specification for a minimum swing defined between TAP V_{T-} to V_{T+}. This assumes a minimum edge rate of 0.5 V/ns.
6. Referenced to the falling edge of TCK.
7. TRST_N must be held asserted for 2 TCK periods to be guaranteed that it is recognized by the processor.

Figure 2-17. TAP Valid Delay Timing Waveform

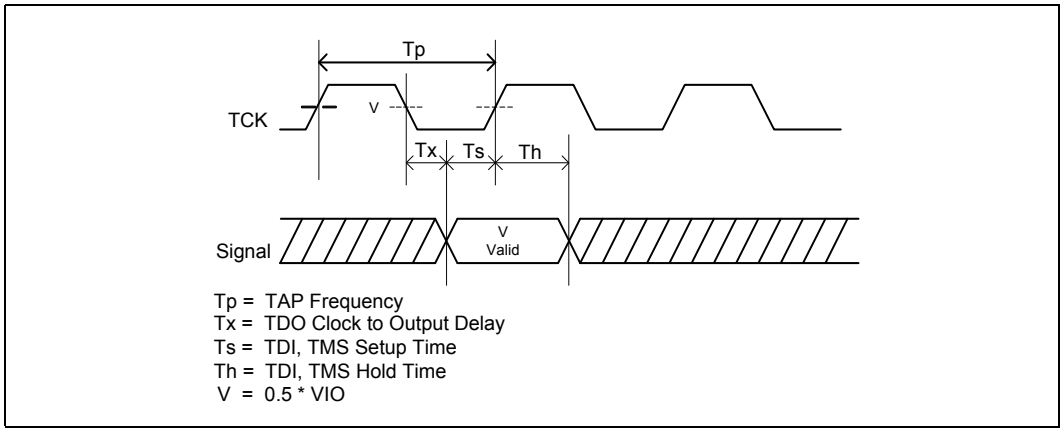
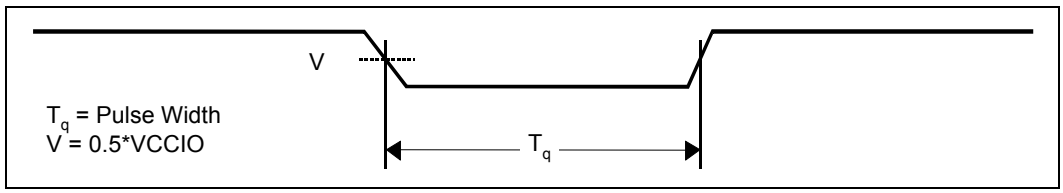


Figure 2-18. Test Reset (TRST_N), Force_PR_N, RESET_N and PROCHOT_N Pulse Width Waveform



2.9 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 2-26 through Table 2-28.

Note: For Figure 2-21 through Figure 2-29, the following apply:

- All common clock AC timings signals are referenced to the Crossing Voltage (V_{CROSS}) of the SYSCLK_DP, SYSCLK_DN at rising edge of SYSCLK_DP.
- All source synchronous AC timings are referenced to their associated strobe (address or data). Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe.
- All AC timings for the TAP signals are referenced to the TCK at 0.5 * V_{IO} at the processor lands. All TAP signal timings (TMS, TDI, and so on) are referenced at 0.5 * V_{IO} at the processor die (pads).
- All CMOS signal timings are referenced at 0.5 * V_{IO} at the processor lands.

The Intel QPI electrical test setup are shown in figures Figure 2-19 and Figure 2-20.

Figure 2-19. Intel QPI System Interface Electrical Test Setup for Validating Standalone TX Voltage and Timing Parameters

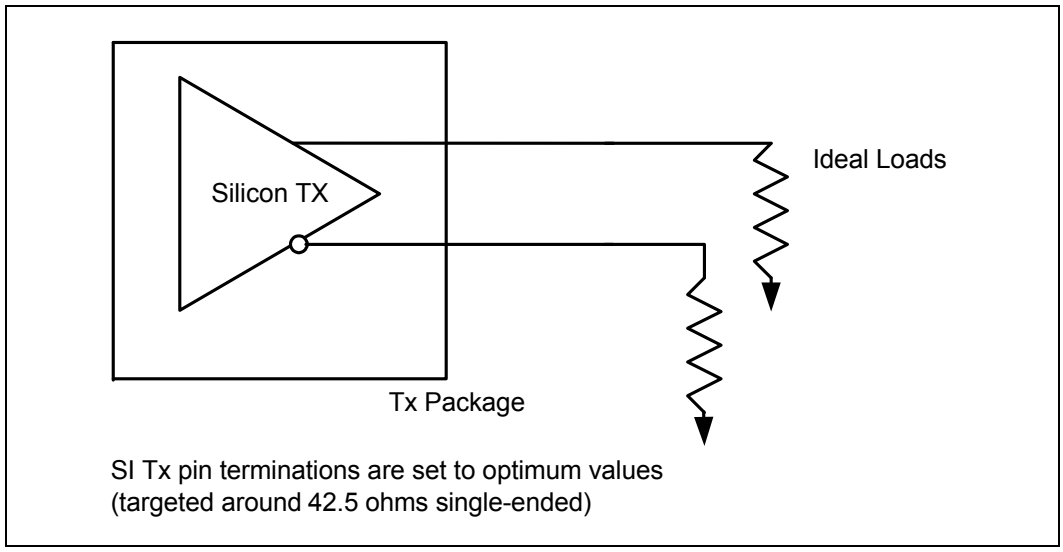


Figure 2-20. Intel QPI System Interface Electrical Test Setup for Validating TX + Worst-Case Interconnect Specifications

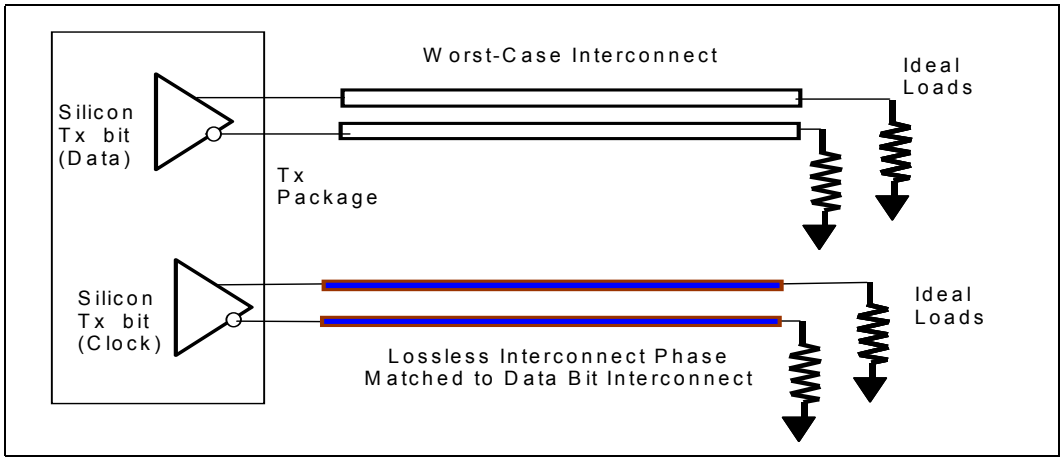


Figure 2-21. Differential Clock Waveform

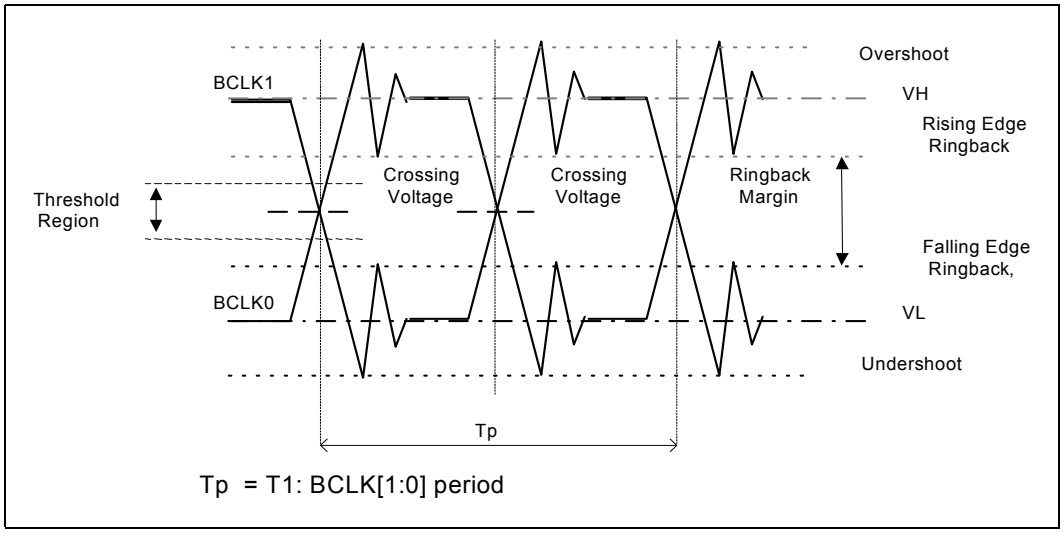


Figure 2-22. Differential Clock Crosspoint Specification

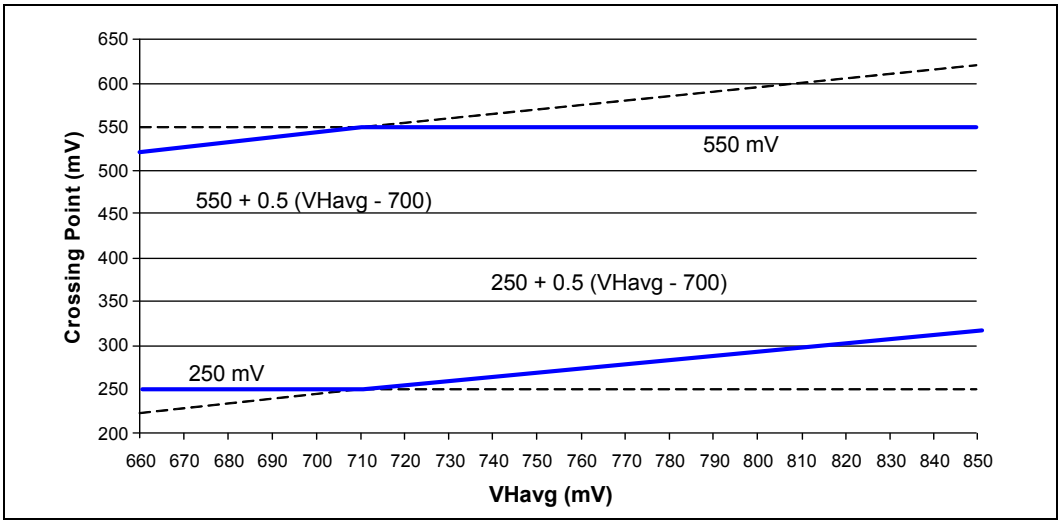


Figure 2-23. System Common Clock Valid Delay Timing Waveform

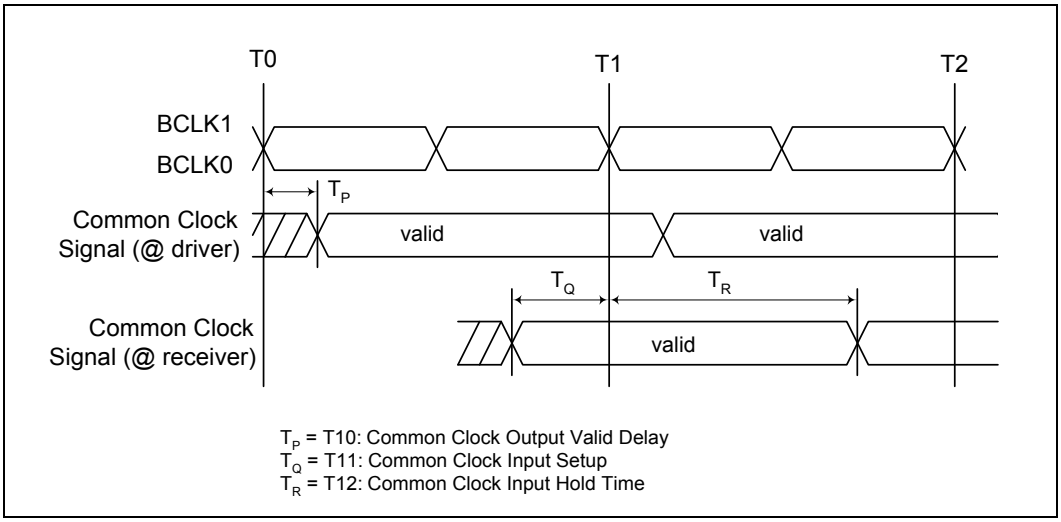


Figure 2-24. Differential Measurement Point for Ringback

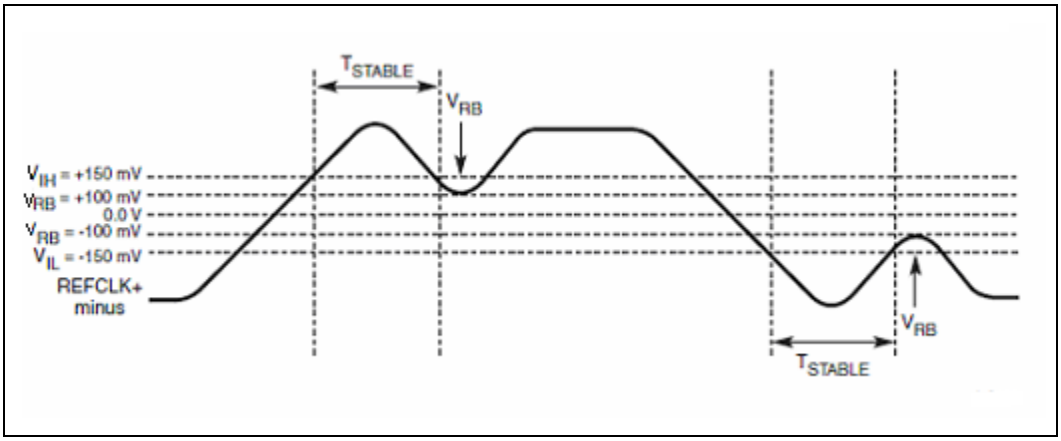


Figure 2-25. Differential Measurement Points for Rise and Fall time

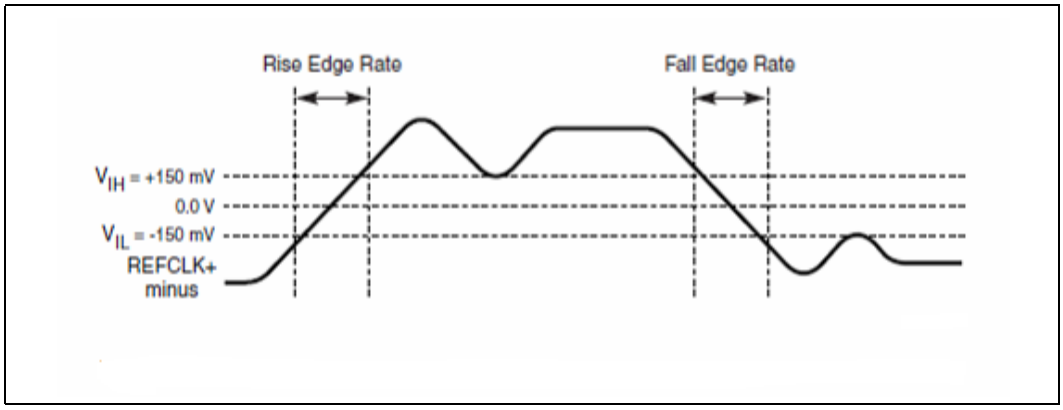


Figure 2-26. Single-Ended Measurement Points for Absolute Cross Point and Swing

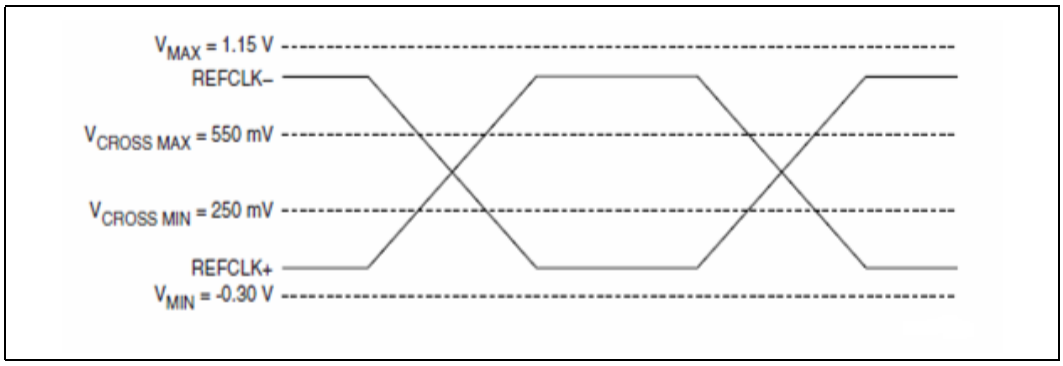


Figure 2-27. Single-Ended Measurement Points for Delta Cross Point

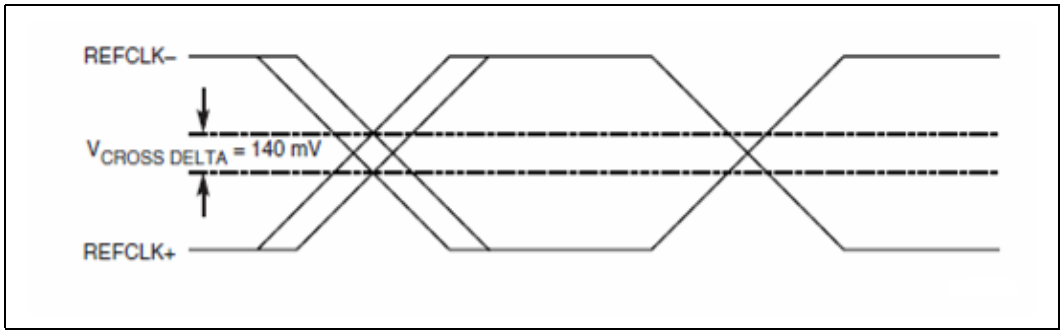
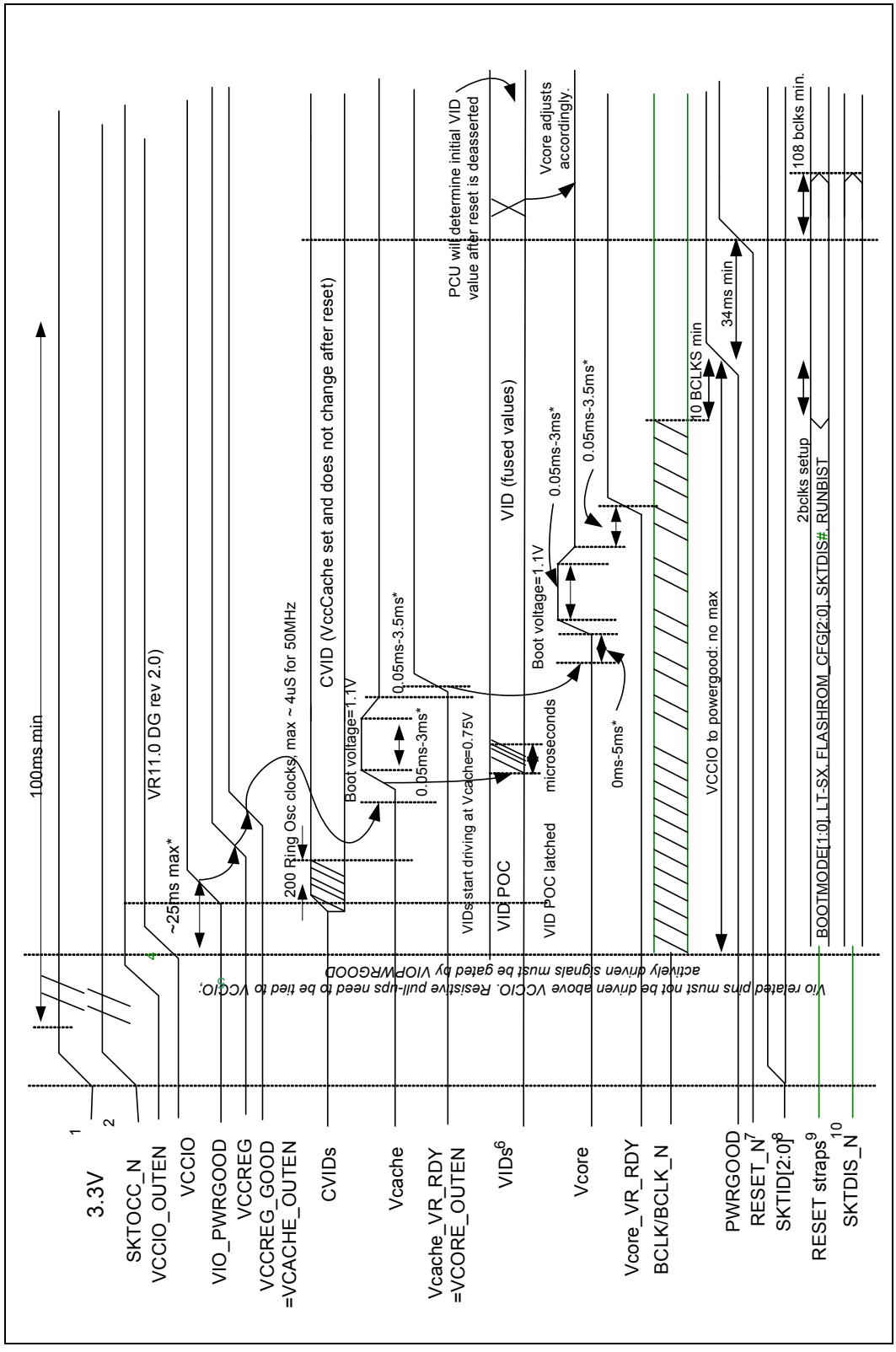


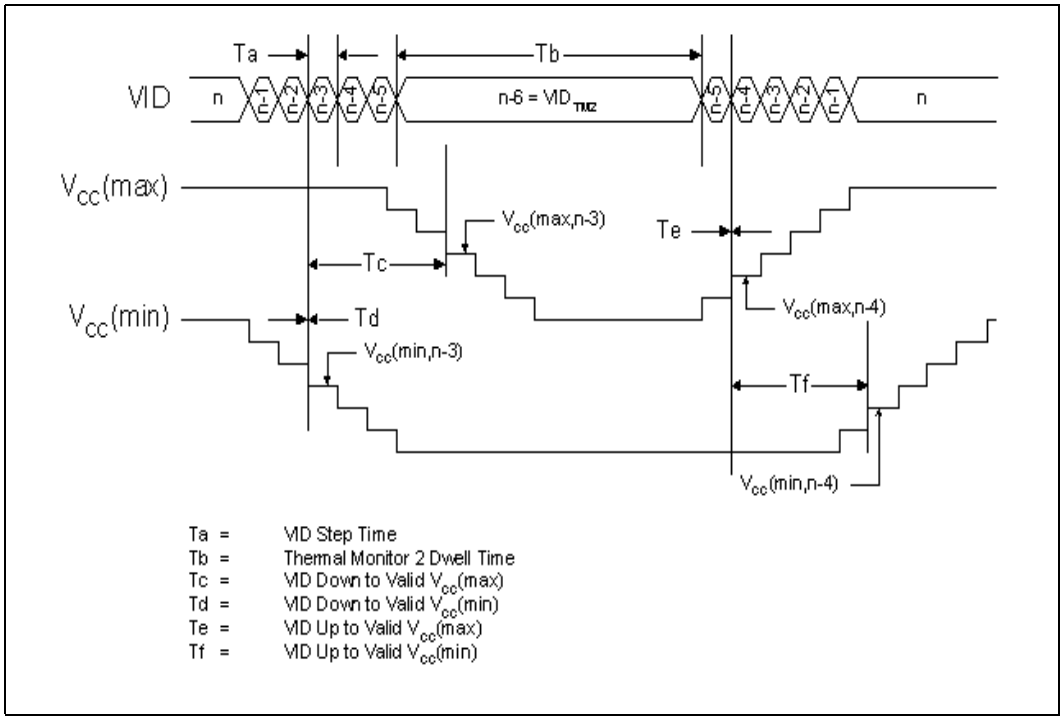
Figure 2-28. Voltage Sequence Timing Requirements



Note:

1. 3.3 V supplies power to on-package parts, including the PIROM/OEM scratch pad. 3.3V must be up at a minimum of 100ms before PWRGOOD is asserted.
2. SKTOCC_N is pulled to an appropriate platform rail; when socket is occupied, package pulls the signal to VSS. Here, SKTOCC_N is assumed pulled to 3.3 V.
3. VIOVIDs are pulled up to an appropriate platform rail. The package pulls appropriate VIO VIDs to VSS.
4. For integrated memory, Millbrook is sequenced after VIO is true. System implementation decides whether installed hot plug memory cards are sequenced with or after system power is up.
5. SMB, SM_WP, SPD, SKTID inputs/bidir are 3.3 V-rail related pins. All other misc IO are VIO-related, including other strapping pins (BOOTMODE pins), INT and error (BIDIR). Vio related pins must not be driven above VCCIO. Resistive pull-ups need to be tied to VCCIO; actively driven signals must be gated by VIOPWRGOOD.
6. Weak pullups/downs assumed on VID pins, for VID POC sampling.
7. Reset_N is an asynchronous input for normal production usage.
8. SKTID must be valid with 3.3V for proper PIROM/OEM scratch pad addressing and must stay valid. SKTID is latched by processor only on a PWRGOOD toggle. SKTID must be driven valid before the assertion of PWRGOOD on a cold-reset.
9. RESET straps: During all resets, reset-latched straps must meet the following setup and hold. Cold reset: Must be stable 2 bclks prior to assertion of PWRGOOD and Reset Warm reset: Must be stable 2 bclks prior to assertion of Reset Hold time: Must be stable 108 bclks hold after deassertion of Reset. Reset-latched straps include BOOTMODE, Intel® Trusted Execution Technology for Servers, FLASHROM_CFG[2:0], SKTDIS_N, and RUNBIST. BOOTMODE & Intel TXT pins are latched only after a processor cold-reset (that is, system power-up or PWRGOOD-reset). RUNBIST: Is reset-deassertion latched. It is a dynamic signal. (system can assert, during runtime but must meet reset setup/hold requirements).
10. SKTDIS_N has no affect on inputs. It also has no impact to SMB pins and package-strapped pins (SKTOCC_N, PROCID_N). The following outputs are not tri-stated by SKTDIS#: TDO, PSI_N, PSI_CACHE_N, VIDs, and CVIDs. SKTDIS_N is transparent while reset is asserted. SKTDIS_N is latched at reset assertion. NOTE: SKTDIS_N has no impact on internal logic (logic is not disabled). A PWRGOOD-reset might be required when the SKT is "enabled" again.
11. * indicates a VR11.1 value.
12. Suggested normal power down should have the opposite sequence. At the minimum, Intel Xeon Processor E7-8800/4800/2800 Product Families processor VRs can be disabled in parallel subject to the power rail's capacitive drain time.
13. In order to ensure Timestamp Counter (TSC) synchronization across sockets in multi-socket systems, the RESET# de-assertion edge should arrive at the same BCLK rising edge on all sockets and should meet Tsu (setup) and Th (hold) requirements. This is relative to the first cold reset in the system. The delay from cold to any warm reset needs to be the same on each socket.

Figure 2-29. VID Step Times and Vcc Waveforms



2.10 Flexible Motherboard Guidelines

The Flexible Motherboard (FMB) guidelines are estimates of the maximum ratings that the Intel Xeon Processor E7-8800/4800/2800 Product Families processor will have over certain time periods. The ratings are only estimates as actual specifications for future processors may differ. The VR 11.1 specification is developed to meet FMB Voltage Specification values required by all Intel Xeon Processor E7-8800/4800/2800 Product Families processor SKUs.

2.11 Reserved (RSVD) or Unused Signals

All Reserved signals must be left unconnected on the motherboard. Any deviation in connection of these signals to any power rail or other signals can result in component malfunction or incompatibility with future processors. See Chapter 4 for socket land listing of the processor and the location of all signals, including RSVD signals.

Unused Intel QPI or Intel SMI input ports may be left as no-connects.

2.12 Test Access Port Connection

The recommended TAP connectivity will be detailed in an upcoming document release.

2.13 Mixing Processors

Intel supports and validates multiple processor configurations only in which all processors operate with the same Intel QPI frequency, core frequency, power segment, have the same number of cores, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

2.14 Processor SPD Interface

The processor SPD Interface is used for memory initialization including the set up and use of the memory thermal sensor on-board the Intel® 7500 scalable memory buffer. Base board management controllers (BMC) can use the PECI interface to the SPD engine for access to this thermal data.

The SPD master in the processor supports 100 kHz operation and the following set of commands:

Send Byte and Receive Byte

Write Byte and Read Byte

Write Word and Read Word

The SPD Interface does not support bus arbitration or clock stretching.

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3 Processor Package Mechanical Specifications

3.1 Package Mechanical Specifications

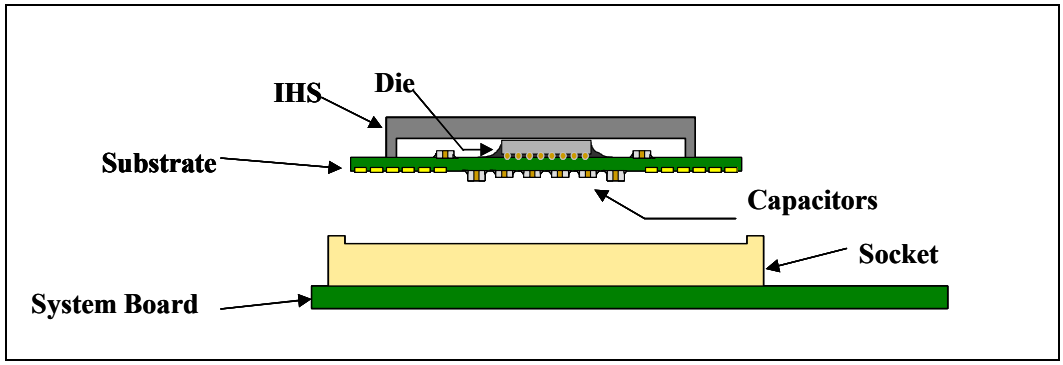
The processor is packaged in a Flip-Chip Land Grid Array (FC-LGA8) package that interfaces with the motherboard via an LGA1567 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 3-1 shows a sketch of the processor package components and how they are assembled together.

Note: Processor package mechanical information and drawings provided in this section are preliminary and subject to change.

The package components shown in Figure 3-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Processor core (die)
3. Package substrate
4. Capacitors

Figure 3-1. Processor Package Assembly Sketch



Note:
1. Socket and motherboard are included for reference and are not part of processor package.

3.1.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 3-2 and Figure 3-3. The drawings include dimensions necessary to design a thermal solution for the processor. All drawing dimensions are in mm. These dimensions include:

1. Package reference with tolerances (total height, length, width, etc.)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums

Figure 3-2. Processor Package Drawing (Sheet 1 of 2)

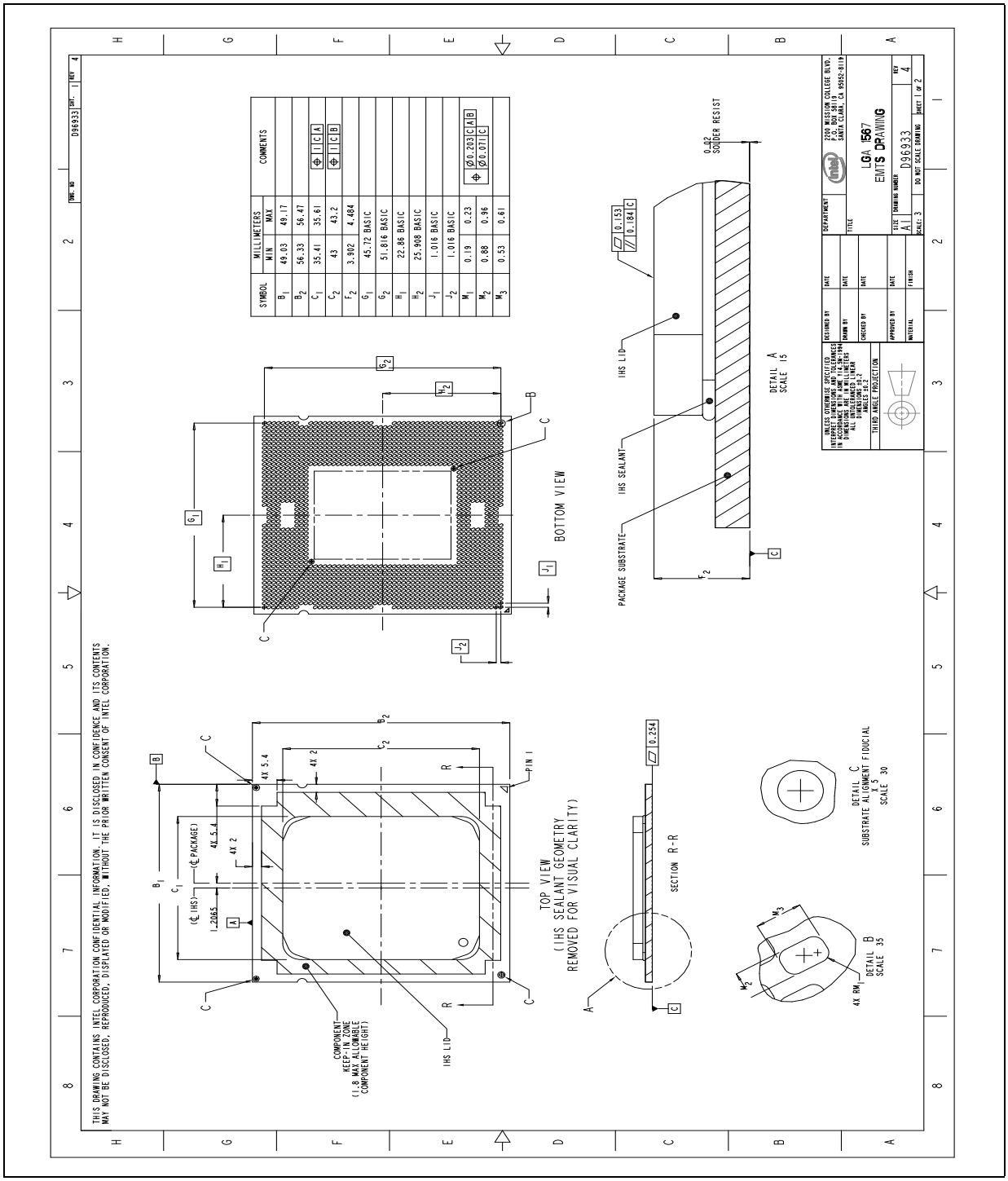
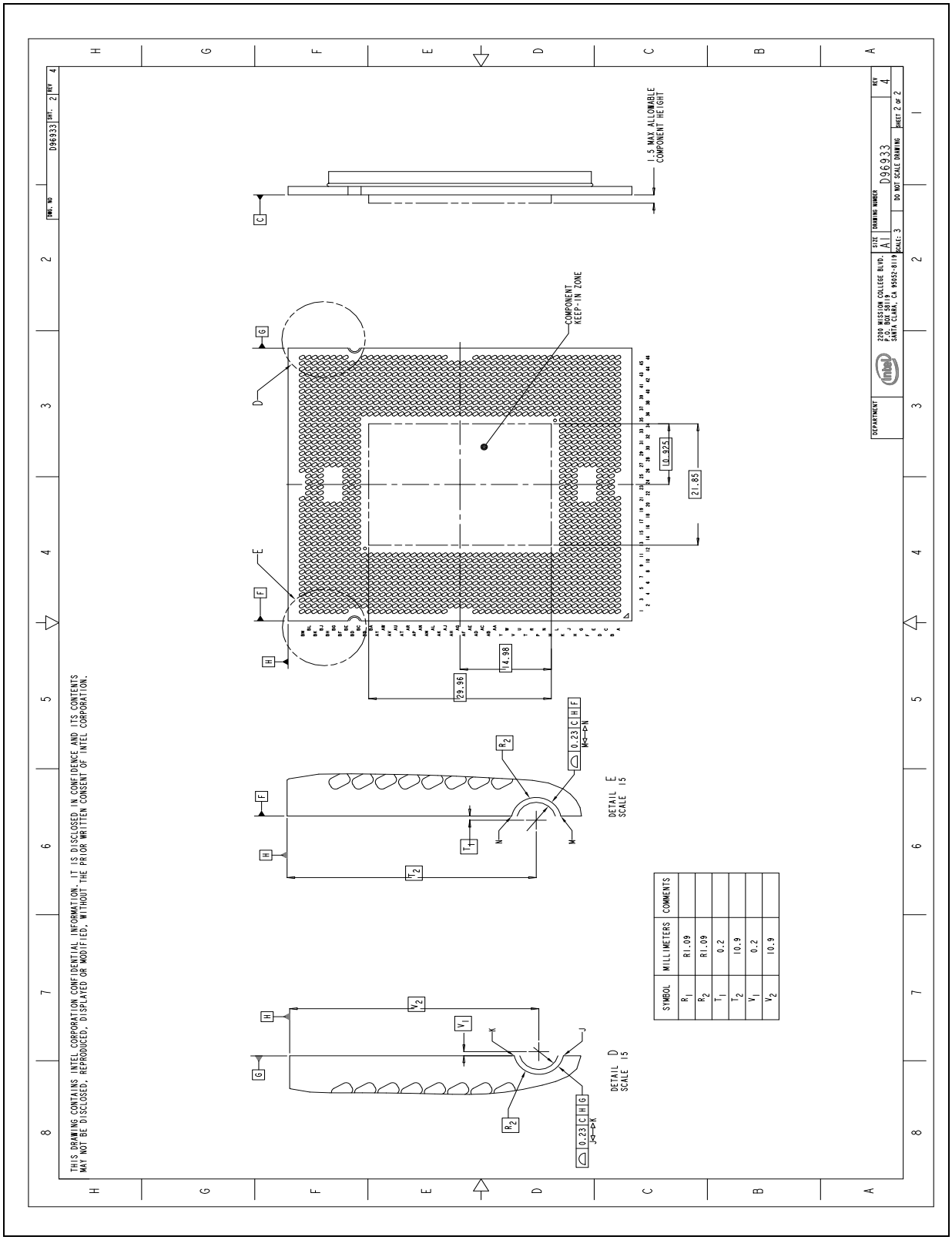


Figure 3-3. Processor Package Drawing (Sheet 2 of 2)



3.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 3-2 and Figure 3-3 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

3.1.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution. The minimum loading specification must be maintained by any thermal and mechanical solutions.

Table 3-1. Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	755 N	Allowable load on the package IHS See notes 1, 2, 3
Dynamic Compressive Load	490 N	See notes 1, 3, 4
Transient Bend Load	778 N	See note 4

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. Dynamic loading is defined as an 11-ms duration average load superimposed on the static load requirement.

3.1.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum	Notes
Shear	355 N	
Tensile	155 N	
Torque	7.9 N-m	

3.1.5 Package Insertion Specifications

The processor can be inserted into and removed from an LGA1567 socket 15 times.

3.1.6 Processor Mass Specification

The typical mass of the processor is ~40g. This mass [weight] includes all the components that are included in the package.

3.1.7 Processor Materials

Table 3-3 lists some of the package components and associated materials.

Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

3.1.8 Processor Markings

Figure 3-4 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 3-4. Processor Top-Side Markings

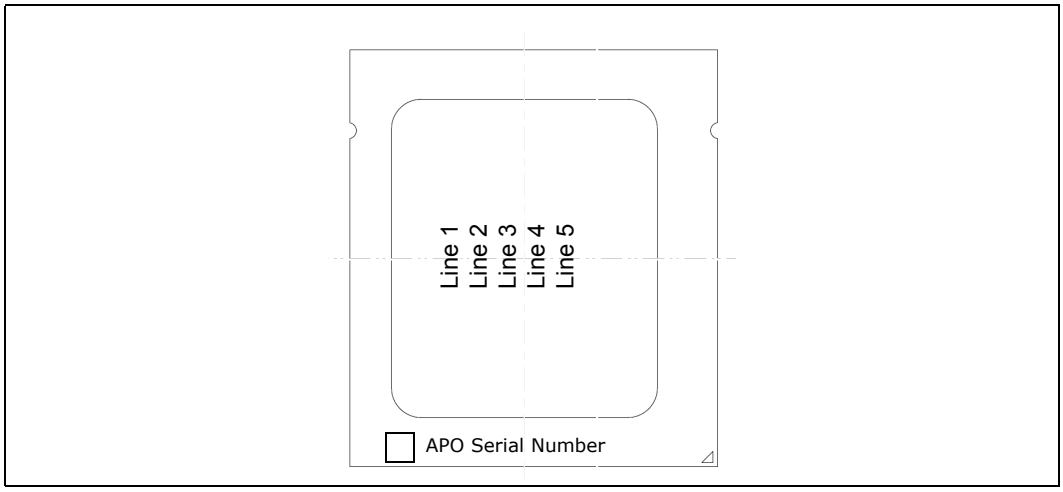


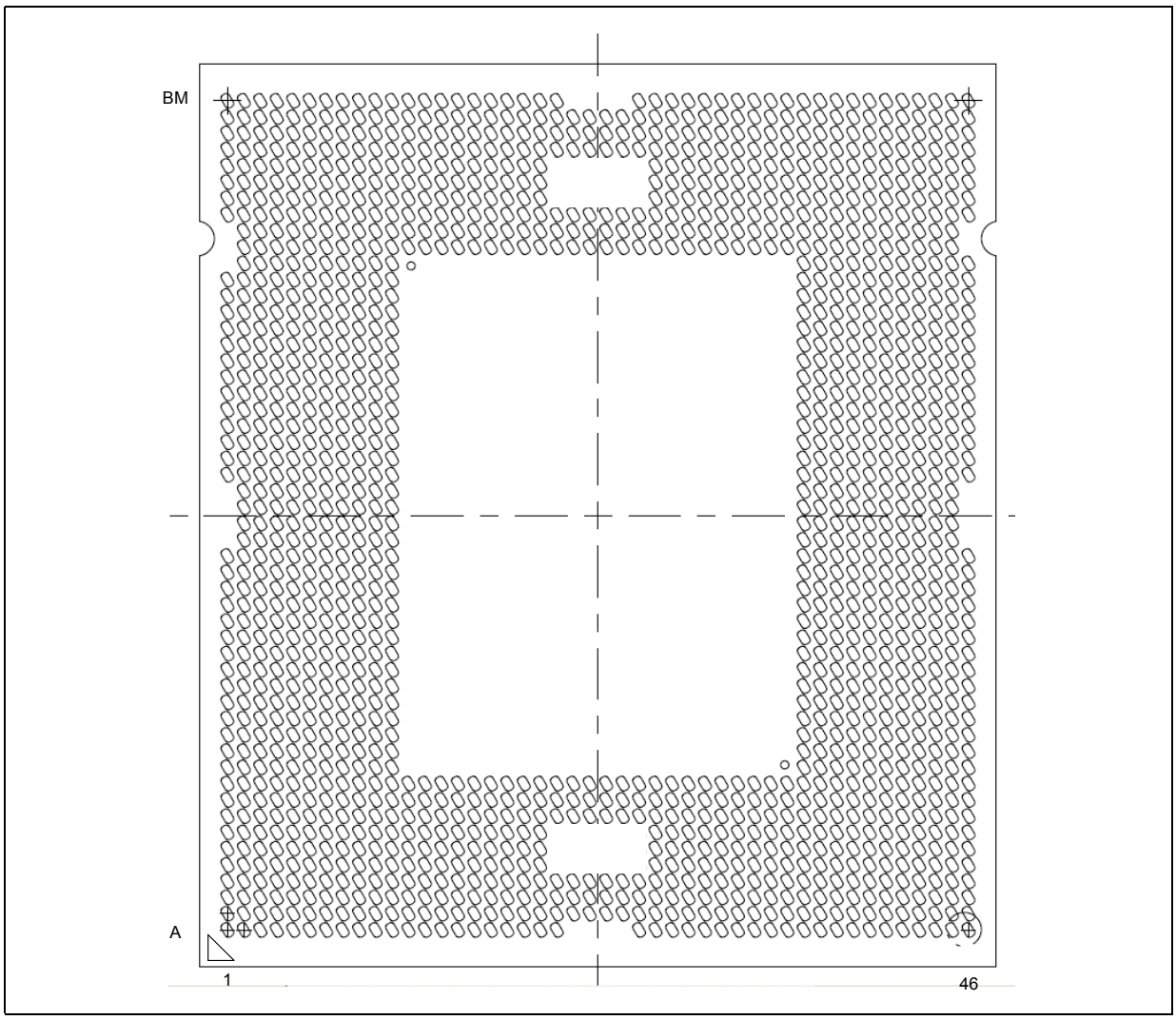
Table 3-4. Mark Content

Mark ID	Value	Notes
Line 1	INTEL [m] [c] 'YY	
Line 2	SUB-BRAND	SSPEC - SUB BRAND
Line 3	SSPEC XXXXX	S-SPEC: Product Specification Number XXXXX: Country of Origin
Line 4	PROC# FREQ/CACHE/INTC	INTC: Processor Interconnect Speed
Line 5	{FPO} {e4}	{Final Process Order Number} {Lead free}
2D Matrix	PROC# S-SPEC FPO SN	

3.1.9 Processor Land Coordinates

Figure 3-5 shows the top view of the processor land coordinates. The coordinates are referred to throughout the document to identify processor lands.

Figure 3-5. Processor Land Coordinates and Quadrants, Top View



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4 Pin Listing

4.1 Processor Package Bottom Land Assignments

This section provides a sorted package bottom pin list in Table 4-1 and Table 4-2. Table 4-1 is a listing of all processor package bottom side lands ordered alphabetically by socket name, and Table 4-2 is a listing ordered by land number.

4.1.1 Processor Pin List, Sorted by Socket Name

Table 4-1. Pin List, Sorted by Socket Name (Sheet 1 of 39)

Socket (EMTS)	Land #	Format	IO
BOOTMODE[0]	BH10	GTL	I
BOOTMODE[1]	BH11	GTL	I
CVID[1]	BL16	CMOS	O
CVID[2]	BK16	CMOS	O
CVID[3]	BJ16	CMOS	O
CVID[4]	BM17	CMOS	O
CVID[5]	BL17	CMOS	O
CVID[6]	BM18	CMOS	O
CVID[7]	BL18	CMOS	O
ERROR0_N	G3	GTL OD	IO
ERROR1_N	G4	GTL OD	IO
FBD0NBIAN[0]	BE8	Differential	I
FBD0NBIAN[1]	BF8	Differential	I
FBD0NBIAN[10]	BC6	Differential	I
FBD0NBIAN[11]	BC8	Differential	I
FBD0NBIAN[12]	BH6	Differential	I
FBD0NBIAN[13]	BK8	Differential	I
FBD0NBIAN[2]	BH8	Differential	I
FBD0NBIAN[3]	BL10	Differential	I
FBD0NBIAN[4]	BM8	Differential	I
FBD0NBIAN[5]	BK9	Differential	I
FBD0NBIAN[6]	BG5	Differential	I
FBD0NBIAN[7]	BF6	Differential	I
FBD0NBIAN[8]	BE6	Differential	I
FBD0NBIAN[9]	BD5	Differential	I
FBD0NBIAP[0]	BD8	Differential	I
FBD0NBIAP[1]	BF9	Differential	I
FBD0NBIAP[10]	BD6	Differential	I
FBD0NBIAP[11]	BC7	Differential	I
FBD0NBIAP[12]	BH7	Differential	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 2 of 39)

Socket (EMTS)	Land #	Format	IO
FBD0NBIAP[13]	BL8	Differential	I
FBD0NBIAP[2]	BG8	Differential	I
FBD0NBIAP[3]	BM10	Differential	I
FBD0NBIAP[4]	BM9	Differential	I
FBD0NBIAP[5]	BK10	Differential	I
FBD0NBIAP[6]	BH5	Differential	I
FBD0NBIAP[7]	BG6	Differential	I
FBD0NBIAP[8]	BE7	Differential	I
FBD0NBIAP[9]	BE5	Differential	I
FBD0NBIBN[0]	BG4	Differential	I
FBD0NBIBN[1]	BK6	Differential	I
FBD0NBIBN[10]	BC4	Differential	I
FBD0NBIBN[11]	BC3	Differential	I
FBD0NBIBN[12]	BH2	Differential	I
FBD0NBIBN[13]	BK2	Differential	I
FBD0NBIBN[2]	BL6	Differential	I
FBD0NBIBN[3]	BM5	Differential	I
FBD0NBIBN[4]	BK5	Differential	I
FBD0NBIBN[5]	BJ4	Differential	I
FBD0NBIBN[6]	BG1	Differential	I
FBD0NBIBN[7]	BF1	Differential	I
FBD0NBIBN[8]	BE3	Differential	I
FBD0NBIBN[9]	BD2	Differential	I
FBD0NBIBP[0]	BF4	Differential	I
FBD0NBIBP[1]	BJ6	Differential	I
FBD0NBIBP[10]	BD4	Differential	I
FBD0NBIBP[11]	BC2	Differential	I
FBD0NBIBP[12]	BJ2	Differential	I
FBD0NBIBP[13]	BK3	Differential	I
FBD0NBIBP[2]	BL7	Differential	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 3 of 39)

Socket (EMTS)	Land #	Format	IO
FBD0NBIBP[3]	BM6	Differential	I
FBD0NBIBP[4]	BL5	Differential	I
FBD0NBIBP[5]	BK4	Differential	I
FBD0NBIBP[6]	BH1	Differential	I
FBD0NBIBP[7]	BF2	Differential	I
FBD0NBIBP[8]	BE4	Differential	I
FBD0NBIBP[9]	BE2	Differential	I
FBD0NBICLKAN0	BJ8	Differential	I
FBD0NBICLKAP0	BJ9	Differential	I
FBD0NBICLKBN0	BH3	Differential	I
FBD0NBICLKBP0	BH4	Differential	I
FBD0SBOAN[0]	BA5	Differential	O
FBD0SBOAN[1]	AY7	Differential	O
FBD0SBOAN[10]	AW8	Differential	O
FBD0SBOAN[2]	AW5	Differential	O
FBD0SBOAN[3]	AV6	Differential	O
FBD0SBOAN[4]	AU7	Differential	O
FBD0SBOAN[5]	AT8	Differential	O
FBD0SBOAN[6]	AP7	Differential	O
FBD0SBOAN[7]	AN6	Differential	O
FBD0SBOAN[8]	AP8	Differential	O
FBD0SBOAN[9]	AR6	Differential	O
FBD0SBOAP[0]	BA6	Differential	O
FBD0SBOAP[1]	AY8	Differential	O
FBD0SBOAP[10]	AV8	Differential	O
FBD0SBOAP[2]	AY5	Differential	O
FBD0SBOAP[3]	AW6	Differential	O
FBD0SBOAP[4]	AV7	Differential	O
FBD0SBOAP[5]	AT7	Differential	O
FBD0SBOAP[6]	AP6	Differential	O
FBD0SBOAP[7]	AN5	Differential	O
FBD0SBOAP[8]	AR8	Differential	O
FBD0SBOAP[9]	AT6	Differential	O
FBD0SBOBN[0]	AW4	Differential	O
FBD0SBOBN[1]	AY3	Differential	O
FBD0SBOBN[10]	AM4	Differential	O
FBD0SBOBN[2]	AW2	Differential	O
FBD0SBOBN[3]	AV1	Differential	O
FBD0SBOBN[4]	AV3	Differential	O
FBD0SBOBN[5]	AR2	Differential	O
FBD0SBOBN[6]	AN2	Differential	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 4 of 39)

Socket (EMTS)	Land #	Format	IO
FBD0SBOBN[7]	AM1	Differential	O
FBD0SBOBN[8]	AP3	Differential	O
FBD0SBOBN[9]	AR4	Differential	O
FBD0SBOBP[0]	AV4	Differential	O
FBD0SBOBP[1]	AY4	Differential	O
FBD0SBOBP[10]	AN4	Differential	O
FBD0SBOBP[2]	AY2	Differential	O
FBD0SBOBP[3]	AW1	Differential	O
FBD0SBOBP[4]	AV2	Differential	O
FBD0SBOBP[5]	AR1	Differential	O
FBD0SBOBP[6]	AP2	Differential	O
FBD0SBOBP[7]	AN1	Differential	O
FBD0SBOBP[8]	AR3	Differential	O
FBD0SBOBP[9]	AT4	Differential	O
FBD0SBOCLKAN0	AU5	Differential	O
FBD0SBOCLKAP0	AT5	Differential	O
FBD0SBOCLKBN0	AU3	Differential	O
FBD0SBOCLKBP0	AU4	Differential	O
FBD1NBICLKCN0	AB5	Differential	I
FBD1NBICLKCP0	AC5	Differential	I
FBD1NBICLKDN0	AB2	Differential	I
FBD1NBICLKDP0	AC2	Differential	I
FBD1NBICN[0]	AC8	Differential	I
FBD1NBICN[1]	AD8	Differential	I
FBD1NBICN[10]	V8	Differential	I
FBD1NBICN[11]	Y8	Differential	I
FBD1NBICN[12]	AA6	Differential	I
FBD1NBICN[13]	AC6	Differential	I
FBD1NBICN[2]	AE8	Differential	I
FBD1NBICN[3]	AF6	Differential	I
FBD1NBICN[4]	AE5	Differential	I
FBD1NBICN[5]	AD6	Differential	I
FBD1NBICN[6]	AA8	Differential	I
FBD1NBICN[7]	W5	Differential	I
FBD1NBICN[8]	Y7	Differential	I
FBD1NBICN[9]	U6	Differential	I
FBD1NBICP[0]	AB8	Differential	I
FBD1NBICP[1]	AD9	Differential	I
FBD1NBICP[10]	V7	Differential	I
FBD1NBICP[11]	W8	Differential	I
FBD1NBICP[12]	AB6	Differential	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 5 of 39)

Socket (EMTS)	Land #	Format	IO
FBD1NBICP[13]	AC7	Differential	I
FBD1NBICP[2]	AF8	Differential	I
FBD1NBICP[3]	AF7	Differential	I
FBD1NBICP[4]	AF5	Differential	I
FBD1NBICP[5]	AE6	Differential	I
FBD1NBICP[6]	AA7	Differential	I
FBD1NBICP[7]	Y5	Differential	I
FBD1NBICP[8]	Y6	Differential	I
FBD1NBICP[9]	V6	Differential	I
FBD1NBIDN[0]	AB4	Differential	I
FBD1NBIDN[1]	AE4	Differential	I
FBD1NBIDN[10]	U4	Differential	I
FBD1NBIDN[11]	W4	Differential	I
FBD1NBIDN[12]	AA1	Differential	I
FBD1NBIDN[13]	AC3	Differential	I
FBD1NBIDN[2]	AG2	Differential	I
FBD1NBIDN[3]	AF3	Differential	I
FBD1NBIDN[4]	AE2	Differential	I
FBD1NBIDN[5]	AD1	Differential	I
FBD1NBIDN[6]	Y3	Differential	I
FBD1NBIDN[7]	W2	Differential	I
FBD1NBIDN[8]	V1	Differential	I
FBD1NBIDN[9]	V3	Differential	I
FBD1NBIDP[0]	AA4	Differential	I
FBD1NBIDP[1]	AD4	Differential	I
FBD1NBIDP[10]	U3	Differential	I
FBD1NBIDP[11]	V4	Differential	I
FBD1NBIDP[12]	AB1	Differential	I
FBD1NBIDP[13]	AD3	Differential	I
FBD1NBIDP[2]	AG3	Differential	I
FBD1NBIDP[3]	AF4	Differential	I
FBD1NBIDP[4]	AF2	Differential	I
FBD1NBIDP[5]	AD2	Differential	I
FBD1NBIDP[6]	Y4	Differential	I
FBD1NBIDP[7]	Y2	Differential	I
FBD1NBIDP[8]	W1	Differential	I
FBD1NBIDP[9]	V2	Differential	I
FBD1SBOCLKCN0	K6	Differential	O
FBD1SBOCLKCP0	J6	Differential	O
FBD1SBOCLKDN0	K1	Differential	O
FBD1SBOCLKDP0	J1	Differential	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 6 of 39)

Socket (EMTS)	Land #	Format	IO
FBD1SBOCN[0]	P5	Differential	O
FBD1SBOCN[1]	N6	Differential	O
FBD1SBOCN[10]	R8	Differential	O
FBD1SBOCN[2]	M6	Differential	O
FBD1SBOCN[3]	L5	Differential	O
FBD1SBOCN[4]	L8	Differential	O
FBD1SBOCN[5]	H7	Differential	O
FBD1SBOCN[6]	J8	Differential	O
FBD1SBOCN[7]	N8	Differential	O
FBD1SBOCN[8]	R7	Differential	O
FBD1SBOCN[9]	H5	Differential	O
FBD1SBOCP[0]	R5	Differential	O
FBD1SBOCP[1]	P6	Differential	O
FBD1SBOCP[10]	P8	Differential	O
FBD1SBOCP[2]	M7	Differential	O
FBD1SBOCP[3]	M5	Differential	O
FBD1SBOCP[4]	L7	Differential	O
FBD1SBOCP[5]	H6	Differential	O
FBD1SBOCP[6]	K8	Differential	O
FBD1SBOCP[7]	N7	Differential	O
FBD1SBOCP[8]	R6	Differential	O
FBD1SBOCP[9]	J5	Differential	O
FBD1SBODN[0]	P2	Differential	O
FBD1SBODN[1]	N1	Differential	O
FBD1SBODN[10]	R4	Differential	O
FBD1SBODN[2]	N3	Differential	O
FBD1SBODN[3]	L1	Differential	O
FBD1SBODN[4]	K2	Differential	O
FBD1SBODN[5]	H2	Differential	O
FBD1SBODN[6]	J4	Differential	O
FBD1SBODN[7]	M4	Differential	O
FBD1SBODN[8]	P4	Differential	O
FBD1SBODN[9]	H3	Differential	O
FBD1SBODP[0]	R2	Differential	O
FBD1SBODP[1]	P1	Differential	O
FBD1SBODP[10]	R3	Differential	O
FBD1SBODP[2]	N2	Differential	O
FBD1SBODP[3]	L2	Differential	O
FBD1SBODP[4]	K3	Differential	O
FBD1SBODP[5]	H1	Differential	O
FBD1SBODP[6]	K4	Differential	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 7 of 39)

Socket (EMTS)	Land #	Format	IO
FBD1SBODP[7]	M3	Differential	O
FBD1SBODP[8]	N4	Differential	O
FBD1SBODP[9]	J3	Differential	O
FLASHROM_CFG[0]	BL15	GTL	I
FLASHROM_CFG[1]	BM15	GTL	I
FLASHROM_CFG[2]	BJ15	GTL	I
FLASHROM_CLK	BL11	GTL	OD
FLASHROM_CS_N[0]	BK13	GTL	OD
FLASHROM_CS_N[1]	BM13	GTL	OD
FLASHROM_CS_N[2]	BL14	GTL	OD
FLASHROM_CS_N[3]	BM14	GTL	OD
FLASHROM_DATI	BL12	GTL	I
FLASHROM_DATO	BM12	GTL	OD
FLASHROM_WP_N	BK11	GTL	OD
FORCE_PR_N	C4	GTL	I
ISENSE_DN	B5	GTL	I
ISENSE_DP	A5	GTL	I
LT-SX (Test-Lo)	BF10	GTL	I
MBP[0]_N	G2	GTL	IO
MBP[1]_N	F2	GTL	IO
MBP[2]_N	F1	GTL	IO
MBP[3]_N	E2	GTL	IO
MBP[4]_N	F4	GTL	IO
MBP[5]_N	E3	GTL	IO
MBP[6]_N	E1	GTL	IO
MBP[7]_N	E4	GTL	IO
MEM_THROTTLE0_N	BC10	GTL	I
MEM_THROTTLE1_N	BD10	GTL	I
NMI	D5	GTL	I
PECI	D43	CMOS	IO
PRDY_N	C3	CMOS	O
PREQ_N	D3	CMOS	I
Proc_ID[0]	AW9	CMOS	O
Proc_ID[1]	AY9	CMOS	O
PROCHOT_N	D2	GTL	OD
PSI_CACHE_N	BF14	CMOS	O
PSI_N	G7	CMOS	O
PWRGOOD	G41	CMOS	I
QPI0_CLKRX_DN	BF37	SCID Diff.	I
QPI0_CLKRX_DP	BF36	SCID Diff.	I
QPI0_CLKTX_DN	BL41	SCID Diff.	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 8 of 39)

Socket (EMTS)	Land #	Format	IO
QPI0_CLKTX_DP	BM41	SCID Diff.	O
QPI0_DRX_DN[0]	BB38	SCID Diff.	I
QPI0_DRX_DN[1]	AY41	SCID Diff.	I
QPI0_DRX_DN[10]	BE35	SCID Diff.	I
QPI0_DRX_DN[11]	BG35	SCID Diff.	I
QPI0_DRX_DN[12]	BJ33	SCID Diff.	I
QPI0_DRX_DN[13]	BM33	SCID Diff.	I
QPI0_DRX_DN[14]	BL32	SCID Diff.	I
QPI0_DRX_DN[15]	BH33	SCID Diff.	I
QPI0_DRX_DN[16]	BG33	SCID Diff.	I
QPI0_DRX_DN[17]	BF32	SCID Diff.	I
QPI0_DRX_DN[18]	BE33	SCID Diff.	I
QPI0_DRX_DN[19]	BD34	SCID Diff.	I
QPI0_DRX_DN[2]	BA40	SCID Diff.	I
QPI0_DRX_DN[3]	BC39	SCID Diff.	I
QPI0_DRX_DN[4]	BC41	SCID Diff.	I
QPI0_DRX_DN[5]	BD40	SCID Diff.	I
QPI0_DRX_DN[6]	BC36	SCID Diff.	I
QPI0_DRX_DN[7]	BF40	SCID Diff.	I
QPI0_DRX_DN[8]	BE39	SCID Diff.	I
QPI0_DRX_DN[9]	BD37	SCID Diff.	I
QPI0_DRX_DP[0]	BB39	SCID Diff.	I
QPI0_DRX_DP[1]	BA41	SCID Diff.	I
QPI0_DRX_DP[10]	BF35	SCID Diff.	I
QPI0_DRX_DP[11]	BG34	SCID Diff.	I
QPI0_DRX_DP[12]	BK33	SCID Diff.	I
QPI0_DRX_DP[13]	BM32	SCID Diff.	I
QPI0_DRX_DP[14]	BK32	SCID Diff.	I
QPI0_DRX_DP[15]	BH32	SCID Diff.	I
QPI0_DRX_DP[16]	BF33	SCID Diff.	I
QPI0_DRX_DP[17]	BE32	SCID Diff.	I
QPI0_DRX_DP[18]	BE34	SCID Diff.	I
QPI0_DRX_DP[19]	BD35	SCID Diff.	I
QPI0_DRX_DP[2]	BB40	SCID Diff.	I
QPI0_DRX_DP[3]	BC40	SCID Diff.	I
QPI0_DRX_DP[4]	BD41	SCID Diff.	I
QPI0_DRX_DP[5]	BE40	SCID Diff.	I
QPI0_DRX_DP[6]	BD36	SCID Diff.	I
QPI0_DRX_DP[7]	BF39	SCID Diff.	I
QPI0_DRX_DP[8]	BE38	SCID Diff.	I
QPI0_DRX_DP[9]	BE37	SCID Diff.	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 9 of 39)

Socket (EMTS)	Land #	Format	IO
QPI0_DTX_DN[0]	BG42	SCID Diff.	O
QPI0_DTX_DN[1]	BF43	SCID Diff.	O
QPI0_DTX_DN[10]	BJ41	SCID Diff.	O
QPI0_DTX_DN[11]	BL40	SCID Diff.	O
QPI0_DTX_DN[12]	BK39	SCID Diff.	O
QPI0_DTX_DN[13]	BL37	SCID Diff.	O
QPI0_DTX_DN[14]	BK37	SCID Diff.	O
QPI0_DTX_DN[15]	BM36	SCID Diff.	O
QPI0_DTX_DN[16]	BL35	SCID Diff.	O
QPI0_DTX_DN[17]	BJ36	SCID Diff.	O
QPI0_DTX_DN[18]	BJ37	SCID Diff.	O
QPI0_DTX_DN[19]	BH39	SCID Diff.	O
QPI0_DTX_DN[2]	BF44	SCID Diff.	O
QPI0_DTX_DN[3]	BF46	SCID Diff.	O
QPI0_DTX_DN[4]	BH43	SCID Diff.	O
QPI0_DTX_DN[5]	BH45	SCID Diff.	O
QPI0_DTX_DN[6]	BJ43	SCID Diff.	O
QPI0_DTX_DN[7]	BK45	SCID Diff.	O
QPI0_DTX_DN[8]	BK42	SCID Diff.	O
QPI0_DTX_DN[9]	BL43	SCID Diff.	O
QPI0_DTX_DP[0]	BH42	SCID Diff.	O
QPI0_DTX_DP[1]	BG43	SCID Diff.	O
QPI0_DTX_DP[10]	BJ40	SCID Diff.	O
QPI0_DTX_DP[11]	BL39	SCID Diff.	O
QPI0_DTX_DP[12]	BJ39	SCID Diff.	O
QPI0_DTX_DP[13]	BM37	SCID Diff.	O
QPI0_DTX_DP[14]	BK36	SCID Diff.	O
QPI0_DTX_DP[15]	BM35	SCID Diff.	O
QPI0_DTX_DP[16]	BK35	SCID Diff.	O
QPI0_DTX_DP[17]	BJ35	SCID Diff.	O
QPI0_DTX_DP[18]	BH37	SCID Diff.	O
QPI0_DTX_DP[19]	BH40	SCID Diff.	O
QPI0_DTX_DP[2]	BF45	SCID Diff.	O
QPI0_DTX_DP[3]	BG46	SCID Diff.	O
QPI0_DTX_DP[4]	BH44	SCID Diff.	O
QPI0_DTX_DP[5]	BJ45	SCID Diff.	O
QPI0_DTX_DP[6]	BK43	SCID Diff.	O
QPI0_DTX_DP[7]	BK44	SCID Diff.	O
QPI0_DTX_DP[8]	BK41	SCID Diff.	O
QPI0_DTX_DP[9]	BL42	SCID Diff.	O
QPI1_CLKRX_DN	AP41	SCID Diff.	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 10 of 39)

Socket (EMTS)	Land #	Format	IO
QPI1_CLKRX_DP	AR41	SCID Diff.	I
QPI1_CLKTX_DN	AY45	SCID Diff.	O
QPI1_CLKTX_DP	AY46	SCID Diff.	O
QPI1_DRX_DN[0]	AN38	SCID Diff.	I
QPI1_DRX_DN[1]	AM37	SCID Diff.	I
QPI1_DRX_DN[10]	AR40	SCID Diff.	I
QPI1_DRX_DN[11]	AU39	SCID Diff.	I
QPI1_DRX_DN[12]	AU41	SCID Diff.	I
QPI1_DRX_DN[13]	AV40	SCID Diff.	I
QPI1_DRX_DN[14]	AW39	SCID Diff.	I
QPI1_DRX_DN[15]	AY40	SCID Diff.	I
QPI1_DRX_DN[16]	AV38	SCID Diff.	I
QPI1_DRX_DN[17]	BA38	SCID Diff.	I
QPI1_DRX_DN[18]	AT39	SCID Diff.	I
QPI1_DRX_DN[19]	AR38	SCID Diff.	I
QPI1_DRX_DN[2]	AJ37	SCID Diff.	I
QPI1_DRX_DN[3]	AK38	SCID Diff.	I
QPI1_DRX_DN[4]	AH41	SCID Diff.	I
QPI1_DRX_DN[5]	AJ40	SCID Diff.	I
QPI1_DRX_DN[6]	AL39	SCID Diff.	I
QPI1_DRX_DN[7]	AL41	SCID Diff.	I
QPI1_DRX_DN[8]	AM40	SCID Diff.	I
QPI1_DRX_DN[9]	AP39	SCID Diff.	I
QPI1_DRX_DP[0]	AN39	SCID Diff.	I
QPI1_DRX_DP[1]	AM38	SCID Diff.	I
QPI1_DRX_DP[10]	AT40	SCID Diff.	I
QPI1_DRX_DP[11]	AU40	SCID Diff.	I
QPI1_DRX_DP[12]	AV41	SCID Diff.	I
QPI1_DRX_DP[13]	AW40	SCID Diff.	I
QPI1_DRX_DP[14]	AW38	SCID Diff.	I
QPI1_DRX_DP[15]	AY39	SCID Diff.	I
QPI1_DRX_DP[16]	AV37	SCID Diff.	I
QPI1_DRX_DP[17]	BA37	SCID Diff.	I
QPI1_DRX_DP[18]	AT38	SCID Diff.	I
QPI1_DRX_DP[19]	AR37	SCID Diff.	I
QPI1_DRX_DP[2]	AJ38	SCID Diff.	I
QPI1_DRX_DP[3]	AK39	SCID Diff.	I
QPI1_DRX_DP[4]	AJ41	SCID Diff.	I
QPI1_DRX_DP[5]	AK40	SCID Diff.	I
QPI1_DRX_DP[6]	AL40	SCID Diff.	I
QPI1_DRX_DP[7]	AM41	SCID Diff.	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 11 of 39)

Socket (EMTS)	Land #	Format	IO
QPI1_DRX_DP[8]	AN40	SCID Diff.	I
QPI1_DRX_DP[9]	AP40	SCID Diff.	I
QPI1_DTX_DN[0]	AT43	SCID Diff.	O
QPI1_DTX_DN[1]	AR43	SCID Diff.	O
QPI1_DTX_DN[10]	BA44	SCID Diff.	O
QPI1_DTX_DN[11]	BA46	SCID Diff.	O
QPI1_DTX_DN[12]	BB44	SCID Diff.	O
QPI1_DTX_DN[13]	BC45	SCID Diff.	O
QPI1_DTX_DN[14]	BD45	SCID Diff.	O
QPI1_DTX_DN[15]	BC43	SCID Diff.	O
QPI1_DTX_DN[16]	BE44	SCID Diff.	O
QPI1_DTX_DN[17]	BA43	SCID Diff.	O
QPI1_DTX_DN[18]	AW44	SCID Diff.	O
QPI1_DTX_DN[19]	AV43	SCID Diff.	O
QPI1_DTX_DN[2]	AN43	SCID Diff.	O
QPI1_DTX_DN[3]	AM45	SCID Diff.	O
QPI1_DTX_DN[4]	AP45	SCID Diff.	O
QPI1_DTX_DN[5]	AR44	SCID Diff.	O
QPI1_DTX_DN[6]	AR46	SCID Diff.	O
QPI1_DTX_DN[7]	AU45	SCID Diff.	O
QPI1_DTX_DN[8]	AV44	SCID Diff.	O
QPI1_DTX_DN[9]	AV46	SCID Diff.	O
QPI1_DTX_DP[0]	AT44	SCID Diff.	O
QPI1_DTX_DP[1]	AP43	SCID Diff.	O
QPI1_DTX_DP[10]	BA45	SCID Diff.	O
QPI1_DTX_DP[11]	BB46	SCID Diff.	O
QPI1_DTX_DP[12]	BB43	SCID Diff.	O
QPI1_DTX_DP[13]	BC44	SCID Diff.	O
QPI1_DTX_DP[14]	BE45	SCID Diff.	O
QPI1_DTX_DP[15]	BD43	SCID Diff.	O
QPI1_DTX_DP[16]	BE43	SCID Diff.	O
QPI1_DTX_DP[17]	AY43	SCID Diff.	O
QPI1_DTX_DP[18]	AW43	SCID Diff.	O
QPI1_DTX_DP[19]	AU43	SCID Diff.	O
QPI1_DTX_DP[2]	AN44	SCID Diff.	O
QPI1_DTX_DP[3]	AM44	SCID Diff.	O
QPI1_DTX_DP[4]	AP46	SCID Diff.	O
QPI1_DTX_DP[5]	AR45	SCID Diff.	O
QPI1_DTX_DP[6]	AT46	SCID Diff.	O
QPI1_DTX_DP[7]	AU46	SCID Diff.	O
QPI1_DTX_DP[8]	AV45	SCID Diff.	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 12 of 39)

Socket (EMTS)	Land #	Format	IO
QPI1_DTX_DP[9]	AW46	SCID Diff.	O
QPI2_CLKRX_DN	AB40	SCID Diff.	I
QPI2_CLKRX_DP	AB39	SCID Diff.	I
QPI2_CLKTX_DN	AE44	SCID Diff.	O
QPI2_CLKTX_DP	AE45	SCID Diff.	O
QPI2_DRX_DN[0]	AC37	SCID Diff.	I
QPI2_DRX_DN[1]	AD38	SCID Diff.	I
QPI2_DRX_DN[10]	AA40	SCID Diff.	I
QPI2_DRX_DN[11]	Y41	SCID Diff.	I
QPI2_DRX_DN[12]	W40	SCID Diff.	I
QPI2_DRX_DN[13]	V40	SCID Diff.	I
QPI2_DRX_DN[14]	U41	SCID Diff.	I
QPI2_DRX_DN[15]	T40	SCID Diff.	I
QPI2_DRX_DN[16]	V39	SCID Diff.	I
QPI2_DRX_DN[17]	V37	SCID Diff.	I
QPI2_DRX_DN[18]	Y38	SCID Diff.	I
QPI2_DRX_DN[19]	AA37	SCID Diff.	I
QPI2_DRX_DN[2]	AF37	SCID Diff.	I
QPI2_DRX_DN[3]	AG38	SCID Diff.	I
QPI2_DRX_DN[4]	AH40	SCID Diff.	I
QPI2_DRX_DN[5]	AG40	SCID Diff.	I
QPI2_DRX_DN[6]	AF41	SCID Diff.	I
QPI2_DRX_DN[7]	AE40	SCID Diff.	I
QPI2_DRX_DN[8]	AD40	SCID Diff.	I
QPI2_DRX_DN[9]	AC41	SCID Diff.	I
QPI2_DRX_DP[0]	AC38	SCID Diff.	I
QPI2_DRX_DP[1]	AD39	SCID Diff.	I
QPI2_DRX_DP[10]	Y40	SCID Diff.	I
QPI2_DRX_DP[11]	W41	SCID Diff.	I
QPI2_DRX_DP[12]	W39	SCID Diff.	I
QPI2_DRX_DP[13]	U40	SCID Diff.	I
QPI2_DRX_DP[14]	T41	SCID Diff.	I
QPI2_DRX_DP[15]	T39	SCID Diff.	I
QPI2_DRX_DP[16]	V38	SCID Diff.	I
QPI2_DRX_DP[17]	U37	SCID Diff.	I
QPI2_DRX_DP[18]	Y37	SCID Diff.	I
QPI2_DRX_DP[19]	AB37	SCID Diff.	I
QPI2_DRX_DP[2]	AF38	SCID Diff.	I
QPI2_DRX_DP[3]	AG39	SCID Diff.	I
QPI2_DRX_DP[4]	AH39	SCID Diff.	I
QPI2_DRX_DP[5]	AF40	SCID Diff.	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 13 of 39)

Socket (EMTS)	Land #	Format	IO
QPI2_DRX_DP[6]	AE41	SCID Diff.	I
QPI2_DRX_DP[7]	AE39	SCID Diff.	I
QPI2_DRX_DP[8]	AC40	SCID Diff.	I
QPI2_DRX_DP[9]	AB41	SCID Diff.	I
QPI2_DTX_DN[0]	AE43	SCID Diff.	O
QPI2_DTX_DN[1]	AH43	SCID Diff.	O
QPI2_DTX_DN[10]	AD43	SCID Diff.	O
QPI2_DTX_DN[11]	AD46	SCID Diff.	O
QPI2_DTX_DN[12]	AC45	SCID Diff.	O
QPI2_DTX_DN[13]	AB46	SCID Diff.	O
QPI2_DTX_DN[14]	AA45	SCID Diff.	O
QPI2_DTX_DN[15]	Y46	SCID Diff.	O
QPI2_DTX_DN[16]	W45	SCID Diff.	O
QPI2_DTX_DN[17]	AA44	SCID Diff.	O
QPI2_DTX_DN[18]	W43	SCID Diff.	O
QPI2_DTX_DN[19]	AB43	SCID Diff.	O
QPI2_DTX_DN[2]	AM43	SCID Diff.	O
QPI2_DTX_DN[3]	AN46	SCID Diff.	O
QPI2_DTX_DN[4]	AL45	SCID Diff.	O
QPI2_DTX_DN[5]	AK43	SCID Diff.	O
QPI2_DTX_DN[6]	AK45	SCID Diff.	O
QPI2_DTX_DN[7]	AH44	SCID Diff.	O
QPI2_DTX_DN[8]	AG43	SCID Diff.	O
QPI2_DTX_DN[9]	AG45	SCID Diff.	O
QPI2_DTX_DP[0]	AF43	SCID Diff.	O
QPI2_DTX_DP[1]	AJ43	SCID Diff.	O
QPI2_DTX_DP[10]	AD44	SCID Diff.	O
QPI2_DTX_DP[11]	AC46	SCID Diff.	O
QPI2_DTX_DP[12]	AC44	SCID Diff.	O
QPI2_DTX_DP[13]	AB45	SCID Diff.	O
QPI2_DTX_DP[14]	Y45	SCID Diff.	O
QPI2_DTX_DP[15]	W46	SCID Diff.	O
QPI2_DTX_DP[16]	W44	SCID Diff.	O
QPI2_DTX_DP[17]	AA43	SCID Diff.	O
QPI2_DTX_DP[18]	Y43	SCID Diff.	O
QPI2_DTX_DP[19]	AC43	SCID Diff.	O
QPI2_DTX_DP[2]	AL43	SCID Diff.	O
QPI2_DTX_DP[3]	AM46	SCID Diff.	O
QPI2_DTX_DP[4]	AL46	SCID Diff.	O
QPI2_DTX_DP[5]	AK44	SCID Diff.	O
QPI2_DTX_DP[6]	AJ45	SCID Diff.	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 14 of 39)

Socket (EMTS)	Land #	Format	IO
QPI2_DTX_DP[7]	AH45	SCID Diff.	O
QPI2_DTX_DP[8]	AG44	SCID Diff.	O
QPI2_DTX_DP[9]	AF45	SCID Diff.	O
QPI3_CLKRX_DN	N45	SCID Diff.	I
QPI3_CLKRX_DP	M45	SCID Diff.	I
QPI3_CLKTX_DN	E44	SCID Diff.	O
QPI3_CLKTX_DP	D44	SCID Diff.	O
QPI3_DRX_DN[0]	P41	SCID Diff.	I
QPI3_DRX_DN[1]	N41	SCID Diff.	I
QPI3_DRX_DN[10]	N43	SCID Diff.	I
QPI3_DRX_DN[11]	L44	SCID Diff.	I
QPI3_DRX_DN[12]	L43	SCID Diff.	I
QPI3_DRX_DN[13]	M41	SCID Diff.	I
QPI3_DRX_DN[14]	N40	SCID Diff.	I
QPI3_DRX_DN[15]	L40	SCID Diff.	I
QPI3_DRX_DN[16]	M38	SCID Diff.	I
QPI3_DRX_DN[17]	N38	SCID Diff.	I
QPI3_DRX_DN[18]	P40	SCID Diff.	I
QPI3_DRX_DN[19]	R39	SCID Diff.	I
QPI3_DRX_DN[2]	T42	SCID Diff.	I
QPI3_DRX_DN[3]	U43	SCID Diff.	I
QPI3_DRX_DN[4]	U44	SCID Diff.	I
QPI3_DRX_DN[5]	R43	SCID Diff.	I
QPI3_DRX_DN[6]	U46	SCID Diff.	I
QPI3_DRX_DN[7]	T45	SCID Diff.	I
QPI3_DRX_DN[8]	P44	SCID Diff.	I
QPI3_DRX_DN[9]	P46	SCID Diff.	I
QPI3_DRX_DP[0]	R41	SCID Diff.	I
QPI3_DRX_DP[1]	N42	SCID Diff.	I
QPI3_DRX_DP[10]	M43	SCID Diff.	I
QPI3_DRX_DP[11]	M44	SCID Diff.	I
QPI3_DRX_DP[12]	L42	SCID Diff.	I
QPI3_DRX_DP[13]	L41	SCID Diff.	I
QPI3_DRX_DP[14]	M40	SCID Diff.	I
QPI3_DRX_DP[15]	L39	SCID Diff.	I
QPI3_DRX_DP[16]	L38	SCID Diff.	I
QPI3_DRX_DP[17]	N37	SCID Diff.	I
QPI3_DRX_DP[18]	P39	SCID Diff.	I
QPI3_DRX_DP[19]	R38	SCID Diff.	I
QPI3_DRX_DP[2]	R42	SCID Diff.	I
QPI3_DRX_DP[3]	T43	SCID Diff.	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 15 of 39)

Socket (EMTS)	Land #	Format	IO
QPI3_DRX_DP[4]	U45	SCID Diff.	I
QPI3_DRX_DP[5]	R44	SCID Diff.	I
QPI3_DRX_DP[6]	T46	SCID Diff.	I
QPI3_DRX_DP[7]	R45	SCID Diff.	I
QPI3_DRX_DP[8]	P45	SCID Diff.	I
QPI3_DRX_DP[9]	N46	SCID Diff.	I
QPI3_DTX_DN[0]	J40	SCID Diff.	O
QPI3_DTX_DN[1]	H42	SCID Diff.	O
QPI3_DTX_DN[10]	C45	SCID Diff.	O
QPI3_DTX_DN[11]	B44	SCID Diff.	O
QPI3_DTX_DN[12]	F42	SCID Diff.	O
QPI3_DTX_DN[13]	B42	SCID Diff.	O
QPI3_DTX_DN[14]	A41	SCID Diff.	O
QPI3_DTX_DN[15]	D42	SCID Diff.	O
QPI3_DTX_DN[16]	C39	SCID Diff.	O
QPI3_DTX_DN[17]	F41	SCID Diff.	O
QPI3_DTX_DN[18]	E39	SCID Diff.	O
QPI3_DTX_DN[19]	E40	SCID Diff.	O
QPI3_DTX_DN[2]	G43	SCID Diff.	O
QPI3_DTX_DN[3]	J43	SCID Diff.	O
QPI3_DTX_DN[4]	F43	SCID Diff.	O
QPI3_DTX_DN[5]	K46	SCID Diff.	O
QPI3_DTX_DN[6]	J45	SCID Diff.	O
QPI3_DTX_DN[7]	G44	SCID Diff.	O
QPI3_DTX_DN[8]	G46	SCID Diff.	O
QPI3_DTX_DN[9]	E45	SCID Diff.	O
QPI3_DTX_DP[0]	J41	SCID Diff.	O
QPI3_DTX_DP[1]	J42	SCID Diff.	O
QPI3_DTX_DP[10]	C44	SCID Diff.	O
QPI3_DTX_DP[11]	B43	SCID Diff.	O
QPI3_DTX_DP[12]	E42	SCID Diff.	O
QPI3_DTX_DP[13]	C42	SCID Diff.	O
QPI3_DTX_DP[14]	B41	SCID Diff.	O
QPI3_DTX_DP[15]	D41	SCID Diff.	O
QPI3_DTX_DP[16]	C40	SCID Diff.	O
QPI3_DTX_DP[17]	F40	SCID Diff.	O
QPI3_DTX_DP[18]	F39	SCID Diff.	O
QPI3_DTX_DP[19]	D40	SCID Diff.	O
QPI3_DTX_DP[2]	H43	SCID Diff.	O
QPI3_DTX_DP[3]	J44	SCID Diff.	O
QPI3_DTX_DP[4]	F44	SCID Diff.	O

Table 4-1. Pin List, Sorted by Socket Name (Sheet 16 of 39)

Socket (EMTS)	Land #	Format	IO
QPI3_DTX_DP[5]	J46	SCID Diff.	O
QPI3_DTX_DP[6]	H45	SCID Diff.	O
QPI3_DTX_DP[7]	G45	SCID Diff.	O
QPI3_DTX_DP[8]	F46	SCID Diff.	O
QPI3_DTX_DP[9]	E46	SCID Diff.	O
RESET_N	B4	GTL	I
RSVD	AA10		IO
RSVD	AA2		IO
RSVD	AB3		IO
RSVD	AD37		IO
RSVD	AE38		IO
RSVD	AF10		IO
RSVD	AG10		IO
RSVD	AG37		IO
RSVD	AG5		IO
RSVD	AG6		IO
RSVD	AG7		IO
RSVD	AG9		IO
RSVD	AH10		IO
RSVD	AH3		IO
RSVD	AH38		IO
RSVD	AH4		IO
RSVD	AH5		IO
RSVD	AH7		IO
RSVD	AH8		IO
RSVD	AH9		IO
RSVD	AJ4		IO
RSVD	AJ46		IO
RSVD	AJ5		IO
RSVD	AJ6		IO
RSVD	AJ7		IO
RSVD	AJ8		IO
RSVD	AJ9		IO
RSVD	AK37		IO
RSVD	AK6		IO
RSVD	AK8		IO
RSVD	AK9		IO
RSVD	AL38		IO
RSVD	AL6		IO
RSVD	AL8		IO
RSVD	AM10		IO

Table 4-1. Pin List, Sorted by Socket Name (Sheet 17 of 39)

Socket (EMTS)	Land #	Format	IO
RSVD	AM6		IO
RSVD	AM7		IO
RSVD	AM8		IO
RSVD	AM9		IO
RSVD	AN37		IO
RSVD	AP38		IO
RSVD	AT2		IO
RSVD	AT37		IO
RSVD	AU2		IO
RSVD	AU38		IO
RSVD	AW37		IO
RSVD	AY38		IO
RSVD	B46		IO
RSVD	BC35		IO
RSVD	BC38		IO
RSVD	BC9		IO
RSVD	BD12		IO
RSVD	BD13		IO
RSVD	BD38		IO
RSVD	BD9		IO
RSVD	BF12		IO
RSVD	BF3		O
RSVD	BG2		O
RSVD	BG32		O
RSVD	BG45		O
RSVD	BH15		O
RSVD	BH16		O
RSVD	C46		O
RSVD	D4		O
RSVD	G6		O
RSVD	H9		O
RSVD	J9		O
RSVD	M39		O
RSVD	P37		O
RSVD	P38		O
RSVD	P9		O
RSVD	R9		O
RSVD	W38		O
RSVD	W9		IO
RSVD	Y10		IO
RSVD	Y9		IO

Table 4-1. Pin List, Sorted by Socket Name (Sheet 18 of 39)

Socket (EMTS)	Land #	Format	IO
RUNBIST	BJ10	GTL	I
SKTDIS_N	BG11	GTL	I
SKTID[0]	BK14	CMOS	I
SKTID[1]	BJ14	CMOS	I
SKTID[2]	BH14	CMOS	I
SKTOCC_N	BJ13		O
SM_WP	BK12	CMOS	I
SMBCLK	BJ12	CMOS	I/OD
SMBDAT	BH12	CMOS	I/OD
SPDCLK	BG10	CMOS	I/OD
SPDDAT	BG9	CMOS	I/OD
SYSCLK_DN	T38	Differential	I
SYSCLK_DP	U38	Differential	I
SYSCLK_LAI	AA39	Differential	I
SYSCLK_LAI_N	AA38	Differential	I
TCLK	K10	GTL	I
TDI	L9	GTL	I
TDO	L10	GTL-OD	O
TEST[0]	A1		I
TEST[1]	A46		IO
TEST[2]	BM46		I
TEST[3]	BM1		IO
Test-Hi	AP10	GTL	I
THERMALERT_N	BG13	CMOS	OD
THERMTRIP_N	F5	GTL-OD	O
TMS	M9	GTL	I
TRST_N	M10	GTL	I
VCACHE	BC15	Power	I
VCACHE	BC17	Power	I
VCACHE	BC18	Power	I
VCACHE	BC20	Power	I
VCACHE	BC21	Power	I
VCACHE	BC23	Power	I
VCACHE	BC24	Power	I
VCACHE	BC26	Power	I
VCACHE	BC27	Power	I
VCACHE	BC29	Power	I
VCACHE	BC30	Power	I
VCACHE	BC32	Power	I
VCACHE	BC33	Power	I
VCACHE	BD15	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 19 of 39)

Socket (EMTS)	Land #	Format	IO
VCACHE	BD17	Power	I
VCACHE	BD18	Power	I
VCACHE	BD20	Power	I
VCACHE	BD21	Power	I
VCACHE	BD23	Power	I
VCACHE	BD24	Power	I
VCACHE	BD26	Power	I
VCACHE	BD27	Power	I
VCACHE	BD29	Power	I
VCACHE	BD30	Power	I
VCACHE	BD32	Power	I
VCACHE	BD33	Power	I
VCACHE	BE15	Power	I
VCACHE	BE17	Power	I
VCACHE	BE18	Power	I
VCACHE	BE20	Power	I
VCACHE	BE21	Power	I
VCACHE	BE23	Power	I
VCACHE	BE24	Power	I
VCACHE	BE26	Power	I
VCACHE	BE27	Power	I
VCACHE	BE29	Power	I
VCACHE	BE30	Power	I
VCACHE	BF15	Power	I
VCACHE	BF17	Power	I
VCACHE	BF18	Power	I
VCACHE	BF20	Power	I
VCACHE	BF27	Power	I
VCACHE	BF29	Power	I
VCACHE	BF30	Power	I
VCACHE	BG15	Power	I
VCACHE	BG17	Power	I
VCACHE	BG18	Power	I
VCACHE	BG20	Power	I
VCACHE	BG27	Power	I
VCACHE	BG29	Power	I
VCACHE	BG30	Power	I
VCACHE	BH17	Power	I
VCACHE	BH18	Power	I
VCACHE	BH20	Power	I
VCACHE	BH27	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 20 of 39)

Socket (EMTS)	Land #	Format	IO
VCACHE	BH29	Power	I
VCACHE	BH30	Power	I
VCACHE	BJ18	Power	I
VCACHE	BJ20	Power	I
VCACHE	BJ21	Power	I
VCACHE	BJ23	Power	I
VCACHE	BJ24	Power	I
VCACHE	BJ26	Power	I
VCACHE	BJ27	Power	I
VCACHE	BJ29	Power	I
VCACHE	BJ30	Power	I
VCACHE	BK20	Power	I
VCACHE	BK21	Power	I
VCACHE	BK23	Power	I
VCACHE	BK24	Power	I
VCACHE	BK26	Power	I
VCACHE	BK27	Power	I
VCACHE	BK29	Power	I
VCACHE	BK30	Power	I
VCACHE	BL20	Power	I
VCACHE	BL21	Power	I
VCACHE	BL23	Power	I
VCACHE	BL24	Power	I
VCACHE	BL26	Power	I
VCACHE	BL27	Power	I
VCACHE	BL29	Power	I
VCACHE	BL30	Power	I
VCACHE	BM20	Power	I
VCACHE	BM21	Power	I
VCACHE	BM26	Power	I
VCACHE	BM27	Power	I
VCACHE	BM29	Power	I
VCACHE	BM30	Power	I
VCACHESENSE	BK18	Power	IO
VCC33	BE10	Power	I
VCC33	BE11	Power	I
VCC33	BE12	Power	I
VCCCORE	K38	Power	I
VCCCORE	K37	Power	I
VCCCORE	K35	Power	I
VCCCORE	K34	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 21 of 39)

Socket (EMTS)	Land #	Format	IO
VCCCORE	K32	Power	I
VCCCORE	K31	Power	I
VCCCORE	K29	Power	I
VCCCORE	K28	Power	I
VCCCORE	K26	Power	I
VCCCORE	K25	Power	I
VCCCORE	K22	Power	I
VCCCORE	K21	Power	I
VCCCORE	K19	Power	I
VCCCORE	K18	Power	I
VCCCORE	K16	Power	I
VCCCORE	K15	Power	I
VCCCORE	K13	Power	I
VCCCORE	K12	Power	I
VCCCORE	J38	Power	I
VCCCORE	J37	Power	I
VCCCORE	J35	Power	I
VCCCORE	J34	Power	I
VCCCORE	J32	Power	I
VCCCORE	J31	Power	I
VCCCORE	J29	Power	I
VCCCORE	J28	Power	I
VCCCORE	J26	Power	I
VCCCORE	J25	Power	I
VCCCORE	J22	Power	I
VCCCORE	J21	Power	I
VCCCORE	J19	Power	I
VCCCORE	J18	Power	I
VCCCORE	J16	Power	I
VCCCORE	J15	Power	I
VCCCORE	J13	Power	I
VCCCORE	J12	Power	I
VCCCORE	J10	Power	I
VCCCORE	H38	Power	I
VCCCORE	H37	Power	I
VCCCORE	H35	Power	I
VCCCORE	H34	Power	I
VCCCORE	H32	Power	I
VCCCORE	H31	Power	I
VCCCORE	H29	Power	I
VCCCORE	H28	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 22 of 39)

Socket (EMTS)	Land #	Format	IO
VCCCORE	H26	Power	I
VCCCORE	H25	Power	I
VCCCORE	H22	Power	I
VCCCORE	H21	Power	I
VCCCORE	H19	Power	I
VCCCORE	H18	Power	I
VCCCORE	H16	Power	I
VCCCORE	H15	Power	I
VCCCORE	H13	Power	I
VCCCORE	H12	Power	I
VCCCORE	H10	Power	I
VCCCORE	G38	Power	I
VCCCORE	G37	Power	I
VCCCORE	G35	Power	I
VCCCORE	G34	Power	I
VCCCORE	G32	Power	I
VCCCORE	G31	Power	I
VCCCORE	G29	Power	I
VCCCORE	G28	Power	I
VCCCORE	G19	Power	I
VCCCORE	G18	Power	I
VCCCORE	G16	Power	I
VCCCORE	G15	Power	I
VCCCORE	G13	Power	I
VCCCORE	G12	Power	I
VCCCORE	G10	Power	I
VCCCORE	G9	Power	I
VCCCORE	F38	Power	I
VCCCORE	F37	Power	I
VCCCORE	F35	Power	I
VCCCORE	F34	Power	I
VCCCORE	F32	Power	I
VCCCORE	F31	Power	I
VCCCORE	F29	Power	I
VCCCORE	F28	Power	I
VCCCORE	F19	Power	I
VCCCORE	F18	Power	I
VCCCORE	F16	Power	I
VCCCORE	F15	Power	I
VCCCORE	F13	Power	I
VCCCORE	F12	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 23 of 39)

Socket (EMTS)	Land #	Format	IO
VCCCORE	F10	Power	I
VCCCORE	F9	Power	I
VCCCORE	E38	Power	I
VCCCORE	E37	Power	I
VCCCORE	E35	Power	I
VCCCORE	E34	Power	I
VCCCORE	E32	Power	I
VCCCORE	E31	Power	I
VCCCORE	E29	Power	I
VCCCORE	E28	Power	I
VCCCORE	E19	Power	I
VCCCORE	E18	Power	I
VCCCORE	E16	Power	I
VCCCORE	E15	Power	I
VCCCORE	E13	Power	I
VCCCORE	E12	Power	I
VCCCORE	E10	Power	I
VCCCORE	E9	Power	I
VCCCORE	D38	Power	I
VCCCORE	D37	Power	I
VCCCORE	D35	Power	I
VCCCORE	D34	Power	I
VCCCORE	D32	Power	I
VCCCORE	D31	Power	I
VCCCORE	D29	Power	I
VCCCORE	D28	Power	I
VCCCORE	D26	Power	I
VCCCORE	D25	Power	I
VCCCORE	D22	Power	I
VCCCORE	D21	Power	I
VCCCORE	D19	Power	I
VCCCORE	D18	Power	I
VCCCORE	D16	Power	I
VCCCORE	D15	Power	I
VCCCORE	D13	Power	I
VCCCORE	D12	Power	I
VCCCORE	D10	Power	I
VCCCORE	D9	Power	I
VCCCORE	C38	Power	I
VCCCORE	C37	Power	I
VCCCORE	C35	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 24 of 39)

Socket (EMTS)	Land #	Format	IO
VCCCORE	C34	Power	I
VCCCORE	C32	Power	I
VCCCORE	C31	Power	I
VCCCORE	C29	Power	I
VCCCORE	C28	Power	I
VCCCORE	C26	Power	I
VCCCORE	C25	Power	I
VCCCORE	C22	Power	I
VCCCORE	C21	Power	I
VCCCORE	C19	Power	I
VCCCORE	C18	Power	I
VCCCORE	C16	Power	I
VCCCORE	C15	Power	I
VCCCORE	C13	Power	I
VCCCORE	C12	Power	I
VCCCORE	C10	Power	I
VCCCORE	C9	Power	I
VCCCORE	B38	Power	I
VCCCORE	B37	Power	I
VCCCORE	B35	Power	I
VCCCORE	B34	Power	I
VCCCORE	B32	Power	I
VCCCORE	B31	Power	I
VCCCORE	B29	Power	I
VCCCORE	B28	Power	I
VCCCORE	B26	Power	I
VCCCORE	B25	Power	I
VCCCORE	B22	Power	I
VCCCORE	B21	Power	I
VCCCORE	B19	Power	I
VCCCORE	B18	Power	I
VCCCORE	B16	Power	I
VCCCORE	B15	Power	I
VCCCORE	B13	Power	I
VCCCORE	B12	Power	I
VCCCORE	B10	Power	I
VCCCORE	B9	Power	I
VCCCORE	A38	Power	I
VCCCORE	A37	Power	I
VCCCORE	A35	Power	I
VCCCORE	A34	Power	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 25 of 39)

Socket (EMTS)	Land #	Format	IO
VCCCORE	A32	Power	I
VCCCORE	A31	Power	I
VCCCORE	A29	Power	I
VCCCORE	A28	Power	I
VCCCORE	A26	Power	I
VCCCORE	A21	Power	I
VCCCORE	A19	Power	I
VCCCORE	A18	Power	I
VCCCORE	A16	Power	I
VCCCORE	A15	Power	I
VCCCORE	A13	Power	I
VCCCORE	A12	Power	I
VCCCORE	A10	Power	I
VCCCORE	A9	Power	I
VCORESENSE	F7	Power	IO
VID[0]	E7	CMOS	IO
VID[1]	E6	CMOS	IO
VID[2]	D7	CMOS	IO
VID[3]	D6	CMOS	IO
VID[4]	C7	CMOS	IO
VID[5]	C6	CMOS	IO
VID[6]	B7	CMOS	IO
VID[7]	A6	CMOS	IO
VIO_VID[1]	BH38	CMOS	O
VIO_VID[2]	BK38	CMOS	O
VIO_VID[3]	BM38	CMOS	O
VIO_VID[4]	BM39	CMOS	O
VIOC	AA42	POWER	I
VIOC	AC36	POWER	I
VIOC	AC42	POWER	I
VIOC	AD42	POWER	I
VIOC	AF36	POWER	I
VIOC	AF42	POWER	I
VIOC	AG42	POWER	I
VIOC	AJ36	POWER	I
VIOC	AJ42	POWER	I
VIOC	AK42	POWER	I
VIOC	AM36	POWER	I
VIOC	AM42	POWER	I
VIOC	AN42	POWER	I
VIOC	AR36	POWER	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 26 of 39)

Socket (EMTS)	Land #	Format	IO
VIOC	AR42	POWER	I
VIOC	AT42	POWER	I
VIOC	AV36	POWER	I
VIOC	AV42	POWER	I
VIOC	AW42	POWER	I
VIOC	BA36	POWER	I
VIOC	BA42	POWER	I
VIOC	BB37	POWER	I
VIOC	BB42	POWER	I
VIOC	BD42	POWER	I
VIOC	BE42	POWER	I
VIOC	BF41	POWER	I
VIOC	BG36	POWER	I
VIOC	BG37	POWER	I
VIOC	BG38	POWER	I
VIOC	BG39	POWER	I
VIOC	BG41	POWER	I
VIOC	BH34	POWER	I
VIOC	BH35	POWER	I
VIOC	BH41	POWER	I
VIOC	BK34	POWER	I
VIOC	BL34	POWER	I
VIOC	M36	POWER	I
VIOC	P36	POWER	I
VIOC	U36	POWER	I
VIOC	V42	POWER	I
VIOC	V43	POWER	I
VIOC	V44	POWER	I
VIOC	V45	POWER	I
VIOC	Y36	POWER	I
VIOC	Y42	POWER	I
VIOF	AB9	POWER	I
VIOF	AC10	POWER	I
VIOF	AC11	POWER	I
VIOF	AE9	POWER	I
VIOF	AF11	POWER	I
VIOF	AJ10	POWER	I
VIOF	AJ11	POWER	I
VIOF	AL10	POWER	I
VIOF	AM11	POWER	I
VIOF	AN10	POWER	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 27 of 39)

Socket (EMTS)	Land #	Format	IO
VIOF	AN8	POWER	I
VIOF	AP9	POWER	I
VIOF	AR10	POWER	I
VIOF	AR11	POWER	I
VIOF	AT9	POWER	I
VIOF	AU9	POWER	I
VIOF	AV10	POWER	I
VIOF	AV11	POWER	I
VIOF	BA1	POWER	I
VIOF	BA10	POWER	I
VIOF	BA11	POWER	I
VIOF	BA2	POWER	I
VIOF	BA3	POWER	I
VIOF	BA7	POWER	I
VIOF	BA8	POWER	I
VIOF	BB10	POWER	I
VIOF	BB11	POWER	I
VIOF	BB2	POWER	I
VIOF	BB4	POWER	I
VIOF	BB5	POWER	I
VIOF	BB6	POWER	I
VIOF	BB8	POWER	I
VIOF	P10	POWER	I
VIOF	P11	POWER	I
VIOF	R10	POWER	I
VIOF	R11	POWER	I
VIOF	T1	POWER	I
VIOF	T2	POWER	I
VIOF	T4	POWER	I
VIOF	T6	POWER	I
VIOF	T7	POWER	I
VIOF	T8	POWER	I
VIOF	U1	POWER	I
VIOF	U10	POWER	I
VIOF	U11	POWER	I
VIOF	U5	POWER	I
VIOF	U8	POWER	I
VIOF	U9	POWER	I
VIOF	Y11	POWER	I
VIOPWRGOOD	H41	CMOS	I
VREG	AJ2	POWER	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 28 of 39)

Socket (EMTS)	Land #	Format	IO
VREG	AK1	POWER	I
VREG	AK2	POWER	I
VREG	AK3	POWER	I
VREG	AK4	POWER	I
VREG	AL1	POWER	I
VREG	AL2	POWER	I
VREG	AL3	POWER	I
VREG	AL4	POWER	I
VREG	AL5	POWER	I
VSS	A11	GND	I
VSS	A14	GND	I
VSS	A17	GND	I
VSS	A2	GND	I
VSS	A20	GND	I
VSS	A27	GND	I
VSS	A3	GND	I
VSS	A30	GND	I
VSS	A33	GND	I
VSS	A36	GND	I
VSS	A39	GND	I
VSS	A4	GND	I
VSS	A40	GND	I
VSS	A42	GND	I
VSS	A43	GND	I
VSS	A44	GND	I
VSS	A45	GND	I
VSS	A7	GND	I
VSS	A8	GND	I
VSS	AA11	GND	I
VSS	AA3	GND	I
VSS	AA36	GND	I
VSS	AA41	GND	I
VSS	AA46	GND	I
VSS	AA5	GND	I
VSS	AA9	GND	I
VSS	AB10	GND	I
VSS	AB11	GND	I
VSS	AB36	GND	I
VSS	AB38	GND	I
VSS	AB42	GND	I
VSS	AB44	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 29 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	AB7	GND	I
VSS	AC1	GND	I
VSS	AC39	GND	I
VSS	AC4	GND	I
VSS	AC9	GND	I
VSS	AD10	GND	I
VSS	AD11	GND	I
VSS	AD36	GND	I
VSS	AD41	GND	I
VSS	AD45	GND	I
VSS	AD5	GND	I
VSS	AD7	GND	I
VSS	AE10	GND	I
VSS	AE11	GND	I
VSS	AE3	GND	I
VSS	AE36	GND	I
VSS	AE37	GND	I
VSS	AE42	GND	I
VSS	AE7	GND	I
VSS	AF39	GND	I
VSS	AF44	GND	I
VSS	AF9	GND	I
VSS	AG11	GND	I
VSS	AG36	GND	I
VSS	AG4	GND	I
VSS	AG41	GND	I
VSS	AG8	GND	I
VSS	AH11	GND	I
VSS	AH2	GND	I
VSS	AH36	GND	I
VSS	AH37	GND	I
VSS	AH42	GND	I
VSS	AH6	GND	I
VSS	AJ1	GND	I
VSS	AJ3	GND	I
VSS	AJ39	GND	I
VSS	AJ44	GND	I
VSS	AK10	GND	I
VSS	AK11	GND	I
VSS	AK36	GND	I
VSS	AK41	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 30 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	AK46	GND	I
VSS	AK5	GND	I
VSS	AK7	GND	I
VSS	AL11	GND	I
VSS	AL36	GND	I
VSS	AL37	GND	I
VSS	AL42	GND	I
VSS	AL44	GND	I
VSS	AL7	GND	I
VSS	AL9	GND	I
VSS	AM2	GND	I
VSS	AM3	GND	I
VSS	AM39	GND	I
VSS	AM5	GND	I
VSS	AN11	GND	I
VSS	AN3	GND	I
VSS	AN36	GND	I
VSS	AN41	GND	I
VSS	AN45	GND	I
VSS	AN7	GND	I
VSS	AN9	GND	I
VSS	AP1	GND	I
VSS	AP11	GND	I
VSS	AP36	GND	I
VSS	AP37	GND	I
VSS	AP4	GND	I
VSS	AP42	GND	I
VSS	AP44	GND	I
VSS	AP5	GND	I
VSS	AR39	GND	I
VSS	AR5	GND	I
VSS	AR7	GND	I
VSS	AR9	GND	I
VSS	AT1	GND	I
VSS	AT10	GND	I
VSS	AT11	GND	I
VSS	AT3	GND	I
VSS	AT36	GND	I
VSS	AT41	GND	I
VSS	AT45	GND	I
VSS	AU1	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 31 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	AU10	GND	I
VSS	AU11	GND	I
VSS	AU36	GND	I
VSS	AU37	GND	I
VSS	AU42	GND	I
VSS	AU44	GND	I
VSS	AU6	GND	I
VSS	AU8	GND	I
VSS	AV39	GND	I
VSS	AV5	GND	I
VSS	AV9	GND	I
VSS	AW10	GND	I
VSS	AW11	GND	I
VSS	AW3	GND	I
VSS	AW36	GND	I
VSS	AW41	GND	I
VSS	AW45	GND	I
VSS	AW7	GND	I
VSS	AY1	GND	I
VSS	AY10	GND	I
VSS	AY11	GND	I
VSS	AY36	GND	I
VSS	AY37	GND	I
VSS	AY42	GND	I
VSS	AY44	GND	I
VSS	AY6	GND	I
VSS	B1	GND	I
VSS	B11	GND	I
VSS	B14	GND	I
VSS	B17	GND	I
VSS	B2	GND	I
VSS	B20	GND	I
VSS	B23	GND	I
VSS	B24	GND	I
VSS	B27	GND	I
VSS	B3	GND	I
VSS	B30	GND	I
VSS	B33	GND	I
VSS	B36	GND	I
VSS	B39	GND	I
VSS	B40	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 32 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	B45	GND	I
VSS	B6	GND	I
VSS	B8	GND	I
VSS	BA39	GND	I
VSS	BA4	GND	I
VSS	BA9	GND	I
VSS	BB3	GND	I
VSS	BB36	GND	I
VSS	BB41	GND	I
VSS	BB45	GND	I
VSS	BB7	GND	I
VSS	BB9	GND	I
VSS	BC11	GND	I
VSS	BC12	GND	I
VSS	BC13	GND	I
VSS	BC14	GND	I
VSS	BC16	GND	I
VSS	BC19	GND	I
VSS	BC22	GND	I
VSS	BC25	GND	I
VSS	BC28	GND	I
VSS	BC31	GND	I
VSS	BC34	GND	I
VSS	BC37	GND	I
VSS	BC42	GND	I
VSS	BC5	GND	I
VSS	BD11	GND	I
VSS	BD14	GND	I
VSS	BD16	GND	I
VSS	BD19	GND	I
VSS	BD22	GND	I
VSS	BD25	GND	I
VSS	BD28	GND	I
VSS	BD3	GND	I
VSS	BD31	GND	I
VSS	BD39	GND	I
VSS	BD44	GND	I
VSS	BD7	GND	I
VSS	BE1	GND	I
VSS	BE13	GND	I
VSS	BE14	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 33 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	BE16	GND	I
VSS	BE19	GND	I
VSS	BE22	GND	I
VSS	BE25	GND	I
VSS	BE28	GND	I
VSS	BE31	GND	I
VSS	BE36	GND	I
VSS	BE41	GND	I
VSS	BE46	GND	I
VSS	BE9	GND	I
VSS	BF11	GND	I
VSS	BF13	GND	I
VSS	BF16	GND	I
VSS	BF19	GND	I
VSS	BF28	GND	I
VSS	BF31	GND	I
VSS	BF34	GND	I
VSS	BF38	GND	I
VSS	BF42	GND	I
VSS	BF5	GND	I
VSS	BF7	GND	I
VSS	BG12	GND	I
VSS	BG14	GND	I
VSS	BG16	GND	I
VSS	BG19	GND	I
VSS	BG28	GND	I
VSS	BG3	GND	I
VSS	BG31	GND	I
VSS	BG40	GND	I
VSS	BG44	GND	I
VSS	BG7	GND	I
VSS	BH13	GND	I
VSS	BH19	GND	I
VSS	BH28	GND	I
VSS	BH31	GND	I
VSS	BH36	GND	I
VSS	BH46	GND	I
VSS	BH9	GND	I
VSS	BJ1	GND	I
VSS	BJ11	GND	I
VSS	BJ17	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 34 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	BJ19	GND	I
VSS	BJ22	GND	I
VSS	BJ25	GND	I
VSS	BJ28	GND	I
VSS	BJ3	GND	I
VSS	BJ31	GND	I
VSS	BJ32	GND	I
VSS	BJ34	GND	I
VSS	BJ38	GND	I
VSS	BJ42	GND	I
VSS	BJ44	GND	I
VSS	BJ46	GND	I
VSS	BJ5	GND	I
VSS	BJ7	GND	I
VSS	BK1	GND	I
VSS	BK15	GND	I
VSS	BK19	GND	I
VSS	BK22	GND	I
VSS	BK25	GND	I
VSS	BK28	GND	I
VSS	BK31	GND	I
VSS	BK40	GND	I
VSS	BK46	GND	I
VSS	BK7	GND	I
VSS	BL1	GND	I
VSS	BL13	GND	I
VSS	BL19	GND	I
VSS	BL2	GND	I
VSS	BL22	GND	I
VSS	BL25	GND	I
VSS	BL28	GND	I
VSS	BL3	GND	I
VSS	BL31	GND	I
VSS	BL33	GND	I
VSS	BL36	GND	I
VSS	BL38	GND	I
VSS	BL4	GND	I
VSS	BL44	GND	I
VSS	BL45	GND	I
VSS	BL46	GND	I
VSS	BL9	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 35 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	BM11	GND	I
VSS	BM16	GND	I
VSS	BM19	GND	I
VSS	BM2	GND	I
VSS	BM28	GND	I
VSS	BM3	GND	I
VSS	BM31	GND	I
VSS	BM34	GND	I
VSS	BM4	GND	I
VSS	BM40	GND	I
VSS	BM42	GND	I
VSS	BM43	GND	I
VSS	BM44	GND	I
VSS	BM45	GND	I
VSS	BM7	GND	I
VSS	C1	GND	I
VSS	C11	GND	I
VSS	C14	GND	I
VSS	C17	GND	I
VSS	C2	GND	I
VSS	C20	GND	I
VSS	C23	GND	I
VSS	C24	GND	I
VSS	C27	GND	I
VSS	C30	GND	I
VSS	C33	GND	I
VSS	C36	GND	I
VSS	C41	GND	I
VSS	C43	GND	I
VSS	C5	GND	I
VSS	C8	GND	I
VSS	D1	GND	I
VSS	D11	GND	I
VSS	D14	GND	I
VSS	D17	GND	I
VSS	D20	GND	I
VSS	D23	GND	I
VSS	D24	GND	I
VSS	D27	GND	I
VSS	D30	GND	I
VSS	D33	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 36 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	D36	GND	I
VSS	D39	GND	I
VSS	D45	GND	I
VSS	D46	GND	I
VSS	D8	GND	I
VSS	E11	GND	I
VSS	E14	GND	I
VSS	E17	GND	I
VSS	E20	GND	I
VSS	E27	GND	I
VSS	E30	GND	I
VSS	E33	GND	I
VSS	E36	GND	I
VSS	E41	GND	I
VSS	E43	GND	I
VSS	E5	GND	I
VSS	E8	GND	I
VSS	F11	GND	I
VSS	F14	GND	I
VSS	F17	GND	I
VSS	F20	GND	I
VSS	F27	GND	I
VSS	F3	GND	I
VSS	F30	GND	I
VSS	F33	GND	I
VSS	F36	GND	I
VSS	F45	GND	I
VSS	F8	GND	I
VSS	G1	GND	I
VSS	G11	GND	I
VSS	G14	GND	I
VSS	G17	GND	I
VSS	G20	GND	I
VSS	G27	GND	I
VSS	G30	GND	I
VSS	G33	GND	I
VSS	G36	GND	I
VSS	G39	GND	I
VSS	G40	GND	I
VSS	G42	GND	I
VSS	G5	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 37 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	G8	GND	I
VSS	H11	GND	I
VSS	H14	GND	I
VSS	H17	GND	I
VSS	H20	GND	I
VSS	H23	GND	I
VSS	H24	GND	I
VSS	H27	GND	I
VSS	H30	GND	I
VSS	H33	GND	I
VSS	H36	GND	I
VSS	H39	GND	I
VSS	H4	GND	I
VSS	H40	GND	I
VSS	H44	GND	I
VSS	H46	GND	I
VSS	H8	GND	I
VSS	J11	GND	I
VSS	J14	GND	I
VSS	J17	GND	I
VSS	J2	GND	I
VSS	J20	GND	I
VSS	J23	GND	I
VSS	J24	GND	I
VSS	J27	GND	I
VSS	J30	GND	I
VSS	J33	GND	I
VSS	J36	GND	I
VSS	J39	GND	I
VSS	J7	GND	I
VSS	K11	GND	I
VSS	K14	GND	I
VSS	K17	GND	I
VSS	K20	GND	I
VSS	K23	GND	I
VSS	K24	GND	I
VSS	K27	GND	I
VSS	K30	GND	I
VSS	K33	GND	I
VSS	K36	GND	I
VSS	K39	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 38 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	K40	GND	I
VSS	K41	GND	I
VSS	K42	GND	I
VSS	K43	GND	I
VSS	K44	GND	I
VSS	K45	GND	I
VSS	K5	GND	I
VSS	K7	GND	I
VSS	K9	GND	I
VSS	L11	GND	I
VSS	L3	GND	I
VSS	L36	GND	I
VSS	L37	GND	I
VSS	L4	GND	I
VSS	L45	GND	I
VSS	L46	GND	I
VSS	L6	GND	I
VSS	M1	GND	I
VSS	M11	GND	I
VSS	M2	GND	I
VSS	M37	GND	I
VSS	M42	GND	I
VSS	M46	GND	I
VSS	M8	GND	I
VSS	N10	GND	I
VSS	N11	GND	I
VSS	N36	GND	I
VSS	N39	GND	I
VSS	N44	GND	I
VSS	N5	GND	I
VSS	N9	GND	I
VSS	P3	GND	I
VSS	P42	GND	I
VSS	P43	GND	I
VSS	P7	GND	I
VSS	R1	GND	I
VSS	R36	GND	I
VSS	R37	GND	I
VSS	R40	GND	I
VSS	R46	GND	I
VSS	T10	GND	I

Table 4-1. Pin List, Sorted by Socket Name (Sheet 39 of 39)

Socket (EMTS)	Land #	Format	IO
VSS	T11	GND	I
VSS	T3	GND	I
VSS	T36	GND	I
VSS	T37	GND	I
VSS	T44	GND	I
VSS	T5	GND	I
VSS	T9	GND	I
VSS	U2	GND	I
VSS	U39	GND	I
VSS	U42	GND	I
VSS	U7	GND	I
VSS	V10	GND	I
VSS	V11	GND	I
VSS	V36	GND	I
VSS	V41	GND	I
VSS	V46	GND	I
VSS	V5	GND	I
VSS	V9	GND	I
VSS	W10	GND	I
VSS	W11	GND	I
VSS	W3	GND	I
VSS	W36	GND	I
VSS	W37	GND	I
VSS	W42	GND	I
VSS	W6	GND	I
VSS	W7	GND	I
VSS	Y1	GND	I
VSS	Y39	GND	I
VSS	Y44	GND	I
VSSCACHESENSE	BK17	Power	IO
VSSCORESENSE	F6	Power	IO

4.1.2 Processor Pin List, Sorted by Land Number

Table 4-2. Pin List, Sorted by land Number (Sheet 1 of 39)

Land #	Socket (EMTS)	Format	IO
A1	TEST[0]		I
A10	VCCCORE	POWER	I
A11	VSS	GND	I
A12	VCCCORE	POWER	I
A13	VCCCORE	POWER	I
A14	VSS	GND	I
A15	VCCCORE	POWER	I
A16	VCCCORE	POWER	I
A17	VSS	GND	I
A18	VCCCORE	POWER	I
A19	VCCCORE	POWER	I
A2	VSS	GND	I
A20	VSS	GND	I
A21	VCCCORE	POWER	I
A26	VCCCORE	POWER	I
A27	VSS	GND	I
A28	VCCCORE	POWER	I
A29	VCCCORE	POWER	I
A3	VSS	GND	I
A30	VSS	GND	I
A31	VCCCORE	POWER	I
A32	VCCCORE	POWER	I
A33	VSS	GND	I
A34	VCCCORE	POWER	I
A35	VCCCORE	POWER	I
A36	VSS	GND	I
A37	VCCCORE	POWER	I
A38	VCCCORE	POWER	I
A39	VSS	GND	I
A4	VSS	GND	I
A40	VSS	GND	I
A41	QPI3_DTX_DN[14]	SCID Diff.	O
A42	VSS	GND	I
A43	VSS	GND	I
A44	VSS	GND	I
A45	VSS	GND	I
A46	TEST[1]		IO
A5	ISENSE_DP	GTL	I
A6	VID[7]	CMOS	IO

Table 4-2. Pin List, Sorted by land Number (Sheet 2 of 39)

Land #	Socket (EMTS)	Format	IO
A7	VSS	GND	I
A8	VSS	GND	I
A9	VCCCORE	POWERf	I
AA1	FBD1NBIDN[12]	Differential	I
AA10	RSVD		IO
AA11	VSS	GND	I
AA2	RSVD		IO
AA3	VSS	GND	I
AA36	VSS	GND	I
AA37	QPI2_DRX_DN[19]	SCID Diff.	I
AA38	SYSCLK_LAI_N	Differential	I
AA39	SYSCLK_LAI	Differential	I
AA4	FBD1NBIDP[0]	Differential	I
AA40	QPI2_DRX_DN[10]	SCID Diff.	I
AA41	VSS	GND	I
AA42	VIOC	POWER	I
AA43	QPI2_DTX_DP[17]	SCID Diff.	O
AA44	QPI2_DTX_DN[17]	SCID Diff.	O
AA45	QPI2_DTX_DN[14]	SCID Diff.	O
AA46	VSS	GND	I
AA5	VSS	GND	I
AA6	FBD1NBICN[12]	Differential	I
AA7	FBD1NBICP[6]	Differential	I
AA8	FBD1NBICN[6]	Differential	I
AA9	VSS	GND	I
AB1	FBD1NBIDP[12]	Differential	I
AB10	VSS	GND	I
AB11	VSS	GND	I
AB2	FBD1NBICLKDN0	Differential	I
AB3	RSVD		IO
AB36	VSS	GND	I
AB37	QPI2_DRX_DP[19]	SCID Diff.	I
AB38	VSS	GND	I
AB39	QPI2_CLKRX_DP	SCID Diff.	I
AB4	FBD1NBIDN[0]	Differential	I
AB40	QPI2_CLKRX_DN	SCID Diff.	I
AB41	QPI2_DRX_DP[9]	SCID Diff.	I
AB42	VSS	GND	I
AB43	QPI2_DTX_DN[19]	SCID Diff.	O

Table 4-2. Pin List, Sorted by land Number (Sheet 3 of 39)

Land #	Socket (EMTS)	Format	IO
AB44	VSS	GND	I
AB45	QPI2_DTX_DP[13]	SCID Diff.	O
AB46	QPI2_DTX_DN[13]	SCID Diff.	O
AB5	FBD1NBICLKCN0	Differential	I
AB6	FBD1NBICP[12]	Differential	I
AB7	VSS	GND	I
AB8	FBD1NBICP[0]	Differential	I
AB9	VIOF	POWER	I
AC1	VSS	GND	I
AC10	VIOF	POWER	I
AC11	VIOF	POWER	I
AC2	FBD1NBICLKDP0	Differential	I
AC3	FBD1NBIDN[13]	Differential	I
AC36	VIOC	POWER	I
AC37	QPI2_DRX_DN[0]	SCID Diff.	I
AC38	QPI2_DRX_DP[0]	SCID Diff.	I
AC39	VSS	GND	I
AC4	VSS	GND	I
AC40	QPI2_DRX_DP[8]	SCID Diff.	I
AC41	QPI2_DRX_DN[9]	SCID Diff.	I
AC42	VIOC	POWER	I
AC43	QPI2_DTX_DP[19]	SCID Diff.	O
AC44	QPI2_DTX_DP[12]	SCID Diff.	O
AC45	QPI2_DTX_DN[12]	SCID Diff.	O
AC46	QPI2_DTX_DP[11]	SCID Diff.	O
AC5	FBD1NBICLKCP0	Differential	I
AC6	FBD1NBICN[13]	Differential	I
AC7	FBD1NBICP[13]	Differential	I
AC8	FBD1NBICN[0]	Differential	I
AC9	VSS	GND	I
AD1	FBD1NBIDN[5]	Differential	I
AD10	VSS	GND	I
AD11	VSS	GND	I
AD2	FBD1NBIDP[5]	Differential	I
AD3	FBD1NBIDP[13]	Differential	I
AD36	VSS	GND	I
AD37	RSVD		IO
AD38	QPI2_DRX_DN[1]	SCID Diff.	I
AD39	QPI2_DRX_DP[1]	SCID Diff.	I
AD4	FBD1NBIDP[1]	Differential	I
AD40	QPI2_DRX_DN[8]	SCID Diff.	I

Table 4-2. Pin List, Sorted by land Number (Sheet 4 of 39)

Land #	Socket (EMTS)	Format	IO
AD41	VSS	GND	I
AD42	VIOC	POWER	I
AD43	QPI2_DTX_DN[10]	SCID Diff.	O
AD44	QPI2_DTX_DP[10]	SCID Diff.	O
AD45	VSS	GND	I
AD46	QPI2_DTX_DN[11]	SCID Diff.	O
AD5	VSS	GND	I
AD6	FBD1NBICN[5]	Differential	I
AD7	VSS	GND	I
AD8	FBD1NBICN[1]	Differential	I
AD9	FBD1NBICP[1]	Differential	I
AE10	VSS	GND	I
AE11	VSS	GND	I
AE2	FBD1NBIDN[4]	Differential	I
AE3	VSS	GND	I
AE36	VSS	GND	I
AE37	VSS	GND	I
AE38	RSVD		IO
AE39	QPI2_DRX_DP[7]	SCID Diff.	I
AE4	FBD1NBIDN[1]	Differential	I
AE40	QPI2_DRX_DN[7]	SCID Diff.	I
AE41	QPI2_DRX_DP[6]	SCID Diff.	I
AE42	VSS	GND	I
AE43	QPI2_DTX_DN[0]	SCID Diff.	O
AE44	QPI2_CLKTX_DN	SCID Diff.	O
AE45	QPI2_CLKTX_DP	SCID Diff.	O
AE5	FBD1NBICN[4]	Differential	I
AE6	FBD1NBICP[5]	Differential	I
AE7	VSS	GND	I
AE8	FBD1NBICN[2]	Differential	I
AE9	VIOF	POWER	I
AF10	RSVD		IO
AF11	VIOF	POWER	I
AF2	FBD1NBIDP[4]	Differential	I
AF3	FBD1NBIDN[3]	Differential	I
AF36	VIOC	POWER	I
AF37	QPI2_DRX_DN[2]	SCID Diff.	I
AF38	QPI2_DRX_DP[2]	SCID Diff.	I
AF39	VSS	GND	I
AF4	FBD1NBIDP[3]	Differential	I
AF40	QPI2_DRX_DP[5]	SCID Diff.	I

Table 4-2. Pin List, Sorted by land Number (Sheet 5 of 39)

Land #	Socket (EMTS)	Format	IO
AF41	QPI2_DRX_DN[6]	SCID Diff.	I
AF42	VIOC	POWER	I
AF43	QPI2_DTX_DP[0]	SCID Diff.	O
AF44	VSS	GND	I
AF45	QPI2_DTX_DP[9]	SCID Diff.	O
AF5	FBD1NBICP[4]	Differential	I
AF6	FBD1NBICN[3]	Differential	I
AF7	FBD1NBICP[3]	Differential	I
AF8	FBD1NBICP[2]	Differential	I
AF9	VSS	GND	I
AG10	RSVD		IO
AG11	VSS	GND	I
AG2	FBD1NBIDN[2]	Differential	I
AG3	FBD1NBIDP[2]	Differential	I
AG36	VSS	GND	I
AG37	RSVD		IO
AG38	QPI2_DRX_DN[3]	SCID Diff.	I
AG39	QPI2_DRX_DP[3]	SCID Diff.	I
AG4	VSS	GND	I
AG40	QPI2_DRX_DN[5]	SCID Diff.	I
AG41	VSS	GND	I
AG42	VIOC	POWER	I
AG43	QPI2_DTX_DN[8]	SCID Diff.	O
AG44	QPI2_DTX_DP[8]	SCID Diff.	O
AG45	QPI2_DTX_DN[9]	SCID Diff.	O
AG5	RSVD		IO
AG6	RSVD		IO
AG7	RSVD		IO
AG8	VSS	GND	I
AG9	RSVD		IO
AH10	RSVD		IO
AH11	VSS	GND	I
AH2	VSS	GND	I
AH3	RSVD		IO
AH36	VSS	GND	I
AH37	VSS	GND	I
AH38	RSVD		IO
AH39	QPI2_DRX_DP[4]	SCID Diff.	I
AH4	RSVD		IO
AH40	QPI2_DRX_DN[4]	SCID Diff.	I
AH41	QPI1_DRX_DN[4]	SCID Diff.	I

Table 4-2. Pin List, Sorted by land Number (Sheet 6 of 39)

Land #	Socket (EMTS)	Format	IO
AH42	VSS	GND	I
AH43	QPI2_DTX_DN[1]	SCID Diff.	O
AH44	QPI2_DTX_DN[7]	SCID Diff.	O
AH45	QPI2_DTX_DP[7]	SCID Diff.	O
AH5	RSVD		IO
AH6	VSS	GND	I
AH7	RSVD		IO
AH8	RSVD		IO
AH9	RSVD		IO
AJ1	VSS	GND	I
AJ10	VIOF	POWER	I
AJ11	VIOF	POWER	I
AJ2	VREG	POWER	I
AJ3	VSS	GND	I
AJ36	VIOC	POWER	I
AJ37	QPI1_DRX_DN[2]	SCID Diff.	I
AJ38	QPI1_DRX_DP[2]	SCID Diff.	I
AJ39	VSS	GND	I
AJ4	RSVD		IO
AJ40	QPI1_DRX_DN[5]	SCID Diff.	I
AJ41	QPI1_DRX_DP[4]	SCID Diff.	I
AJ42	VIOC	POWER	I
AJ43	QPI2_DTX_DP[1]	SCID Diff.	O
AJ44	VSS	GND	I
AJ45	QPI2_DTX_DP[6]	SCID Diff.	O
AJ46	RSVD		IO
AJ5	RSVD		IO
AJ6	RSVD		IO
AJ7	RSVD		IO
AJ8	RSVD		IO
AJ9	RSVD		IO
AK1	VREG	POWER	I
AK10	VSS	GND	I
AK11	VSS	GND	I
AK2	VREG	POWER	I
AK3	VREG	POWER	I
AK36	VSS	GND	I
AK37	RSVD		IO
AK38	QPI1_DRX_DN[3]	SCID Diff.	I
AK39	QPI1_DRX_DP[3]	SCID Diff.	I
AK4	VREG	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 7 of 39)

Land #	Socket (EMTS)	Format	IO
AK40	QPI1_DRX_DP[5]	SCID Diff.	I
AK41	VSS	GND	I
AK42	VIOC	POWER	I
AK43	QPI2_DTX_DN[5]	SCID Diff.	O
AK44	QPI2_DTX_DP[5]	SCID Diff.	O
AK45	QPI2_DTX_DN[6]	SCID Diff.	O
AK46	VSS	GND	I
AK5	VSS	GND	I
AK6	RSVD		IO
AK7	VSS	GND	I
AK8	RSVD		IO
AK9	RSVD		IO
AL1	VREG	POWER	I
AL10	VIOF	POWER	I
AL11	VSS	GND	I
AL2	VREG	POWER	I
AL3	VREG	POWER	I
AL36	VSS	GND	I
AL37	VSS	GND	I
AL38	RSVD		IO
AL39	QPI1_DRX_DN[6]	SCID Diff.	I
AL4	VREG	POWER	I
AL40	QPI1_DRX_DP[6]	SCID Diff.	I
AL41	QPI1_DRX_DN[7]	SCID Diff.	I
AL42	VSS	GND	I
AL43	QPI2_DTX_DP[2]	SCID Diff.	O
AL44	VSS	GND	I
AL45	QPI2_DTX_DN[4]	SCID Diff.	O
AL46	QPI2_DTX_DP[4]	SCID Diff.	O
AL5	VREG	Power	I
AL6	RSVD		IO
AL7	VSS	GND	I
AL8	RSVD		IO
AL9	VSS	GND	I
AM1	FBD0SBOBN[7]	Differential	O
AM10	RSVD		IO
AM11	VIOF	POWER	I
AM2	VSS	GND	I
AM3	VSS	GND	I
AM36	VIOC	POWER	I
AM37	QPI1_DRX_DN[1]	SCID Diff.	I

Table 4-2. Pin List, Sorted by land Number (Sheet 8 of 39)

Land #	Socket (EMTS)	Format	IO
AM38	QPI1_DRX_DP[1]	SCID Diff.	I
AM39	VSS	GND	I
AM4	FBD0SBOBN[10]	Differential	O
AM40	QPI1_DRX_DN[8]	SCID Diff.	I
AM41	QPI1_DRX_DP[7]	SCID Diff.	I
AM42	VIOC	POWER	I
AM43	QPI2_DTX_DN[2]	SCID Diff.	O
AM44	QPI1_DTX_DP[3]	SCID Diff.	O
AM45	QPI1_DTX_DN[3]	SCID Diff.	O
AM46	QPI2_DTX_DP[3]	SCID Diff.	O
AM5	VSS	GND	I
AM6	RSVD		IO
AM7	RSVD		IO
AM8	RSVD		IO
AM9	RSVD		IO
AN1	FBD0SBOBP[7]	Differential	O
AN10	VIOF	POWER	I
AN11	VSS	GND	I
AN2	FBD0SBOBN[6]	Differential	O
AN3	VSS	GND	I
AN36	VSS	GND	I
AN37	RSVD		IO
AN38	QPI1_DRX_DN[0]	SCID Diff.	I
AN39	QPI1_DRX_DP[0]	SCID Diff.	I
AN4	FBD0SBOBP[10]	Differential	O
AN40	QPI1_DRX_DP[8]	SCID Diff.	I
AN41	VSS	GND	I
AN42	VIOC	POWER	I
AN43	QPI1_DTX_DN[2]	SCID Diff.	O
AN44	QPI1_DTX_DP[2]	SCID Diff.	O
AN45	VSS	GND	I
AN46	QPI2_DTX_DN[3]	SCID Diff.	O
AN5	FBD0SBOAP[7]	Differential	O
AN6	FBD0SBOAN[7]	Differential	O
AN7	VSS	GND	I
AN8	VIOF	POWER	I
AN9	VSS	GND	I
AP1	VSS	GND	I
AP10	Test-Hi	GTL	IO
AP11	VSS	GND	I
AP2	FBD0SBOBP[6]	Differential	O

Table 4-2. Pin List, Sorted by land Number (Sheet 9 of 39)

Land #	Socket (EMTS)	Format	IO
AP3	FBD0SBOBN[8]	Differential	O
AP36	VSS	GND	I
AP37	VSS	GND	I
AP38	RSVD		IO
AP39	QPI1_DRX_DN[9]	SCID Diff.	I
AP4	VSS	GND	I
AP40	QPI1_DRX_DP[9]	SCID Diff.	I
AP41	QPI1_CLKRX_DN	SCID Diff.	I
AP42	VSS	GND	I
AP43	QPI1_DTX_DP[1]	SCID Diff.	O
AP44	VSS	GND	I
AP45	QPI1_DTX_DN[4]	SCID Diff.	O
AP46	QPI1_DTX_DP[4]	SCID Diff.	O
AP5	VSS	GND	I
AP6	FBD0SBOAP[6]	Differential	O
AP7	FBD0SBOAN[6]	Differential	O
AP8	FBD0SBOAN[8]	Differential	O
AP9	VIOF	POWER	I
AR1	FBD0SBOBP[5]	Differential	O
AR10	VIOF	POWER	I
AR11	VIOF	POWER	I
AR2	FBD0SBOBN[5]	Differential	O
AR3	FBD0SBOBP[8]	Differential	O
AR36	VIOC	POWER	I
AR37	QPI1_DRX_DP[19]	SCID Diff.	I
AR38	QPI1_DRX_DN[19]	SCID Diff.	I
AR39	VSS	GND	I
AR4	FBD0SBOBN[9]	Differential	O
AR40	QPI1_DRX_DN[10]	SCID Diff.	I
AR41	QPI1_CLKRX_DP	SCID Diff.	I
AR42	VIOC	POWER	I
AR43	QPI1_DTX_DN[1]	SCID Diff.	O
AR44	QPI1_DTX_DN[5]	SCID Diff.	O
AR45	QPI1_DTX_DP[5]	SCID Diff.	O
AR46	QPI1_DTX_DN[6]	SCID Diff.	O
AR5	VSS	GND	I
AR6	FBD0SBOAN[9]	Differential	O
AR7	VSS	GND	I
AR8	FBD0SBOAP[8]	Differential	O
AR9	VSS	GND	I
AT1	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 10 of 39)

Land #	Socket (EMTS)	Format	IO
AT10	VSS	GND	I
AT11	VSS	GND	I
AT2	RSVD		IO
AT3	VSS	GND	I
AT36	VSS	GND	I
AT37	RSVD		IO
AT38	QPI1_DRX_DP[18]	SCID Diff.	I
AT39	QPI1_DRX_DN[18]	SCID Diff.	I
AT4	FBD0SBOBP[9]	Differential	O
AT40	QPI1_DRX_DP[10]	SCID Diff.	I
AT41	VSS	GND	I
AT42	VIOC	POWER	I
AT43	QPI1_DTX_DN[0]	SCID Diff.	O
AT44	QPI1_DTX_DP[0]	SCID Diff.	O
AT45	VSS	GND	I
AT46	QPI1_DTX_DP[6]	SCID Diff.	O
AT5	FBD0SBOCLKAP0	Differential	O
AT6	FBD0SBOAP[9]	Differential	O
AT7	FBD0SBOAP[5]	Differential	O
AT8	FBD0SBOAN[5]	Differential	O
AT9	VIOF	POWER	I
AU1	VSS	GND	I
AU10	VSS	GND	I
AU11	VSS	GND	I
AU2	RSVD		IO
AU3	FBD0SBOCLKBN0	Differential	O
AU36	VSS	GND	I
AU37	VSS	GND	I
AU38	RSVD		IO
AU39	QPI1_DRX_DN[11]	SCID Diff.	I
AU4	FBD0SBOCLKBP0	Differential	O
AU40	QPI1_DRX_DP[11]	SCID Diff.	I
AU41	QPI1_DRX_DN[12]	SCID Diff.	I
AU42	VSS	GND	I
AU43	QPI1_DTX_DP[19]	SCID Diff.	O
AU44	VSS	GND	I
AU45	QPI1_DTX_DN[7]	SCID Diff.	O
AU46	QPI1_DTX_DP[7]	SCID Diff.	O
AU5	FBD0SBOCLKAN0	Differential	O
AU6	VSS	GND	I
AU7	FBD0SBOAN[4]	Differential	O

Table 4-2. Pin List, Sorted by land Number (Sheet 11 of 39)

Land #	Socket (EMTS)	Format	IO
AU8	VSS	GND	I
AU9	VIOF	POWER	I
AV1	FBD0SBOBN[3]	Differential	O
AV10	VIOF	POWER	I
AV11	VIOF	POWER	I
AV2	FBD0SBOBP[4]	Differential	O
AV3	FBD0SBOBN[4]	Differential	O
AV36	VIOC	POWER	I
AV37	QPI1_DRX_DP[16]	SCID Diff.	I
AV38	QPI1_DRX_DN[16]	SCID Diff.	I
AV39	VSS	GND	I
AV4	FBD0SBOBP[0]	Differential	O
AV40	QPI1_DRX_DN[13]	SCID Diff.	I
AV41	QPI1_DRX_DP[12]	SCID Diff.	I
AV42	VIOC	POWER	I
AV43	QPI1_DTX_DN[19]	SCID Diff.	O
AV44	QPI1_DTX_DN[8]	SCID Diff.	O
AV45	QPI1_DTX_DP[8]	SCID Diff.	O
AV46	QPI1_DTX_DN[9]	SCID Diff.	O
AV5	VSS	GND	I
AV6	FBD0SBOAN[3]	Differential	O
AV7	FBD0SBOAP[4]	Differential	O
AV8	FBD0SBOAP[10]	Differential	O
AV9	VSS	GND	I
AW1	FBD0SBOBP[3]	Differential	O
AW10	VSS	GND	I
AW11	VSS	GND	I
AW2	FBD0SBOBN[2]	Differential	O
AW3	VSS	GND	I
AW36	VSS	GND	I
AW37	RSVD		IO
AW38	QPI1_DRX_DP[14]	SCID Diff.	I
AW39	QPI1_DRX_DN[14]	SCID Diff.	I
AW4	FBD0SBOBN[0]	Differential	O
AW40	QPI1_DRX_DP[13]	SCID Diff.	I
AW41	VSS	GND	I
AW42	VIOC	POWER	I
AW43	QPI1_DTX_DP[18]	SCID Diff.	O
AW44	QPI1_DTX_DN[18]	SCID Diff.	O
AW45	VSS	GND	I
AW46	QPI1_DTX_DP[9]	SCID Diff.	O

Table 4-2. Pin List, Sorted by land Number (Sheet 12 of 39)

Land #	Socket (EMTS)	Format	IO
AW5	FBD0SBOAN[2]	Differential	O
AW6	FBD0SBOAP[3]	Differential	O
AW7	VSS	GND	I
AW8	FBD0SBOAN[10]	Differential	O
AW9	Proc_ID[0]	CMOS	O
AY1	VSS	GND	I
AY10	VSS	GND	I
AY11	VSS	GND	I
AY2	FBD0SBOBP[2]	Differential	O
AY3	FBD0SBOBN[1]	Differential	O
AY36	VSS	GND	I
AY37	VSS	GND	I
AY38	RSVD		IO
AY39	QPI1_DRX_DP[15]	SCID Diff.	I
AY4	FBD0SBOBP[1]	Differential	O
AY40	QPI1_DRX_DN[15]	SCID Diff.	I
AY41	QPI0_DRX_DN[1]	SCID Diff.	I
AY42	VSS	GND	I
AY43	QPI1_DTX_DP[17]	SCID Diff.	O
AY44	VSS	GND	I
AY45	QPI1_CLKTX_DN	SCID Diff.	O
AY46	QPI1_CLKTX_DP	SCID Diff.	O
AY5	FBD0SBOAP[2]	Differential	O
AY6	VSS	GND	I
AY7	FBD0SBOAN[1]	Differential	O
AY8	FBD0SBOAP[1]	Differential	O
AY9	Proc_ID[1]	CMOS	O
B1	VSS	GND	I
B10	VCCCORE	POWER	I
B11	VSS	GND	I
B12	VCCCORE	POWER	I
B13	VCCCORE	POWER	I
B14	VSS	GND	I
B15	VCCCORE	POWER	I
B16	VCCCORE	POWER	I
B17	VSS	GND	I
B18	VCCCORE	POWER	I
B19	VCCCORE	POWER	I
B2	VSS	GND	I
B20	VSS	GND	I
B21	VCCCORE	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 13 of 39)

Land #	Socket (EMTS)	Format	IO
B22	VCCCORE	POWER	I
B23	VSS	GND	I
B24	VSS	GND	I
B25	VCCCORE	POWER	I
B26	VCCCORE	POWER	I
B27	VSS	GND	I
B28	VCCCORE	POWER	I
B29	VCCCORE	POWER	I
B3	VSS	GND	I
B30	VSS	GND	I
B31	VCCCORE	POWER	I
B32	VCCCORE	POWER	I
B33	VSS	GND	I
B34	VCCCORE	POWER	I
B35	VCCCORE	POWER	I
B36	VSS	GND	I
B37	VCCCORE	POWER	I
B38	VCCCORE	POWER	I
B39	VSS	GND	I
B4	RESET_N	GTL	I
B40	VSS	GND	I
B41	QPI3_DTX_DP[14]	SCID Diff.	O
B42	QPI3_DTX_DN[13]	SCID Diff.	O
B43	QPI3_DTX_DP[11]	SCID Diff.	O
B44	QPI3_DTX_DN[11]	SCID Diff.	O
B45	VSS	GND	I
B46	RSVD		IO
B5	ISENSE_DN	GTL	I
B6	VSS	GND	I
B7	VID[6]	CMOS	IO
B8	VSS	GND	I
B9	VCCCORE	POWER	I
BA1	VIOF	POWER	I
BA10	VIOF	POWER	I
BA11	VIOF	POWER	I
BA2	VIOF	POWER	I
BA3	VIOF	POWER	I
BA36	VIOC	POWER	I
BA37	QPI1_DRX_DP[17]	SCID Diff.	I
BA38	QPI1_DRX_DN[17]	SCID Diff.	I
BA39	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 14 of 39)

Land #	Socket (EMTS)	Format	IO
BA4	VSS	GND	I
BA40	QPI0_DRX_DN[2]	SCID Diff.	I
BA41	QPI0_DRX_DP[1]	SCID Diff.	I
BA42	VIOC	POWER	I
BA43	QPI1_DTX_DN[17]	SCID Diff.	O
BA44	QPI1_DTX_DN[10]	SCID Diff.	O
BA45	QPI1_DTX_DP[10]	SCID Diff.	O
BA46	QPI1_DTX_DN[11]	SCID Diff.	O
BA5	FBD0SBOAN[0]	Differential	O
BA6	FBD0SBOAP[0]	Differential	O
BA7	VIOF	POWER	I
BA8	VIOF	POWER	I
BA9	VSS	GND	I
BB10	VIOF	POWER	I
BB11	VIOF	POWER	I
BB2	VIOF	POWER	I
BB3	VSS	GND	I
BB36	VSS	GND	I
BB37	VIOC	POWER	I
BB38	QPI0_DRX_DN[0]	SCID Diff.	I
BB39	QPI0_DRX_DP[0]	SCID Diff.	I
BB4	VIOF	POWER	I
BB40	QPI0_DRX_DP[2]	SCID Diff.	I
BB41	VSS	GND	I
BB42	VIOC	POWER	I
BB43	QPI1_DTX_DP[12]	SCID Diff.	O
BB44	QPI1_DTX_DN[12]	SCID Diff.	O
BB45	VSS	GND	I
BB46	QPI1_DTX_DP[11]	SCID Diff.	O
BB5	VIOF	POWER	I
BB6	VIOF	POWER	I
BB7	VSS	GND	I
BB8	VIOF	POWER	I
BB9	VSS	GND	I
BC10	MEM_THROTTLE0_N	GTL	I
BC11	VSS	GND	I
BC12	VSS	GND	I
BC13	VSS	GND	I
BC14	VSS	GND	I
BC15	VCACHE	Power	I
BC16	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 15 of 39)

Land #	Socket (EMTS)	Format	IO
BC17	VCACHE	Power	I
BC18	VCACHE	Power	I
BC19	VSS	GND	I
BC2	FBD0NBIBP[11]	Differential	I
BC20	VCACHE	POWER	I
BC21	VCACHE	POWER	I
BC22	VSS	GND	I
BC23	VCACHE	POWER	I
BC24	VCACHE	POWER	I
BC25	VSS	GND	I
BC26	VCACHE	POWER	I
BC27	VCACHE	POWER	I
BC28	VSS	GND	I
BC29	VCACHE	POWER	I
BC3	FBD0NBIBN[11]	Differential	I
BC30	VCACHE	POWER	I
BC31	VSS	GND	I
BC32	VCACHE	POWER	I
BC33	VCACHE	POWER	I
BC34	VSS	GND	I
BC35	RSVD		IO
BC36	QPI0_DRX_DN[6]	SCID Diff.	I
BC37	VSS	GND	I
BC38	RSVD		IO
BC39	QPI0_DRX_DN[3]	SCID Diff.	I
BC4	FBD0NBIBN[10]	Differential	I
BC40	QPI0_DRX_DP[3]	SCID Diff.	I
BC41	QPI0_DRX_DN[4]	SCID Diff.	I
BC42	VSS	GND	I
BC43	QPI1_DTX_DN[15]	SCID Diff.	O
BC44	QPI1_DTX_DP[13]	SCID Diff.	O
BC45	QPI1_DTX_DN[13]	SCID Diff.	O
BC5	VSS	GND	I
BC6	FBD0NBIAN[10]	Differential	I
BC7	FBD0NBIAP[11]	Differential	I
BC8	FBD0NBIAN[11]	Differential	I
BC9	RSVD		IO
BD10	MEM_THROTTLE1_N	GTL	I
BD11	VSS	GND	I
BD12	RSVD		IO
BD13	RSVD		IO

Table 4-2. Pin List, Sorted by land Number (Sheet 16 of 39)

Land #	Socket (EMTS)	Format	IO
BD14	VSS	GND	I
BD15	VCACHE	POWER	I
BD16	VSS	GND	I
BD17	VCACHE	POWER	I
BD18	VCACHE	POWER	I
BD19	VSS	GND	I
BD2	FBD0NBIBN[9]	Differential	I
BD20	VCACHE	POWER	I
BD21	VCACHE	POWER	I
BD22	VSS	GND	I
BD23	VCACHE	POWER	I
BD24	VCACHE	POWER	I
BD25	VSS	GND	I
BD26	VCACHE	POWER	I
BD27	VCACHE	POWER	I
BD28	VSS	GND	I
BD29	VCACHE	POWER	I
BD3	VSS	GND	I
BD30	VCACHE	POWER	I
BD31	VSS	GND	I
BD32	VCACHE	POWER	I
BD33	VCACHE	POWER	I
BD34	QPI0_DRX_DN[19]	SCID Diff.	I
BD35	QPI0_DRX_DP[19]	SCID Diff.	I
BD36	QPI0_DRX_DP[6]	SCID Diff.	I
BD37	QPI0_DRX_DN[9]	SCID Diff.	I
BD38	RSVD		IO
BD39	VSS	GND	I
BD4	FBD0NBIBP[10]	Differential	I
BD40	QPI0_DRX_DN[5]	SCID Diff.	I
BD41	QPI0_DRX_DP[4]	SCID Diff.	I
BD42	VIOC	POWER	I
BD43	QPI1_DTX_DP[15]	SCID Diff.	O
BD44	VSS	GND	I
BD45	QPI1_DTX_DN[14]	SCID Diff.	O
BD5	FBD0NBIAN[9]	Differential	I
BD6	FBD0NBIAP[10]	Differential	I
BD7	VSS	GND	I
BD8	FBD0NBIAP[0]	Differential	I
BD9	RSVD		IO
BE1	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 17 of 39)

Land #	Socket (EMTS)	Format	IO
BE10	VCC33	POWER	I
BE11	VCC33	POWER	I
BE12	VCC33	POWER	I
BE13	VSS	GND	I
BE14	VSS	GND	I
BE15	VCACHE	POWER	I
BE16	VSS	GND	I
BE17	VCACHE	POWER	I
BE18	VCACHE	POWER	I
BE19	VSS	GND	I
BE2	FBD0NBIBP[9]	Differential	I
BE20	VCACHE	POWER	I
BE21	VCACHE	POWER	I
BE22	VSS	GND	I
BE23	VCACHE	POWER	I
BE24	VCACHE	POWER	I
BE25	VSS	GND	I
BE26	VCACHE	POWER	I
BE27	VCACHE	POWER	I
BE28	VSS	GND	I
BE29	VCACHE	POWER	I
BE3	FBD0NBIBN[8]	Differential	I
BE30	VCACHE	POWER	I
BE31	VSS	GND	I
BE32	QPI0_DRX_DP[17]	SCID Diff.	I
BE33	QPI0_DRX_DN[18]	SCID Diff.	I
BE34	QPI0_DRX_DP[18]	SCID Diff.	I
BE35	QPI0_DRX_DN[10]	SCID Diff.	I
BE36	VSS	GND	I
BE37	QPI0_DRX_DP[9]	SCID Diff.	I
BE38	QPI0_DRX_DP[8]	SCID Diff.	I
BE39	QPI0_DRX_DN[8]	SCID Diff.	I
BE4	FBD0NBIBP[8]	Differential	I
BE40	QPI0_DRX_DP[5]	SCID Diff.	I
BE41	VSS	GND	I
BE42	VIOC	POWER	I
BE43	QPI1_DTX_DP[16]	SCID Diff.	O
BE44	QPI1_DTX_DN[16]	SCID Diff.	O
BE45	QPI1_DTX_DP[14]	SCID Diff.	O
BE46	VSS	GND	I
BE5	FBD0NBIAP[9]	Differential	I

Table 4-2. Pin List, Sorted by land Number (Sheet 18 of 39)

Land #	Socket (EMTS)	Format	IO
BE6	FBD0NBIAN[8]	Differential	I
BE7	FBD0NBIAP[8]	Differential	I
BE8	FBD0NBIAN[0]	Differential	I
BE9	VSS	GND	I
BF1	FBD0NBIBN[7]	Differential	I
BF10	LT-SX (Test-Lo)	GTL	I
BF11	VSS	GND	I
BF12	RSVD		IO
BF13	VSS	GND	I
BF14	PSI_CACHE_N	CMOS	O
BF15	VCACHE	POWER	I
BF16	VSS	GND	I
BF17	VCACHE	POWER	I
BF18	VCACHE	POWER	I
BF19	VSS	GND	I
BF2	FBD0NBIBP[7]	Differential	I
BF20	VCACHE	POWER	I
BF27	VCACHE	POWER	I
BF28	VSS	GND	I
BF29	VCACHE	POWER	I
BF3	RSVD		IO
BF30	VCACHE	POWER	I
BF31	VSS	GND	I
BF32	QPI0_DRX_DN[17]	SCID Diff.	I
BF33	QPI0_DRX_DP[16]	SCID Diff.	I
BF34	VSS	GND	I
BF35	QPI0_DRX_DP[10]	SCID Diff.	I
BF36	QPI0_CLKRX_DP	SCID Diff.	I
BF37	QPI0_CLKRX_DN	SCID Diff.	I
BF38	VSS	GND	I
BF39	QPI0_DRX_DP[7]	SCID Diff.	I
BF4	FBD0NBIBP[0]	Differential	I
BF40	QPI0_DRX_DN[7]	SCID Diff.	I
BF41	VIOC	POWER	I
BF42	VSS	GND	I
BF43	QPI0_DTX_DN[1]	SCID Diff.	O
BF44	QPI0_DTX_DN[2]	SCID Diff.	O
BF45	QPI0_DTX_DP[2]	SCID Diff.	O
BF46	QPI0_DTX_DN[3]	SCID Diff.	O
BF5	VSS	GND	I
BF6	FBD0NBIAN[7]	Differential	I

Table 4-2. Pin List, Sorted by land Number (Sheet 19 of 39)

Land #	Socket (EMTS)	Format	IO
BF7	VSS	GND	I
BF8	FBD0NBIAN[1]	Differential	I
BF9	FBD0NBIAP[1]	Differential	I
BG1	FBD0NBIBN[6]	Differential	I
BG10	SPDCLK	CMOS	I/OD
BG11	SKTDIS_N	GTL	I
BG12	VSS	GND	I
BG13	THERMALERT_N	CMOS	OD
BG14	VSS	GND	I
BG15	VCACHE	POWER	I
BG16	VSS	GND	I
BG17	VCACHE	POWER	I
BG18	VCACHE	POWER	I
BG19	VSS	GND	I
BG2	RSVD		IO
BG20	VCACHE	POWER	I
BG27	VCACHE	POWER	I
BG28	VSS	GND	I
BG29	VCACHE	POWER	I
BG3	VSS	GND	I
BG30	VCACHE	POWER	I
BG31	VSS	GND	I
BG32	RSVD		IO
BG33	QPI0_DRX_DN[16]	SCID Diff.	I
BG34	QPI0_DRX_DP[11]	SCID Diff.	I
BG35	QPI0_DRX_DN[11]	SCID Diff.	I
BG36	VIOC	POWER	I
BG37	VIOC	POWER	I
BG38	VIOC	POWER	I
BG39	VIOC	POWER	I
BG4	FBD0NBIBN[0]	Differential	I
BG40	VSS	GND	I
BG41	VIOC	POWER	I
BG42	QPI0_DTX_DN[0]	SCID Diff.	O
BG43	QPI0_DTX_DP[1]	SCID Diff.	O
BG44	VSS	GND	I
BG45	RSVD		IO
BG46	QPI0_DTX_DP[3]	SCID Diff.	O
BG5	FBD0NBIAN[6]	Differential	I
BG6	FBD0NBIAP[7]	Differential	I
BG7	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 20 of 39)

Land #	Socket (EMTS)	Format	IO
BG8	FBD0NBIAP[2]	Differential	I
BG9	SPDDAT	CMOS	I/OD
BH1	FBD0NBIBP[6]	Differential	I
BH10	BOOTMODE[0]	GTL	I
BH11	BOOTMODE[1]	GTL	I
BH12	SMBDAT	CMOS	I/OD
BH13	VSS	GND	I
BH14	SKTID[2]	CMOS	I
BH15	RSVD		IO
BH16	RSVD		IO
BH17	VCACHE	POWER	I
BH18	VCACHE	POWER	I
BH19	VSS	GND	I
BH2	FBD0NBIBN[12]	Differential	I
BH20	VCACHE	POWER	I
BH27	VCACHE	POWER	I
BH28	VSS	GND	I
BH29	VCACHE	POWER	I
BH3	FBD0NBICLKBN0	Differential	I
BH30	VCACHE	POWER	I
BH31	VSS	GND	I
BH32	QPI0_DRX_DP[15]	SCID Diff.	I
BH33	QPI0_DRX_DN[15]	SCID Diff.	I
BH34	VIOC	POWER	I
BH35	VIOC	POWER	I
BH36	VSS	GND	I
BH37	QPI0_DTX_DP[18]	SCID Diff.	O
BH38	VIO_VID[1]	CMOS	O
BH39	QPI0_DTX_DN[19]	SCID Diff.	O
BH4	FBD0NBICLKBP0	Differential	I
BH40	QPI0_DTX_DP[19]	SCID Diff.	O
BH41	VIOC	POWER	I
BH42	QPI0_DTX_DP[0]	SCID Diff.	O
BH43	QPI0_DTX_DN[4]	SCID Diff.	O
BH44	QPI0_DTX_DP[4]	SCID Diff.	O
BH45	QPI0_DTX_DN[5]	SCID Diff.	O
BH46	VSS	GND	I
BH5	FBD0NBIAP[6]	Differential	I
BH6	FBD0NBIAN[12]	Differential	I
BH7	FBD0NBIAP[12]	Differential	I
BH8	FBD0NBIAN[2]	Differential	I

Table 4-2. Pin List, Sorted by land Number (Sheet 21 of 39)

Land #	Socket (EMTS)	Format	IO
BH9	VSS	GND	I
BJ1	VSS	GND	I
BJ10	RUNBIST	GTL	I
BJ11	VSS	GND	I
BJ12	SMBCLK	CMOS	I/OD
BJ13	SKTOCC_N		O
BJ14	SKTID[1]	CMOS	I
BJ15	FLASHROM_CFG[2]	GTL	I
BJ16	CVID[3]	CMOS	O
BJ17	VSS	GND	I
BJ18	VCACHE	POWER	I
BJ19	VSS	GND	I
BJ2	FBD0NBIBP[12]	Differential	I
BJ20	VCACHE	POWER	I
BJ21	VCACHE	POWER	I
BJ22	VSS	GND	I
BJ23	VCACHE	POWER	I
BJ24	VCACHE	POWER	I
BJ25	VSS	GND	I
BJ26	VCACHE	POWER	I
BJ27	VCACHE	POWER	I
BJ28	VSS	GND	I
BJ29	VCACHE	POWER	I
BJ3	VSS	GND	I
BJ30	VCACHE	POWER	I
BJ31	VSS	GND	I
BJ32	VSS	GND	I
BJ33	QPI0_DRX_DN[12]	SCID Diff.	I
BJ34	VSS	GND	I
BJ35	QPI0_DTX_DP[17]	SCID Diff.	O
BJ36	QPI0_DTX_DN[17]	SCID Diff.	O
BJ37	QPI0_DTX_DN[18]	SCID Diff.	O
BJ38	VSS	GND	I
BJ39	QPI0_DTX_DP[12]	SCID Diff.	O
BJ4	FBD0NBIBN[5]	Differential	I
BJ40	QPI0_DTX_DP[10]	SCID Diff.	O
BJ41	QPI0_DTX_DN[10]	SCID Diff.	O
BJ42	VSS	GND	I
BJ43	QPI0_DTX_DN[6]	SCID Diff.	O
BJ44	VSS	GND	I
BJ45	QPI0_DTX_DP[5]	SCID Diff.	O

Table 4-2. Pin List, Sorted by land Number (Sheet 22 of 39)

Land #	Socket (EMTS)	Format	IO
BJ46	VSS	GND	I
BJ5	VSS	GND	I
BJ6	FBD0NBIBP[1]	Differential	I
BJ7	VSS	GND	I
BJ8	FBD0NBICLKAN0	Differential	I
BJ9	FBD0NBICLKAP0	Differential	I
BK1	VSS	GND	I
BK10	FBD0NBIAP[5]	Differential	I
BK11	FLASHROM_WP_N	GTL	OD
BK12	SM_WP	CMOS	I
BK13	FLASHROM_CS_N[0]	GTL	OD
BK14	SKTID[0]	CMOS	I
BK15	VSS	GND	I
BK16	CVID[2]	CMOS	O
BK17	VSSCACHESENSE	POWER	IO
BK18	VCACHESENSE	POWER	IO
BK19	VSS	GND	I
BK2	FBD0NBIBN[13]	Differential	I
BK20	VCACHE	POWER	I
BK21	VCACHE	POWER	I
BK22	VSS	GND	I
BK23	VCACHE	POWER	I
BK24	VCACHE	POWER	I
BK25	VSS	GND	I
BK26	VCACHE	POWER	I
BK27	VCACHE	POWER	I
BK28	VSS	GND	I
BK29	VCACHE	POWER	I
BK3	FBD0NBIBP[13]	Differential	I
BK30	VCACHE	POWER	I
BK31	VSS	GND	I
BK32	QPI0_DRX_DP[14]	SCID Diff.	I
BK33	QPI0_DRX_DP[12]	SCID Diff.	I
BK34	VIOC	POWER	I
BK35	QPI0_DTX_DP[16]	SCID Diff.	O
BK36	QPI0_DTX_DP[14]	SCID Diff.	O
BK37	QPI0_DTX_DN[14]	SCID Diff.	O
BK38	VIO_VID[2]	CMOS	O
BK39	QPI0_DTX_DN[12]	SCID Diff.	O
BK4	FBD0NBIBP[5]	Differential	I
BK40	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 23 of 39)

Land #	Socket (EMTS)	Format	IO
BK41	QPI0_DTX_DP[8]	SCID Diff.	O
BK42	QPI0_DTX_DN[8]	SCID Diff.	O
BK43	QPI0_DTX_DP[6]	SCID Diff.	O
BK44	QPI0_DTX_DP[7]	SCID Diff.	O
BK45	QPI0_DTX_DN[7]	SCID Diff.	O
BK46	VSS	GND	I
BK5	FBD0NBIBN[4]	Differential	I
BK6	FBD0NBIBN[1]	Differential	I
BK7	VSS	GND	I
BK8	FBD0NBIAN[13]	Differential	I
BK9	FBD0NBIAN[5]	Differential	I
BL1	VSS	GND	I
BL10	FBD0NBIAN[3]	Differential	I
BL11	FLASHROM_CLK	GTL	OD
BL12	FLASHROM_DATI	GTL	I
BL13	VSS	GND	I
BL14	FLASHROM_CS_N[2]	GTL	OD
BL15	FLASHROM_CFG[0]	GTL	I
BL16	CVID[1]	CMOS	O
BL17	CVID[5]	CMOS	O
BL18	CVID[7]	CMOS	O
BL19	VSS	GND	I
BL2	VSS	GND	I
BL20	VCACHE	POWER	I
BL21	VCACHE	POWER	I
BL22	VSS	GND	I
BL23	VCACHE	POWER	I
BL24	VCACHE	POWER	I
BL25	VSS	GND	I
BL26	VCACHE	POWER	I
BL27	VCACHE	POWER	I
BL28	VSS	GND	I
BL29	VCACHE	POWER	I
BL3	VSS	GND	I
BL30	VCACHE	POWER	I
BL31	VSS	GND	I
BL32	QPI0_DRX_DN[14]	SCID Diff.	I
BL33	VSS	GND	I
BL34	VIOC	POWER	I
BL35	QPI0_DTX_DN[16]	SCID Diff.	O
BL36	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 24 of 39)

Land #	Socket (EMTS)	Format	IO
BL37	QPI0_DTX_DN[13]	SCID Diff.	O
BL38	VSS	GND	I
BL39	QPI0_DTX_DP[11]	SCID Diff.	O
BL4	VSS	GND	I
BL40	QPI0_DTX_DN[11]	SCID Diff.	O
BL41	QPI0_CLKTX_DN	SCID Diff.	O
BL42	QPI0_DTX_DP[9]	SCID Diff.	O
BL43	QPI0_DTX_DN[9]	SCID Diff.	O
BL44	VSS	GND	I
BL45	VSS	GND	I
BL46	VSS	GND	I
BL5	FBD0NBIBP[4]	Differential	I
BL6	FBD0NBIBN[2]	Differential	I
BL7	FBD0NBIBP[2]	Differential	I
BL8	FBD0NBIAP[13]	Differential	I
BL9	VSS	GND	I
BM1	TEST[3]	GND	IO
BM10	FBD0NBIAP[3]	Differential	I
BM11	VSS	GND	I
BM12	FLASHROM_DATO	GTL	OD
BM13	FLASHROM_CS_N[1]	GTL	OD
BM14	FLASHROM_CS_N[3]	GTL	OD
BM15	FLASHROM_CFG[1]	GTL	I
BM16	VSS	GND	I
BM17	CVID[4]	CMOS	O
BM18	CVID[6]	CMOS	O
BM19	VSS	GND	I
BM2	VSS	GND	I
BM20	VCACHE	POWER	I
BM21	VCACHE	POWER	I
BM26	VCACHE	POWER	I
BM27	VCACHE	POWER	I
BM28	VSS	GND	I
BM29	VCACHE	POWER	I
BM3	VSS	GND	I
BM30	VCACHE	POWER	I
BM31	VSS	GND	I
BM32	QPI0_DRX_DP[13]	SCID Diff.	I
BM33	QPI0_DRX_DN[13]	SCID Diff.	I
BM34	VSS	GND	I
BM35	QPI0_DTX_DP[15]	SCID Diff.	O

Table 4-2. Pin List, Sorted by land Number (Sheet 25 of 39)

Land #	Socket (EMTS)	Format	IO
BM36	QPI0_DTX_DN[15]	SCID Diff.	O
BM37	QPI0_DTX_DP[13]	SCID Diff.	O
BM38	VIO_VID[3]	CMOS	O
BM39	VIO_VID[4]	CMOS	O
BM4	VSS	GND	I
BM40	VSS	GND	I
BM41	QPI0_CLKTX_DP	SCID Diff.	O
BM42	VSS	GND	I
BM43	VSS	GND	I
BM44	VSS	GND	I
BM45	VSS	GND	I
BM46	TEST[2]	GND	I
BM5	FBD0NBIBN[3]	Differential	I
BM6	FBD0NBIBP[3]	Differential	I
BM7	VSS	GND	I
BM8	FBD0NBIAN[4]	Differential	I
BM9	FBD0NBIAP[4]	Differential	I
C1	VSS	GND	I
C10	VCCCORE	POWER	I
C11	VSS	GND	I
C12	VCCCORE	POWER	I
C13	VCCCORE	POWER	I
C14	VSS	GND	I
C15	VCCCORE	POWER	I
C16	VCCCORE	POWER	I
C17	VSS	GND	I
C18	VCCCORE	POWER	I
C19	VCCCORE	POWER	I
C2	VSS	GND	I
C20	VSS	GND	I
C21	VCCCORE	POWER	I
C22	VCCCORE	POWER	I
C23	VSS	GND	I
C24	VSS	GND	I
C25	VCCCORE	POWER	I
C26	VCCCORE	POWER	I
C27	VSS	GND	I
C28	VCCCORE	POWER	I
C29	VCCCORE	POWER	I
C3	PRDY_N	CMOS	O
C30	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 26 of 39)

Land #	Socket (EMTS)	Format	IO
C31	VCCCORE	POWER	I
C32	VCCCORE	POWER	I
C33	VSS	GND	I
C34	VCCCORE	POWER	I
C35	VCCCORE	POWER	I
C36	VSS	GND	I
C37	VCCCORE	POWER	I
C38	VCCCORE	POWER	I
C39	QPI3_DTX_DN[16]	SCID Diff.	O
C4	FORCE_PR_N	GTL	I
C40	QPI3_DTX_DP[16]	SCID Diff.	O
C41	VSS	GND	I
C42	QPI3_DTX_DP[13]	SCID Diff.	O
C43	VSS	GND	I
C44	QPI3_DTX_DP[10]	SCID Diff.	O
C45	QPI3_DTX_DN[10]	SCID Diff.	O
C46	RSVD		IO
C5	VSS	GND	I
C6	VID[5]	CMOS	IO
C7	VID[4]	CMOS	IO
C8	VSS	GND	I
C9	VCCCORE	POWER	I
D1	VSS	GND	I
D10	VCCCORE	POWER	I
D11	VSS	GND	I
D12	VCCCORE	POWER	I
D13	VCCCORE	POWER	I
D14	VSS	GND	I
D15	VCCCORE	POWER	I
D16	VCCCORE	POWER	I
D17	VSS	GND	I
D18	VCCCORE	POWER	I
D19	VCCCORE	POWER	I
D2	PROCHOT_N	GTL	OD
D20	VSS	GND	I
D21	VCCCORE	POWER	I
D22	VCCCORE	POWER	I
D23	VSS	GND	I
D24	VSS	GND	I
D25	VCCCORE	POWER	I
D26	VCCCORE	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 27 of 39)

Land #	Socket (EMTS)	Format	IO
D27	VSS	GND	I
D28	VCCCORE	POWER	I
D29	VCCCORE	POWER	I
D3	PREQ_N	CMOS	I
D30	VSS	GND	I
D31	VCCCORE	POWER	I
D32	VCCCORE	POWER	I
D33	VSS	GND	I
D34	VCCCORE	POWER	I
D35	VCCCORE	POWER	I
D36	VSS	GND	I
D37	VCCCORE	POWER	I
D38	VCCCORE	POWER	I
D39	VSS	GND	I
D4	RSVD		IO
D40	QPI3_DTX_DP[19]	SCID Diff.	O
D41	QPI3_DTX_DP[15]	SCID Diff.	O
D42	QPI3_DTX_DN[15]	SCID Diff.	O
D43	PECI	CMOS	IO
D44	QPI3_CLKTX_DP	SCID Diff.	O
D45	VSS	GND	I
D46	VSS	GND	I
D5	NMI	GTL	I
D6	VID[3]	CMOS	IO
D7	VID[2]	CMOS	IO
D8	VSS	GND	I
D9	VCCCORE	POWER	I
E1	MBP[6]_N	GTL	IO
E10	VCCCORE	POWER	I
E11	VSS	GND	I
E12	VCCCORE	POWER	I
E13	VCCCORE	POWER	I
E14	VSS	GND	I
E15	VCCCORE	POWER	I
E16	VCCCORE	POWER	I
E17	VSS	GND	I
E18	VCCCORE	POWER	I
E19	VCCCORE	POWER	I
E2	MBP[3]_N	GTL	IO
E20	VSS	GND	I
E27	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 28 of 39)

Land #	Socket (EMTS)	Format	IO
E28	VCCCORE	POWER	I
E29	VCCCORE	POWER	I
E3	MBP[5]_N	GTL	IO
E30	VSS	GND	I
E31	VCCCORE	POWER	I
E32	VCCCORE	POWER	I
E33	VSS	GND	I
E34	VCCCORE	POWER	I
E35	VCCCORE	POWER	I
E36	VSS	GND	I
E37	VCCCORE	POWER	I
E38	VCCCORE	POWER	I
E39	QPI3_DTX_DN[18]	SCID Diff.	O
E4	MBP[7]_N	GTL	IO
E40	QPI3_DTX_DN[19]	SCID Diff.	O
E41	VSS	GND	I
E42	QPI3_DTX_DP[12]	SCID Diff.	O
E43	VSS	GND	I
E44	QPI3_CLKTX_DN	SCID Diff.	O
E45	QPI3_DTX_DN[9]	SCID Diff.	O
E46	QPI3_DTX_DP[9]	SCID Diff.	O
E5	VSS	GND	I
E6	VID[1]	CMOS	IO
E7	VID[0]	CMOS	IO
E8	VSS	GND	I
E9	VCCCORE	POWER	I
F1	MBP[2]_N	GTL	IO
F10	VCCCORE	POWER	I
F11	VSS	GND	I
F12	VCCCORE	POWER	I
F13	VCCCORE	POWER	I
F14	VSS	GND	I
F15	VCCCORE	POWER	I
F16	VCCCORE	POWER	I
F17	VSS	GND	I
F18	VCCCORE	POWER	I
F19	VCCCORE	POWER	I
F2	MBP[1]_N	GTL	IO
F20	VSS	GND	I
F27	VSS	GND	I
F28	VCCCORE	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 29 of 39)

Land #	Socket (EMTS)	Format	IO
F29	VCCCORE	POWER	I
F3	VSS	GND	I
F30	VSS	GND	I
F31	VCCCORE	POWER	I
F32	VCCCORE	POWER	I
F33	VSS	GND	I
F34	VCCCORE	POWER	I
F35	VCCCORE	POWER	I
F36	VSS	GND	I
F37	VCCCORE	POWER	I
F38	VCCCORE	POWER	I
F39	QPI3_DTX_DP[18]	SCID Diff.	O
F4	MBP[4]_N	GTL	IO
F40	QPI3_DTX_DP[17]	SCID Diff.	O
F41	QPI3_DTX_DN[17]	SCID Diff.	O
F42	QPI3_DTX_DN[12]	SCID Diff.	O
F43	QPI3_DTX_DN[4]	SCID Diff.	O
F44	QPI3_DTX_DP[4]	SCID Diff.	O
F45	VSS	GND	I
F46	QPI3_DTX_DP[8]	SCID Diff.	O
F5	THERMTRIP_N	GTL-OD	O
F6	VSSCORESENSE	POWER	IO
F7	VCORESENSE	POWER	IO
F8	VSS	GND	I
F9	VCCCORE	POWER	I
G1	VSS	GND	I
G10	VCCCORE	POWER	I
G11	VSS	GND	I
G12	VCCCORE	POWER	I
G13	VCCCORE	POWER	I
G14	VSS	GND	I
G15	VCCCORE	POWER	I
G16	VCCCORE	POWER	I
G17	VSS	GND	I
G18	VCCCORE	POWER	I
G19	VCCCORE	POWER	I
G2	MBP[0]_N	GTL	IO
G20	VSS	GND	I
G27	VSS	GND	I
G28	VCCCORE	POWER	I
G29	VCCCORE	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 30 of 39)

Land #	Socket (EMTS)	Format	IO
G3	ERROR0_N	GTL OD	IO
G30	VSS	GND	I
G31	VCCCORE	POWER	I
G32	VCCCORE	POWER	I
G33	VSS	GND	I
G34	VCCCORE	POWER	I
G35	VCCCORE	POWER	I
G36	VSS	GND	I
G37	VCCCORE	POWER	I
G38	VCCCORE	POWER	I
G39	VSS	GND	I
G4	ERROR1_N	GTL-OD	IO
G40	VSS	GND	I
G41	PWRGOOD	CMOS	I
G42	VSS	GND	I
G43	QPI3_DTX_DN[2]	SCID Diff.	O
G44	QPI3_DTX_DN[7]	SCID Diff.	O
G45	QPI3_DTX_DP[7]	SCID Diff.	O
G46	QPI3_DTX_DN[8]	SCID Diff.	O
G5	VSS	GND	I
G6	RSVD		IO
G7	PSI_N	CMOS	O
G8	VSS	GND	I
G9	VCCCORE	POWER	I
H1	FBD1SBODP[5]	Differential	O
H10	VCCCORE	POWER	I
H11	VSS	GND	I
H12	VCCCORE	POWER	I
H13	VCCCORE	POWER	I
H14	VSS	GND	I
H15	VCCCORE	POWER	I
H16	VCCCORE	POWER	I
H17	VSS	GND	I
H18	VCCCORE	POWER	I
H19	VCCCORE	POWER	I
H2	FBD1SBODN[5]	Differential	O
H20	VSS	GND	I
H21	VCCCORE	POWER	I
H22	VCCCORE	POWER	I
H23	VSS	GND	I
H24	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 31 of 39)

Land #	Socket (EMTS)	Format	IO
H25	VCCCORE	POWER	I
H26	VCCCORE	POWER	I
H27	VSS	GND	I
H28	VCCCORE	POWER	I
H29	VCCCORE	POWER	I
H3	FBD1SBODN[9]	Differential	O
H30	VSS	GND	I
H31	VCCCORE	POWER	I
H32	VCCCORE	POWER	I
H33	VSS	GND	I
H34	VCCCORE	POWER	I
H35	VCCCORE	POWER	I
H36	VSS	GND	I
H37	VCCCORE	POWER	I
H38	VCCCORE	POWER	I
H39	VSS	GND	I
H4	VSS	GND	I
H40	VSS	GND	I
H41	VIOPWRGOOD	CMOS	I
H42	QPI3_DTX_DN[1]	SCID Diff.	O
H43	QPI3_DTX_DP[2]	SCID Diff.	O
H44	VSS	GND	I
H45	QPI3_DTX_DP[6]	SCID Diff.	O
H46	VSS	GND	I
H5	FBD1SBOCN[9]	Differential	O
H6	FBD1SBOCP[5]	Differential	O
H7	FBD1SBOCN[5]	Differential	O
H8	VSS	GND	I
H9	RSVD		IO
J1	FBD1SBOCLKDP0	Differential	O
J10	VCCCORE	POWER	I
J11	VSS	GND	I
J12	VCCCORE	POWER	I
J13	VCCCORE	POWER	I
J14	VSS	GND	I
J15	VCCCORE	POWER	I
J16	VCCCORE	POWER	I
J17	VSS	GND	I
J18	VCCCORE	POWER	I
J19	VCCCORE	POWER	I
J2	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 32 of 39)

Land #	Socket (EMTS)	Format	IO
J20	VSS	GND	I
J21	VCCCORE	POWER	I
J22	VCCCORE	POWER	I
J23	VSS	GND	I
J24	VSS	GND	I
J25	VCCCORE	POWER	I
J26	VCCCORE	POWER	I
J27	VSS	GND	I
J28	VCCCORE	POWER	I
J29	VCCCORE	POWER	I
J3	FBD1SBODP[9]	Differential	O
J30	VSS	GND	I
J31	VCCCORE	POWER	I
J32	VCCCORE	POWER	I
J33	VSS	GND	I
J34	VCCCORE	POWER	I
J35	VCCCORE	POWER	I
J36	VSS	GND	I
J37	VCCCORE	POWER	I
J38	VCCCORE	POWER	I
J39	VSS	GND	I
J4	FBD1SBODN[6]	Differential	O
J40	QPI3_DTX_DN[0]	SCID Diff.	O
J41	QPI3_DTX_DP[0]	SCID Diff.	O
J42	QPI3_DTX_DP[1]	SCID Diff.	O
J43	QPI3_DTX_DN[3]	SCID Diff.	O
J44	QPI3_DTX_DP[3]	SCID Diff.	O
J45	QPI3_DTX_DN[6]	SCID Diff.	O
J46	QPI3_DTX_DP[5]	SCID Diff.	O
J5	FBD1SBOCP[9]	Differential	O
J6	FBD1SBOCLKCP0	Differential	O
J7	VSS	GND	I
J8	FBD1SBOCN[6]	Differential	O
J9	RSVD		IO
K1	FBD1SBOCLKDN0	Differential	O
K10	TCLK	GTL	I
K11	VSS	GND	I
K12	VCCCORE	POWER	I
K13	VCCCORE	POWER	I
K14	VSS	GND	I
K15	VCCCORE	POWER	I

Table 4-2. Pin List, Sorted by land Number (Sheet 33 of 39)

Land #	Socket (EMTS)	Format	IO
K16	VCCCORE	POWER	I
K17	VSS	GND	I
K18	VCCCORE	POWER	I
K19	VCCCORE	POWER	I
K2	FBD1SBODN[4]	Differential	O
K20	VSS	GND	I
K21	VCCCORE	POWER	I
K22	VCCCORE	POWER	I
K23	VSS	GND	I
K24	VSS	GND	I
K25	VCCCORE	POWER	I
K26	VCCCORE	POWER	I
K27	VSS	GND	I
K28	VCCCORE	POWER	I
K29	VCCCORE	POWER	I
K3	FBD1SBODP[4]	Differential	O
K30	VSS	GND	I
K31	VCCCORE	POWER	I
K32	VCCCORE	POWER	I
K33	VSS	GND	I
K34	VCCCORE	POWER	I
K35	VCCCORE	POWER	I
K36	VSS	GND	I
K37	VCCCORE	POWER	I
K38	VCCCORE	POWER	I
K39	VSS	GND	I
K4	FBD1SBODP[6]	Differential	O
K40	VSS	GND	I
K41	VSS	GND	I
K42	VSS	GND	I
K43	VSS	GND	I
K44	VSS	GND	I
K45	VSS	GND	I
K46	QPI3_DTX_DN[5]	SCID Diff.	O
K5	VSS	GND	I
K6	FBD1SBOCLKCN0	Differential	O
K7	VSS	GND	I
K8	FBD1SBOCP[6]	Differential	O
K9	VSS	GND	I
L1	FBD1SBODN[3]	Differential	O
L10	TDO	GTL OD	O

Table 4-2. Pin List, Sorted by land Number (Sheet 34 of 39)

Land #	Socket (EMTS)	Format	IO
L11	VSS	GND	I
L2	FBD1SBODP[3]	Differential	O
L3	VSS	GND	I
L36	VSS	GND	I
L37	VSS	GND	I
L38	QPI3_DRX_DP[16]	SCID Diff.	I
L39	QPI3_DRX_DP[15]	SCID Diff.	I
L4	VSS	GND	I
L40	QPI3_DRX_DN[15]	SCID Diff.	I
L41	QPI3_DRX_DP[13]	SCID Diff.	I
L42	QPI3_DRX_DP[12]	SCID Diff.	I
L43	QPI3_DRX_DN[12]	SCID Diff.	I
L44	QPI3_DRX_DN[11]	SCID Diff.	I
L45	VSS	GND	I
L46	VSS	GND	I
L5	FBD1SBOCN[3]	Differential	O
L6	VSS	GND	I
L7	FBD1SBOCP[4]	Differential	O
L8	FBD1SBOCN[4]	Differential	O
L9	TDI	GTL	I
M1	VSS	GND	I
M10	TRST_N	GTL	I
M11	VSS	GND	I
M2	VSS	GND	I
M3	FBD1SBODP[7]	Differential	O
M36	VIOC	POWER	I
M37	VSS	GND	I
M38	QPI3_DRX_DN[16]	SCID Diff.	I
M39	RSVD		IO
M4	FBD1SBODN[7]	Differential	O
M40	QPI3_DRX_DP[14]	SCID Diff.	I
M41	QPI3_DRX_DN[13]	SCID Diff.	I
M42	VSS	GND	I
M43	QPI3_DRX_DP[10]	SCID Diff.	I
M44	QPI3_DRX_DP[11]	SCID Diff.	I
M45	QPI3_CLKRX_DP	SCID Diff.	I
M46	VSS	GND	I
M5	FBD1SBOCP[3]	Differential	O
M6	FBD1SBOCN[2]	Differential	O
M7	FBD1SBOCP[2]	Differential	O
M8	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 35 of 39)

Land #	Socket (EMTS)	Format	IO
M9	TMS	GTL	I
N1	FBD1SBODN[1]	Differential	O
N10	VSS	GND	I
N11	VSS	GND	I
N2	FBD1SBODP[2]	Differential	O
N3	FBD1SBODN[2]	Differential	O
N36	VSS	GND	I
N37	QPI3_DRX_DP[17]	SCID Diff.	I
N38	QPI3_DRX_DN[17]	SCID Diff.	I
N39	VSS	GND	I
N4	FBD1SBODP[8]	Differential	O
N40	QPI3_DRX_DN[14]	SCID Diff.	I
N41	QPI3_DRX_DN[1]	SCID Diff.	I
N42	QPI3_DRX_DP[1]	SCID Diff.	I
N43	QPI3_DRX_DN[10]	SCID Diff.	I
N44	VSS	GND	I
N45	QPI3_CLKRX_DN	SCID Diff.	I
N46	QPI3_DRX_DP[9]	SCID Diff.	I
N5	VSS	GND	I
N6	FBD1SBOCN[1]	Differential	O
N7	FBD1SBOCP[7]	Differential	O
N8	FBD1SBOCN[7]	Differential	O
N9	VSS	GND	I
P1	FBD1SBODP[1]	Differential	O
P10	VIOF	POWER	I
P11	VIOF	POWER	I
P2	FBD1SBODN[0]	Differential	O
P3	VSS	GND	I
P36	VIOC	POWER	I
P37	RSVD		IO
P38	RSVD		IO
P39	QPI3_DRX_DP[18]	SCID Diff.	I
P4	FBD1SBODN[8]	Differential	O
P40	QPI3_DRX_DN[18]	SCID Diff.	I
P41	QPI3_DRX_DN[0]	SCID Diff.	I
P42	VSS	GND	I
P43	VSS	GND	I
P44	QPI3_DRX_DN[8]	SCID Diff.	I
P45	QPI3_DRX_DP[8]	SCID Diff.	I
P46	QPI3_DRX_DN[9]	SCID Diff.	I
P5	FBD1SBOCN[0]	Differential	O

Table 4-2. Pin List, Sorted by land Number (Sheet 36 of 39)

Land #	Socket (EMTS)	Format	IO
P6	FBD1SBOCP[1]	Differential	O
P7	VSS	GND	I
P8	FBD1SBOCP[10]	Differential	O
P9	RSVD		IO
R1	VSS	GND	I
R10	VIOF	POWER	I
R11	VIOF	POWER	I
R2	FBD1SBODP[0]	Differential	O
R3	FBD1SBODP[10]	Differential	O
R36	VSS	GND	I
R37	VSS	GND	I
R38	QPI3_DRX_DP[19]	SCID Diff.	I
R39	QPI3_DRX_DN[19]	SCID Diff.	I
R4	FBD1SBODN[10]	Differential	O
R40	VSS	GND	I
R41	QPI3_DRX_DP[0]	SCID Diff.	I
R42	QPI3_DRX_DP[2]	SCID Diff.	I
R43	QPI3_DRX_DN[5]	SCID Diff.	I
R44	QPI3_DRX_DP[5]	SCID Diff.	I
R45	QPI3_DRX_DP[7]	SCID Diff.	I
R46	VSS	GND	I
R5	FBD1SBOCP[0]	Differential	O
R6	FBD1SBOCP[8]	Differential	O
R7	FBD1SBOCN[8]	Differential	O
R8	FBD1SBOCN[10]	Differential	O
R9	RSVD		IO
T1	VIOF	POWER	I
T10	VSS	GND	I
T11	VSS	GND	I
T2	VIOF	POWER	I
T3	VSS	GND	I
T36	VSS	GND	I
T37	VSS	GND	I
T38	SYSCLK_DN	Differential	I
T39	QPI2_DRX_DP[15]	SCID Diff.	I
T4	VIOF	POWER	I
T40	QPI2_DRX_DN[15]	SCID Diff.	I
T41	QPI2_DRX_DP[14]	SCID Diff.	I
T42	QPI3_DRX_DN[2]	SCID Diff.	I
T43	QPI3_DRX_DP[3]	SCID Diff.	I
T44	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 37 of 39)

Land #	Socket (EMTS)	Format	IO
T45	QPI3_DRX_DN[7]	SCID Diff.	I
T46	QPI3_DRX_DP[6]	SCID Diff.	I
T5	VSS	GND	I
T6	VIOF	POWER	I
T7	VIOF	POWER	I
T8	VIOF	POWER	I
T9	VSS	GND	I
U1	VIOF	POWER	I
U10	VIOF	POWER	I
U11	VIOF	POWER	I
U2	VSS	GND	I
U3	FBD1NBIDP[10]	Differential	I
U36	VIOC	POWER	I
U37	QPI2_DRX_DP[17]	SCID Diff.	I
U38	SYSCLK_DP	Differential	I
U39	VSS	GND	I
U4	FBD1NBIDN[10]	Differential	I
U40	QPI2_DRX_DP[13]	SCID Diff.	I
U41	QPI2_DRX_DN[14]	SCID Diff.	I
U42	VSS	GND	I
U43	QPI3_DRX_DN[3]	SCID Diff.	I
U44	QPI3_DRX_DN[4]	SCID Diff.	I
U45	QPI3_DRX_DP[4]	SCID Diff.	I
U46	QPI3_DRX_DN[6]	SCID Diff.	I
U5	VIOF	POWER	I
U6	FBD1NBICN[9]	Differential	I
U7	VSS	GND	I
U8	VIOF	POWER	I
U9	VIOF	POWER	I
V1	FBD1NBIDN[8]	Differential	I
V10	VSS	GND	I
V11	VSS	GND	I
V2	FBD1NBIDP[9]	Differential	I
V3	FBD1NBIDN[9]	Differential	I
V36	VSS	GND	I
V37	QPI2_DRX_DN[17]	SCID Diff.	I
V38	QPI2_DRX_DP[16]	SCID Diff.	I
V39	QPI2_DRX_DN[16]	SCID Diff.	I
V4	FBD1NBIDP[11]	Differential	I
V40	QPI2_DRX_DN[13]	SCID Diff.	I
V41	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 38 of 39)

Land #	Socket (EMTS)	Format	IO
V42	VIOC	POWER	I
V43	VIOC	POWER	I
V44	VIOC	POWER	I
V45	VIOC	POWER	I
V46	VSS	GND	I
V5	VSS	GND	I
V6	FBD1NBICP[9]	Differential	I
V7	FBD1NBICP[10]	Differential	I
V8	FBD1NBICN[10]	Differential	I
V9	VSS	GND	I
W1	FBD1NBIDP[8]	Differential	I
W10	VSS	GND	I
W11	VSS	GND	I
W2	FBD1NBIDN[7]	Differential	I
W3	VSS	GND	I
W36	VSS	GND	I
W37	VSS	GND	I
W38	RSVD		IO
W39	QPI2_DRX_DP[12]	SCID Diff.	I
W4	FBD1NBIDN[11]	Differential	I
W40	QPI2_DRX_DN[12]	SCID Diff.	I
W41	QPI2_DRX_DP[11]	SCID Diff.	I
W42	VSS	GND	I
W43	QPI2_DTX_DN[18]	SCID Diff.	O
W44	QPI2_DTX_DP[16]	SCID Diff.	O
W45	QPI2_DTX_DN[16]	SCID Diff.	O
W46	QPI2_DTX_DP[15]	SCID Diff.	O
W5	FBD1NBICN[7]	Differential	I
W6	VSS	GND	I
W7	VSS	GND	I
W8	FBD1NBICP[11]	Differential	I
W9	RSVD		IO
Y1	VSS	GND	I
Y10	RSVD		IO
Y11	VIOF	POWER	I
Y2	FBD1NBIDP[7]	Differential	I
Y3	FBD1NBIDN[6]	Differential	I
Y36	VIOC	POWER	I
Y37	QPI2_DRX_DP[18]	SCID Diff.	I
Y38	QPI2_DRX_DN[18]	SCID Diff.	I
Y39	VSS	GND	I

Table 4-2. Pin List, Sorted by land Number (Sheet 39 of 39)

Land #	Socket (EMTS)	Format	IO
Y4	FBD1NBIDP[6]	Differential	I
Y40	QPI2_DRX_DP[10]	SCID Diff.	I
Y41	QPI2_DRX_DN[11]	SCID Diff.	I
Y42	VIOC	POWER	I
Y43	QPI2_DTX_DP[18]	SCID Diff.	O
Y44	VSS	GND	I
Y45	QPI2_DTX_DP[14]	SCID Diff.	O
Y46	QPI2_DTX_DN[15]	SCID Diff.	O
Y5	FBD1NBICP[7]	Differential	I
Y6	FBD1NBICP[8]	Differential	I
Y7	FBD1NBICN[8]	Differential	I
Y8	FBD1NBICN[11]	Differential	I
Y9	RSVD		IO

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5 Signal Definitions

Table 5-1. Signal Definitions (Sheet 1 of 6)

Name	Type	Description
BOOTMODE[1:0]	I	The BOOTMODE[1:0] inputs are to specify which mode the Intel Xeon Processor E7-8800/4800/2800 Product Families processor will boot to. For details on the modes refer to the *Intel® Xeon® Processor 7500 Series Datasheet, Volume 2*.
CVID[7:1]	O	Voltage ID driven out to the VR 11.1 for dynamic/static adjustment of processor voltage set point. See VCACHE below. This signal has on die termination.
ERROR[0]_N	IO	Pulsed Signal. As output, signals un-corrected error condition of the processor. As an input, can be programmed to signal SMI to the cores. Open drain
ERROR[1]_N	IO	Level Signal. As output, signals fatal error condition of the processor. As an input, can be programmed to signal SMI to the cores. Open drain.
FBD0NBI[A/B][P/N][13:0]	I	These differential pair data signals generated from the branch zero, channel A and B of Intel® SMI links are input to the Intel Xeon Processor E7-8800/4800/2800 Product Families processor. **Intel SMI** | **0** | **NB** | **I** | **A/B** | **P/N** | **[13:0]** Interface Name | Branch Number | North Bound | Input | Channel | Differential Pair Polarity Positive/ Negative | Lane Number Example: FBD0NBIAP[0] Intel SMI branch 0, North bound data input lane 0 signal of channel A and positive bit of the differential pair.
FBD0NBICLK[A/B][P/N]0	I	These differential pair clock signals generated from the branch zero, channel A and B of Intel® SMI links are input to the Intel Xeon Processor E7-8800/4800/2800 Product Families processor. **Intel SMI** | **0** | **NB** | **I** | **CLK** | **A/B** | **P/N** Interface Name | Branch Number | North Bound | Input | Clock | Channel | Differential Pair Polarity Positive/ Negative Example: FBD0NBICLKAP0 Intel SMI branch 0, Northbound clock input signal of channel A and positive bit of the differential pair.
FBD0SBO[A/B][P/N][10:0]	O	These differential pair output data signals generated from Intel Xeon Processor E7-8800/4800/2800 Product Families processor to the branch zero, channel A and B of Intel® SMI links. **Intel SMI** | **0** | **SB** | **O** | **A/B** | **P/N** | **[10:0]** Interface Name | Branch Number | South Bound | Output | Channel | Differential Pair Polarity Positive/ Negative | Lane Number Example: FBD0SBOAP[0] Intel SMI branch 1, southbound data output lane 0 signal of channel A and positive bit of the differential pair.

Table 5-1. Signal Definitions (Sheet 2 of 6)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>FBD0SBOCLK[A/B][P/N]0</td><td>O</td><td>These differential pair output clock signals generated from Intel Xeon Processor E7-8800/4800/2800 Product Families processor are inputs to the branch zero, channel A and B of Intel® SMI links.
<table><tr><th>Intel SMI</th><th>0</th><th>SB</th><th>O</th><th>CLK</th><th>A/B</th><th>P/N</th></tr><tr><td>Interface Name</td><td>Branch Number</td><td>South Bound</td><td>Output</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr></table>
Example: FBD0SBICLKAP0 Intel SMI branch 0, south bound clock output signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD1NBI[C/D][P/N][13:0]</td><td>I</td><td>These differential pair output data signals generated from Intel Xeon Processor E7-8800/4800/2800 Product Families processor are inputs to the branch one, channel C and D of Intel® SMI links.
<table><tr><th>Intel SMI</th><th>1</th><th>NB</th><th>I</th><th>C/D</th><th>P/N</th><th>[13:0]</th></tr><tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr></table>
Example: FBD1NBIAP[0] Intel SMI branch 1, North bound data input lane 0 signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD1NBICLK[C/D][P/N]0</td><td>I</td><td>These differential pair clock signals generated from the branch one, channel C and D of Intel® SMI links are input to the Intel Xeon Processor E7-8800/4800/2800 Product Families processor.
<table><tr><th>Intel SMI</th><th>1</th><th>NB</th><th>I</th><th>CLK</th><th>C/D</th><th>P/N</th></tr><tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Input</td><td>Clock</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td></tr></table>
Example: FBD1NBICLKAP0 Intel SMI branch 1, Northbound clock input signal of channel A and positive bit of the differential pair.</td></tr>
<tr><td>FBD1SBO[C/D][P/N][10:0]</td><td>O</td><td>These differential pair output data signals generated from Intel Xeon Processor E7-8800/4800/2800 Product Families processor to the branch one, channel C and D of Intel® SMI links.
<table><tr><th>Intel SMI</th><th>1</th><th>NB</th><th>O</th><th>C/D</th><th>P/N</th><th>[10:0]</th></tr><tr><td>Interface Name</td><td>Branch Number</td><td>North Bound</td><td>Output</td><td>Channel</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr></table>
Example: FBD1SBOAP[0] Intel SMI branch 1, South bound data Output lane 0 signal of channel A and positive bit of the differential pair.</td></tr>
</table>

Table 5-1. Signal Definitions (Sheet 3 of 6)

Name	Type	Description
FBD1SBOCLK[C/D][P/N]0	O	These differential pair output clock signals generated from Intel Xeon Processor E7-8800/4800/2800 Product Families processor are inputs to the branch one, channel C and D of Intel® SMI links. **Intel SMI** | **1** | **SB** | **O** | **CLK** | **C/D** | **P/N** Interface Name | Branch Number | South Bound | Output | Clock | Channel | Differential Pair Polarity Positive/ Negative Example: FBD1SBICLKAP0 Intel SMI branch 1, south bound clock output signal of channel A and positive bit of the differential pair.
FLASHROM_CFG[2:0]	I	These are input signals to the Intel Xeon Processor E7-8800/4800/2800 Product Families processor that would initialize and map the serial Flash ROM upon reset. After the reset is deasserted this input would be ignored by the processor logic.
FLASHROM_CLK	O	Serial flash ROM clock.
FLASHROM_CS[3:0]_N	O	Serial Flash ROM chip selects. Up to four separate flash ROM parts may be used.
FLASHROM_DATI	I	Serial Data Input (from ROM(s) to processor).
FLASHROM_DATO	O	Serial Data Output (from processor to ROM(s)).
FLASHROM_WP_N	O	Flash ROM write-protect.
FORCE_PR_N	I	Force processor power reduction by activation of a TCC.
ISENSE_D[N/P]	IO	Current sense for Vcore VR11.1
LT-SX (Test-Lo)	I	In platforms supporting the Intel TXT feature, the Intel TXT pin on the processor should be variable setting and driven based on the processor type installed. With Intel Xeon Processor E7-8800/4800/2800 Product Families processor installed, the Intel TXT pin should be driven high to support Intel TXT. With Intel® Xeon® processor 7500 series installed the Intel TXT pin should be driven low. Note that TXT is not supported on the Intel® Xeon® processor 7500 series. On platforms not supporting the TXT feature, the pin can be strapped low. For Intel® Xeon® processor 7500 series debug purposes, you will need that ability to pull Intel TXT low.
MBP[7:0]	IO	Sideband signals connecting to XDP header for Run-time control and debug.
MEM_THROTTLE[1:0]_N	I	When asserted, the internal memory controllers throttle the memory command issue rate to a configurable fraction of the nominal command rate settings. MEM_Throttle[1] corresponds to mem_ctrl behind the HA xxx 11, and MEM_Throttle[0] corresponds to mem_ctrl behind HA xxx 01.
NMI	I	Interrupt input. Active high. Must be minimum of three clocks.
PECI	IO	Processor Sideband Access via PECI interface.
PRDY_N	O	Processor debug interface.
PREQ_N	I	Processor debug interface.
Proc_ID[1:0]	O	Processor ID. 11: Intel® Xeon® processor 7500. 10: Intel Xeon Processor E7-8800/ 4800/2800 Product Families. 01, 00: Reserved for future generations.
PROCHOT_N	O	The assertion of PROCHOT_N (processor hot) indicates that the processor die temperature has reached its thermal limit. Open Drain Output.
PSI_CACHE_N	O	Vcache Power Status Indicator signal to the VR that the processor is in package C3 or C6 power states so the VR can use fewer phases. This signal has on die termination of 50 ohms.
PSI_N	O	Vcore Power Status Indicator signal to the VR that the processor is in package C3 or C6 power states so the VR can use fewer phases. This signal has on die termination of 50 ohms.

Table 5-1. Signal Definitions (Sheet 4 of 6)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>PWRGOOD</td><td>I</td><td>The processor requires this signal to be a clean indication that all Intel Xeon Processor E7-8800/4800/2800 Product Families processor clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOODcan be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD.
The PWRGOOD signal must be supplied to the processor at 1.1V. This signal is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. VCCSTBY33 signal should be stable for 10 SYSCLOCKs before PWRGOOD is asserted.</td></tr>
<tr><td>QPI[3:0]_DRx_D[P/N][19:0], QPI[3:0]_CLKRX_D[P/N]</td><td>I</td><td>These Intel QPI input data signals provide means of communication between two Intel QPI ports via one uni-directional transfer link (In). The Rx links, are terminally ground referenced. These signals can be configured as a full width link with 20 active lanes, a half width link with 10 active lanes or as a quarter width link with five active lanes.
<table>
<tr><th>Intel QPI Interface</th><th>3:0</th><th>R</th><th>P/N</th><th>DAT[19:0]</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Receiver</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: QPI4RPDAT[0] represents Intel QPI port 5 Data, lane 0,receive signal and Positive bit of the differential pair.</td></tr>
<tr><td>QPI[3:0]_DTX_D[P/ N][19:0],QPI[3:0]_clkTX_D[P/N]</td><td>O</td><td>These Intel QPI output data signals provide means of communication between two Intel QPI ports via one uni-directional transfer link (Out).The links, Tx, are terminally ground referenced. These signals can be configured as a full width link with 20 active lanes, a half width link with 10 active lanes or as a quarter width link with five active lanes.
<table>
<tr><th>Intel QPI Interface</th><th>3:0</th><th>T</th><th>P/N</th><th>DAT[19:0]</th></tr>
<tr><td>Interface Name</td><td>Port Number</td><td>Transmitter</td><td>Differential Pair
Polarity Positive/ Negative</td><td>Lane Number</td></tr>
</table>
Example: QPI4RPDAT[0] represents Intel QPI port 5 Data, lane 0,Transmit signal and Positive bit of the differential pair.</td></tr>
<tr><td>RESET_N</td><td>I</td><td>Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. BOOTMODE[0:1] signals are sampled at the active-to-inactive transition of RESET_N for selecting appropriate BOOTMODE. Also RUNBIST is sampled at the active-to-inactive transition of RESET_N to select BIST operation.</td></tr>
<tr><td>RSVD</td><td></td><td>These Pins are reserved and should be treated as NO CONNECT, left unconnected.</td></tr>
<tr><td>RUNBIST</td><td>I</td><td>This input pin is sampled on a active-to-inactive transition of RESET_N. If sampled high, this enables BIST (Recommended).</td></tr>
<tr><td>SKTDIS_N</td><td>I</td><td>Sampled with the rising edge of RESET_N input. Asserted, signal will disable the socket, tri-state I/O.</td></tr>
<tr><td>SKTID[2:0]</td><td>I</td><td>Socket ID strapping pins. These pins determine the addresses to be used on the SMBus to access the processor.</td></tr>
<tr><td>SKTOCC_N</td><td>O</td><td>Static signal, asserted low when the socket is occupied with processor.</td></tr>
<tr><td>SM_WP</td><td>I</td><td>WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to VCCSTBY33.</td></tr>
</table>

Table 5-1. Signal Definitions (Sheet 5 of 6)

Name	Type	Description
SMBCLK	I/O	The SMBus Clock (SMBCLK) signal is an input clock to the system management logic which is required for operation of the system management features of the Intel Xeon Processor E7-8800/4800/2800 Product Families processor. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor. This is an open drain signal.
SMBDAT	I/O	The SMBus Data (SMBDAT) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices. This is an open drain signal.
SPDCLK	I/O	This is a bi-directional clock signal between Intel Xeon Processor E7-8800/4800/ 2800 Product Families processor, DRAM SPD registers and external components on the board. This is an open drain signal.
SPDDAT	I/O	This is a bi-directional data signal between Intel Xeon Processor E7-8800/4800/2800 Product Families processor, DRAM SPD registers and external components on the board. This is an open drain signal.
SYSCLK_DP/SYSCLK_DP	I	The differential clock pair SYSCLK_DP/SYSCLK_DN provides the fundamental clock source for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor. All processor link agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of SYSCLK crossing the falling edge of SYSCLK_N. These differential clock pair should not be asserted until VCCCORE, VIOC, VIOF, VCACHE and VCC33 are stabilized.
SYSCLK_LAI/SYSCLK_LAI_N	I	These are reference clocks used only for debug purposes. Electrical specifications on these clocks are identical to SYSCLK_DP/SYSCLK_DN.
TCK	I	Test Clock (TCK) provides the clock input for the processor TAP.
TDI	I	Test Data In (TDI) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	Test Data Out (TDO) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. This is an open drain output.
TEST[3:0]	I	Four corner pins used to study socket corner joint reliability. VSS on package, however, not required to be connected.
Test-Hi	I	Strap pins to VIO via TBD resistor.
THERMALERT_N	O	Thermal Alert (THERMALERT_N) is an output signal and is asserted when the on-die thermal sensors readings exceed a pre-programmed threshold.
THERMTRIP_N	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. To ensure that there are no false trips, Thermal Trip (THERMTRIP_N) will activate at a temperature that is about 115°C as measured at the core. Once activated, the processor will stop all execution and the signal remains latched until RESET_N goes active. It is strongly recommended that all power be removed from the processor before bringing the processor back up. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP_N and remain stopped. Strapping is 1k-10k Ohms.
TMS	I	Test Mode Select (TMS) is a JTAG specification support signal used by debug tools.
TRST_N	I	Test Reset (TRST_N) resets the TAP logic. TRST_N must be driven electrically low during power on Reset.
VCACHE	I	This provides power to processor LLC and system interface logic. Actual value of the voltage is determined by the settings of CVID[7:1].
VCACHESENSE	IO	VR Sense lines. (VCACHE)
VCC33	I	VCC33 supplies 3.3V to PIROM/OEM Scratch ROM, INITROM and level translators. This supply is required both for PIROM usage and for correct processor boot operation.
VCCCORE	I	This provides power to the Cores on the processor. Actual value of the voltage is determined by the settings of VID[7:0].
VSSCOREESENSE	IO	VR Sense lines. (Vcore)

Table 5-1. Signal Definitions (Sheet 6 of 6)

Name	Type	Description
VID[7:0]	I/O	VID[7:0] is an input only during Power On Configuration. It is an output signal during normal operation. As an output, VID[7:0] (Voltage ID) are signals that are used to support automatic selection of power supply voltages (V_{CC}). Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for more information. The voltage supply for these signals must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals become valid. The VID signals are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the signals, or disable itself. As an inputs during Power On Configuration: VID [7] is an electronic safety key for distinguishing VR11.1 from PMPV6. VID[6] is a spare bit reserved for future use. VID[5:3] - IMON bits are output signals for IMON gain setting. See *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines* for gain setting information. VID[2:0] or MSID[2:0] - Market Segment ID, or MSID are provided to indicate the Market Segment for the processor and may be used for future processor compatibility or for keying. In addition, MSID protects the platform by preventing a higher power processor from booting in a platform designed for lower power processors. This value is latched from the platform in to the CPU, on the rising edge of VioPWRGOOD, during the cold boot power up sequence.
VIO_VID[4:1]	O	Voltage ID driven out to the VR 11.1 for dynamic/static adjustment of processor voltage set point. Note that these pins are either floated, or tied to ground on the package.
VIOC	I	VIOC provides power to the input/output interface on the Intel Xeon Processor E7-8800/4800/2800 Product Families processor Intel® QPI I/O.
VIOF	I	VIOF provides power to the input/output interface on the Intel Xeon Processor E7-8800/4800/2800 Product Families processor Intel® SMI I/O.
VIOPowerGood	I	VIO Power Good signal.
VREG	I	~1.8 V. Voltage to PLLs.
VSS	I	VSS is the ground plane for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor.
VSSCACHESENSE	IO	VR Sense lines. (Vcache)

§

6 Thermal Specifications

6.1 Package Thermal Specifications

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. For more information on designing a component level thermal solution, refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide*.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

6.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel® processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile (see Table 6-1 and Figure 6-1 for 130W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor, Table 6-1 and Figure 6-2 for 105W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor, and Table 6-1 and Figure 6-3 for 95W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide*.

Intel Xeon Processor E7-8800/4800/2800 Product Families processor implements a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to ensure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) bus as described in Section 6.3. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT_N (see Section 6.2, "Processor Thermal Features" on page 118). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed only need to guarantee that the case temperature meets the thermal profile specifications.

Intel has developed a thermal profile that can be implemented with 130W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor to ensure adherence to Intel reliability requirements. The 130W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor Thermal Profile (see Figure 6-1; Table 6-2) is representative of a volumetrically unconstrained thermal solution (that is, industry enabled 4U heatsink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive

applications. Intel has developed the thermal profile to allow customers to choose the thermal solution and environmental parameters that best suit their platform implementation.

The 105W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor (see Figure 6-2; Table 6-3) and 95W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor (see Figure 6-3; Table 6-4) support a single Thermal Profile. The Thermal Profiles are indicative of a constrained thermal environment. Utilization of a thermal solution that does not meet the Thermal Profile will violate the thermal specifications and may result in permanent damage to the processor.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the associated T_{CASE_MAX} value. It should be noted that the upper point associated with the 130W TDP Intel Xeon Processor E7-8800/4800/2800 Product Families processor Thermal Profile (x = TDP and y = T_{CASE_MAX} P @ TDP) represents a thermal solution design point. In actuality the processor case temperature may not reach this value due to TCC activation (see Figure 6-1 for the Performance Intel Xeon Processor E7-8800/4800/2800 Product Families processor). The lower point of the thermal profile consists of x = $P_{\_PROFILE\_MIN}$ and y = T_{CASE_MAX} @ $P_{\_PROFILE\_MIN}$. $P_{\_PROFILE\_MIN}$ is defined as the processor power at which T_{CASE}, calculated from the thermal profile, is equal to 69°C.

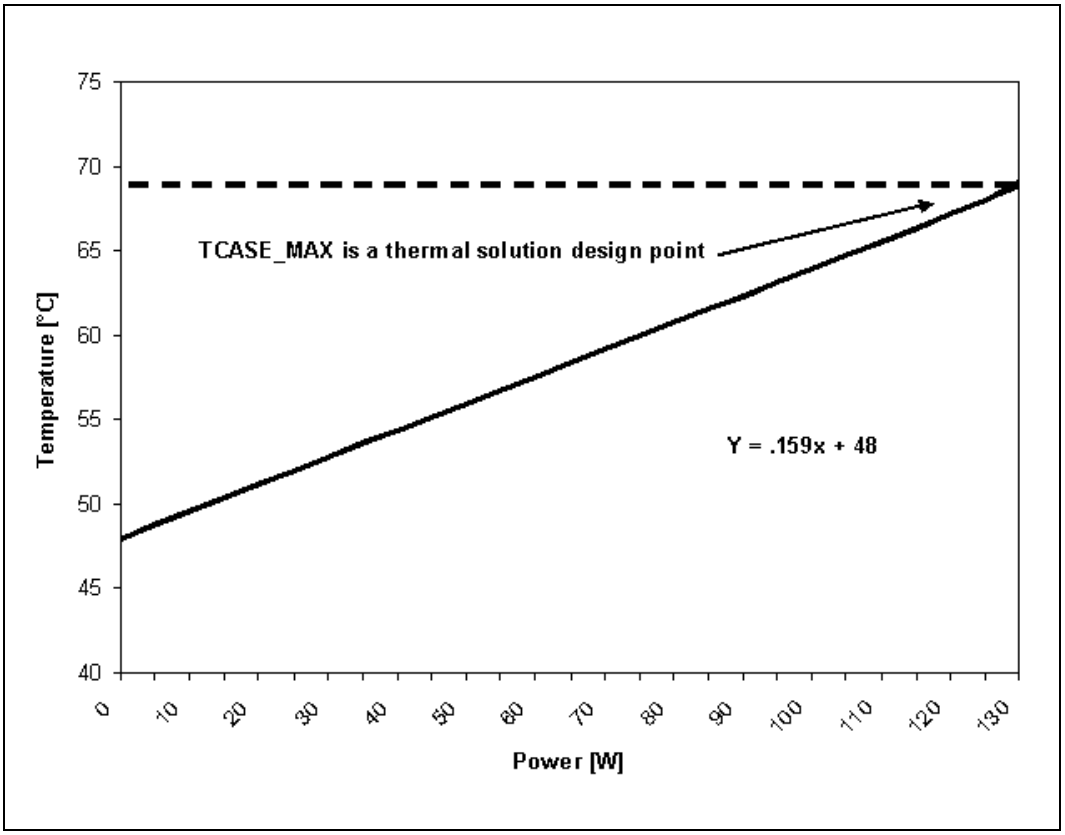
Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) instead of the maximum processor power consumption. The Intel® Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to Section 6.2. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. The Intel Thermal Monitor 1 or Intel Thermal Monitor 2 feature must be enabled for the processor to remain within its specifications.

Table 6-1. Processor Thermal Specifications

Core Frequency	Thermal Design Power (W)	Minimum TCASE (°C)	Maximum TCASE (°C)	Notes
Processor Launch to FMB	130	5	See Figure 6-1; Table 6-2;	1, 2, 3, 4, 5
Processor Launch to FMB	105	5	See Figure 6-2; Table 6-3;	1, 2, 3, 4, 5
Processor Launch to FMB	95	5	See Figure 6-3; Table 6-4;	1, 2, 3, 4, 5

Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on pre-silicon estimates and simulations. These specifications may be updated with characterized data from silicon measurements in a future release of this document.
4. Power specifications are defined at all VIDs found in Table 2-2. The Intel Xeon Processor E7-8800/4800/2800 Product Families processor may be shipped under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-1. 130W TDP Processor Thermal Profile



Notes:
1. Thermal Profile is representative of a volumetrically unconstrained platform. Refer to Table 6-2 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See Section 6.2 for details on TCC activation.)
3. Refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide* for system and environmental implementation details.

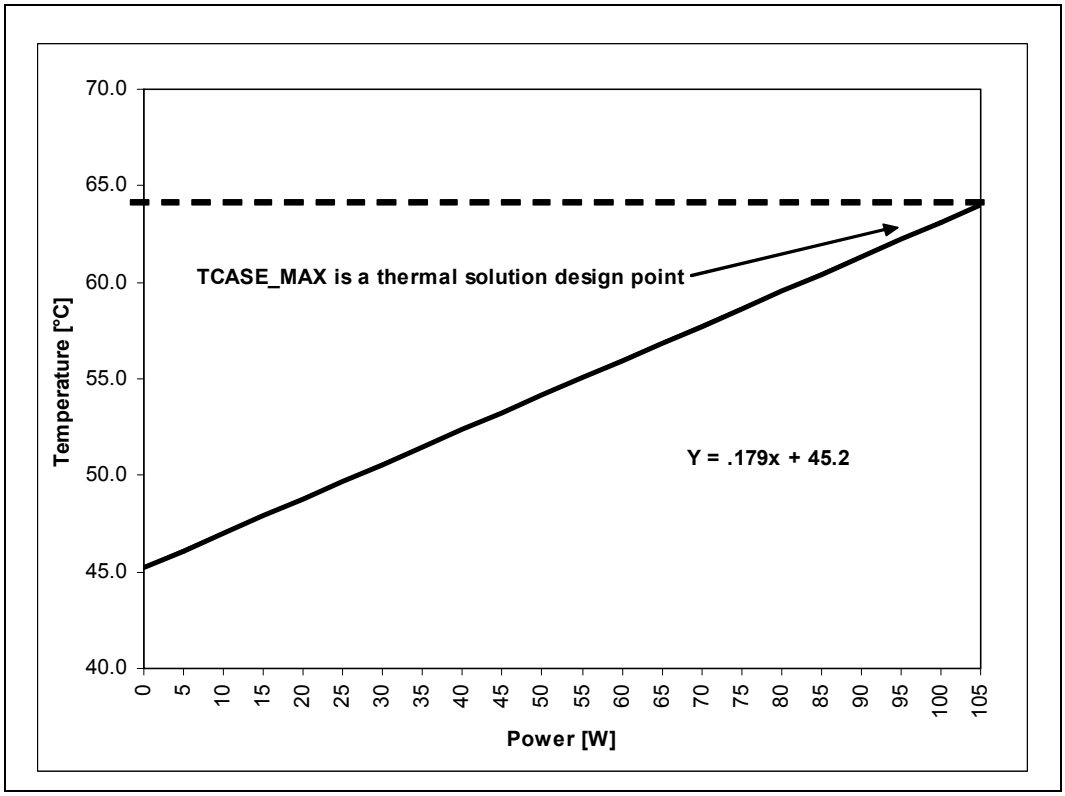
Table 6-2. 130W TDP Processor Thermal Profile Table (Sheet 1 of 2)

Power (W)	T_{CASE_MAX} (°C)
0	48.0
5	48.8
10	49.6
15	50.4
20	51.2
25	52.0
30	52.8
35	53.6
40	54.4
45	55.2
50	56.0
55	56.8
60	57.6
65	58.4

Table 6-2. 130W TDP Processor Thermal Profile Table (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)
70	59.1
75	59.9
80	60.7
85	61.5
90	62.3
95	63.1
100	63.9
105	64.7
110	65.5
115	66.3
120	67.1
125	67.9
130	69.0

Figure 6-2. 105W TDP Processor Thermal Profile



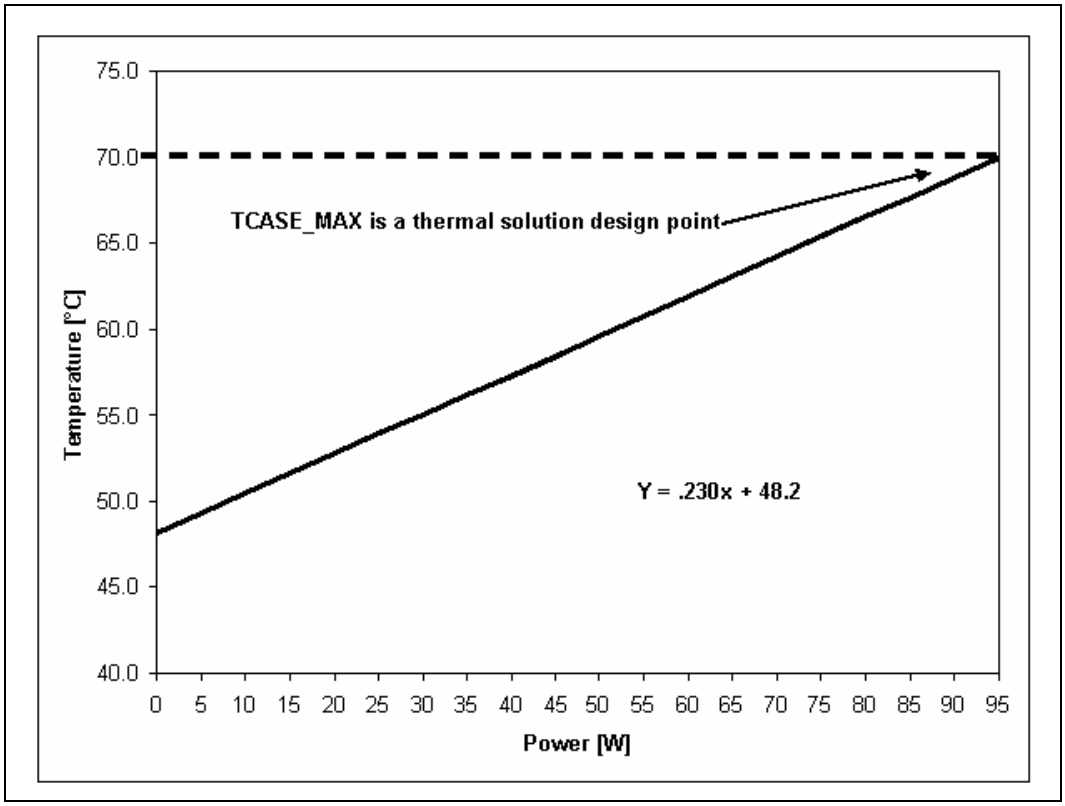
Notes:

1. Thermal Profile is representative of a volumetrically constrained platform. Refer to Table 6-3 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See Section 6.2 for details on TCC activation.)
3. Refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide* for system and environmental implementation details.

Table 6-3. 105W TDP Processor Thermal Profile Table

Power (W)	T_{CASE_MAX} (°C)
0	45.2
5	46.1
10	47.0
15	47.9
20	48.8
25	49.7
30	50.6
35	51.5
40	52.4
45	53.3
50	54.1
55	55.0
60	55.9
65	56.8
70	57.7
75	58.6
80	59.5
85	60.4
90	61.3
95	62.2
100	63.1
105	64.0

Figure 6-3. 95W TDP Processor Thermal Profile



Notes:
1. Thermal profile is representative of a volumetrically constrained platform. Refer to Table 6-4 for discrete points that constitute the thermal profile.
2. Implementation of the Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See Section 6.2 for details on TCC activation.)
3. Refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide* for system and environmental implementation details.

Table 6-4. 95W TDP Processor Thermal Profile Table (Sheet 1 of 2)

Power (W)	T_{CASE_MAX} (°C)
0	48.2
5	49.3
10	50.5
15	51.6
20	52.8
25	53.9
30	55.1
35	56.2
40	57.4
45	58.5
50	59.7
55	60.8
60	62.0
65	63.1
70	64.3

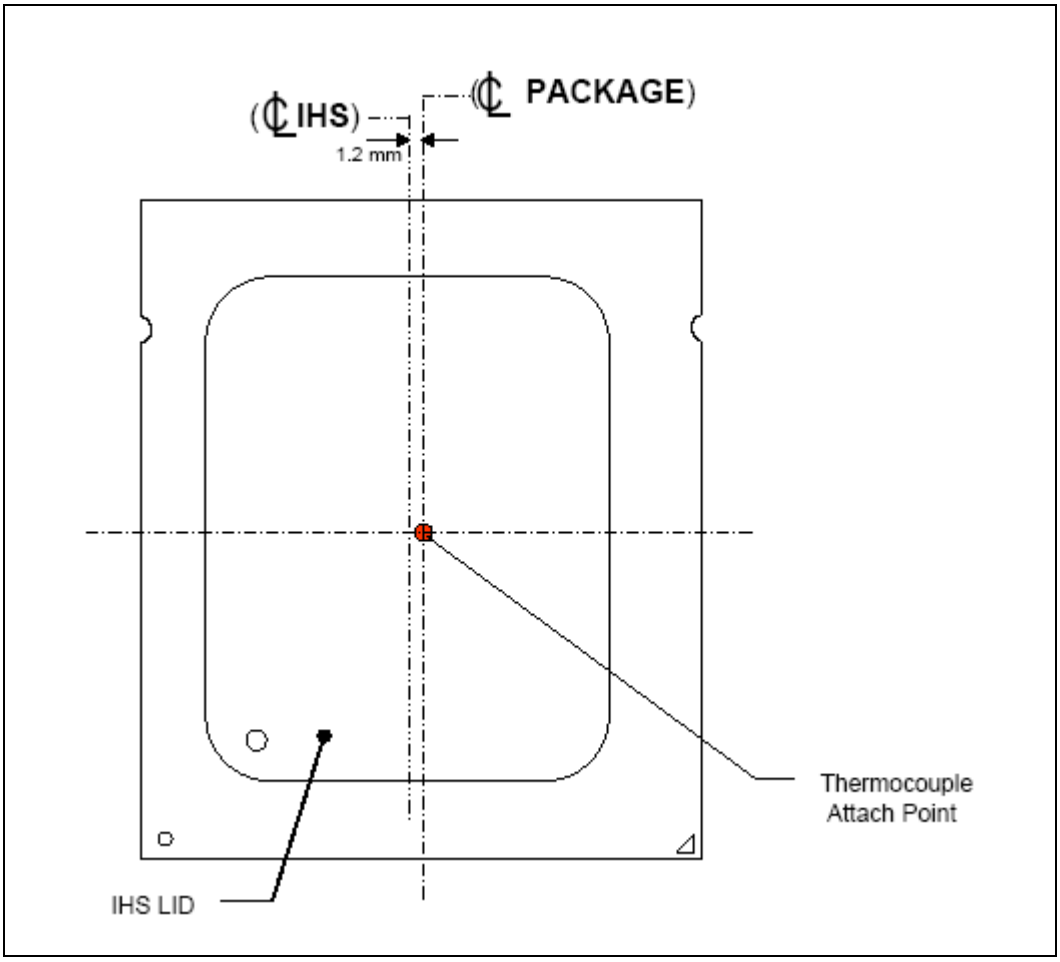
Table 6-4. 95W TDP Processor Thermal Profile Table (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)
75	65.4
80	66.6
85	67.7
90	68.9
95	70.0

6.1.2 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) are specified in Table 6-2 through Table 6-4, and are measured at the geometric top center of the processor substrate, not IHS, as in previous products. Figure 6-4 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Xeon® Processor 7500 Series and Intel® Xeon® Processor E7-8800/4800/2800 Product Families Thermal and Mechanical Design Guide*.

Figure 6-4. Case Temperature (T_{CASE}) Measurement Location



Note: Figure is not to scale and is for reference only.

6.2 Processor Thermal Features

6.2.1 Thermal Monitor Features

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor provides two thermal monitor features, Intel Thermal Monitor 1 (“TM1”) and Intel Thermal Monitor 2 (“TM2”). Both Intel Thermal Monitor 1 and 2 must be enabled in BIOS for the processor to be operating within specifications. When both are enabled, Intel Thermal Monitor 2 will be activated first and Intel Thermal Monitor 1 will be added if Intel Thermal Monitor 2 is not effective.

6.2.2 Intel® Thermal Monitor 1

The Intel Thermal Monitor 1 feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. Intel Thermal Monitor 1 or Intel Thermal Monitor 2 must be enabled for the processor to be operating within specifications. The temperature at which Intel Thermal Monitor 1 activates the thermal control circuit is not user-configurable and is not software-visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When Intel Thermal Monitor 1 is enabled, and a high temperature situation exists (that is, TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 - 50%). Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a thermal solution designed to meet the Intel Xeon Processor E7-8800/4800/2800 Product Families processor Thermal Profiles, it is anticipated that the TCC would only be activated for very short periods of time when running the most power-intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The duty cycle for the TCC, when activated by the Intel Thermal Monitor 1, is factory-configured and cannot be modified. Intel Thermal Monitor 1 does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.3 Intel Thermal Monitor 2

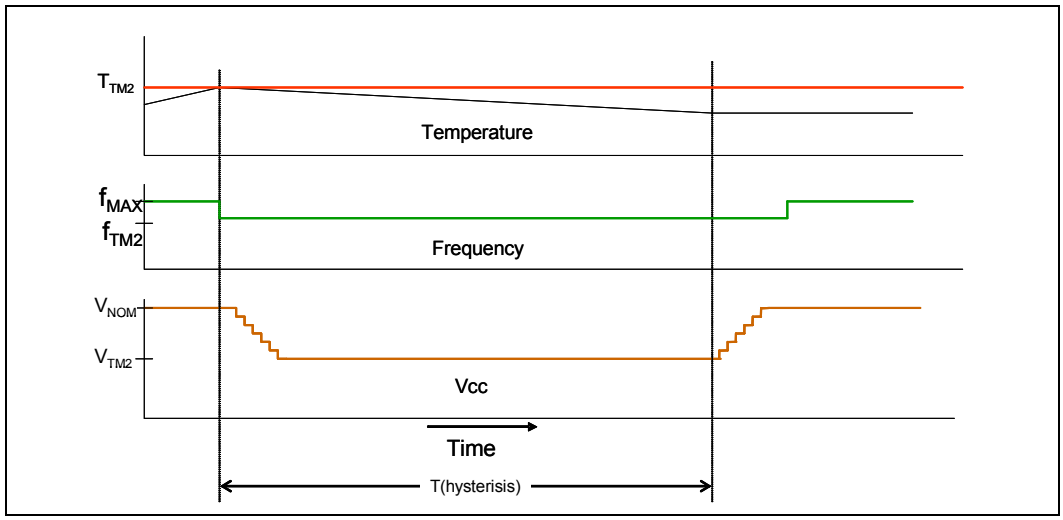
The Intel Xeon Processor E7-8800/4800/2800 Product Families processor adds supports for an enhanced thermal monitor capability known as Intel Thermal Monitor 2. This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor. Intel Thermal Monitor 1 or Intel Thermal Monitor 2 must be enabled for the processor to be operating within specifications. Intel Thermal Monitor 2 requires support for dynamic VID transitions in the platform.

When Intel Thermal Monitor 2 is enabled, and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated for all processor cores. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption. The lowest bus multiplier for the Intel Thermal Monitor 2 is 8:1. This results in an operating frequency of 1066 MHz.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support the Intel Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one or two VID table entries (see Table 2-2). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to ensure proper operation once the processor reaches its normal operating frequency. Refer to Figure 6-5 for an illustration of this ordering.

Figure 6-5. Intel® Thermal Monitor 2 Frequency and Voltage Ordering



The PROCHOT_N signal is asserted when a high-temperature situation is detected, regardless of whether Intel Thermal Monitor 1 or Intel Thermal Monitor 2 is enabled.

6.2.4 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Intel Thermal Monitor 1 and Intel Thermal Monitor 2 features. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing Intel Xeon Processor E7-8800/4800/2800 Product Families processor must not rely on software usage of this mechanism to limit the processor temperature. There are two ways to implement On-Demand mode. If bit

4 of the IA32_CLOCK_MODULATION MSR is set to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. Also, a write the P_CNT I/O address, the processor will immediately reduce power consumptions as well.

The P_CNT I/O address write controls all active cores. The MSR write only impacts the core that performed the MSR write. The P_CNT I/O address write takes priority over the MSR write.

When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

6.2.5 PROCHOT_N Signal

An external signal, PROCHOT_N (processor hot) is asserted when the temperature of any processor core has reached its factory configured trip point. If Intel Thermal Monitor 1 and Intel Thermal Monitor 2 are enabled (note that Intel Thermal Monitor 1 and Intel Thermal Monitor 2 must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT_N is asserted. Intel Thermal Monitor 2 activates first, and Intel Thermal Monitor 1 activates only if needed to further reduce temperature. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT_N. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual* and the *Intel® Xeon® Processor 7500 Series Datasheet Volume 2* for specific register and programming details.

PROCHOT_N is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by Thermal Profile) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT_N trip temperature, or the case temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, or PROCHOT_N.

This signal is only valid when power good is asserted, and CPU reset is not asserted.

6.2.6 FORCE_PR_N Signal

The FORCE_PR_N (force power reduction) input can be used by the platform to cause Intel Xeon Processor E7-8800/4800/2800 Product Families processor to activate the TCC. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCE_PR_N signal. FORCE_PR_N is an asynchronous input. Assertion of the FORCE_PR_N signal will activate TCC for all operating processor cores. The TCC will remain active until the system deasserts FORCE_PR_N. FORCE_PR_N can be used to thermally protect other system components. To use the VR as an example, when FORCE_PR_N is asserted, the TCC circuit in the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

It should be noted that assertion of FORCE_PR_N does not automatically assert PROCHOT_N. As mentioned previously, the PROCHOT_N signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 µs is recommended when FORCE_PR_N is asserted by the system. Sustained activation of the FORCE_PR_N signal may cause noticeable platform performance degradation.

6.2.7 THERMTRIP_N Signal

Regardless of whether or not the Intel Thermal Monitor 1 or 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when any core has reached an elevated temperature (refer to the THERMTRIP_N definition in Table 5-1). At this point, the sideband signal THERMTRIP_N will go active and stay active as described in Table 5-1. THERMTRIP_N activation is independent of processor activity. If THERMTRIP_N is asserted, processor core voltage (V_{CC}) and processor cache voltage (Vcache) must be removed within the time frame defined.

This signal is only valid when power good is asserted, and CPU reset is not asserted.

6.2.8 THERMALERT_N Signal

The THERMALERT_N pin activates when a pre-programmed temperature is reached on any of the device cores. This pre-programmed temperature is an offset from Prochot, an programmed via BIOS. There is no sign for the value, as it is always assumed that the values is less than or equal to Prochot. When not programmed, the value is zero.

The expected usage for this signal is in fan speed control when direct PECI readings are not used. Note that all thermal specifications must be met when using this signal as part of an over all thermal solution.

This signal is only valid when power good is asserted, CPU reset is not asserted, and BIOS has configured the THERMALERT threshold temperature. Note that BIOS can not configure the THERMALERT threshold until the processor is out of reset.

6.3 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic ‘0’ or logic ‘1’. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel® processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

The PECI bus offers:

- A wide speed range from 2 Kbps to 2 Mbps
- CRC check byte used to efficiently and atomically confirm accurate data delivery
- Synchronization at the beginning of every message minimizes device timing accuracy requirements

What follows is a processor-specific PECI client definition, and is largely an addendum to the PECI Network Layer and Design Recommendations sections for the PECI 2.0 Specification document.

Note: Note that the PECI commands described in this document apply to the Intel Xeon Processor E7-8800/4800/2800 Product Families processor only. Refer to Table 6-5 for a list of PECI commands supported by the Intel Xeon Processor E7-8800/4800/2800 Product Families processor PECI client.

Table 6-5. Summary of Processor-specific PECI Commands

Command	Supported on Intel Xeon Processor E7-8800/4800/2800 Product Families processor CPU
Ping()	Yes
GetDIB()	Yes
GetTemp()	Yes
PCIConfigRd()	Yes
PCIConfigWr()	Yes
MbxSend() [1]	Yes
MbxGet() [1]	Yes

Note:
1. Refer to Table 6-9 for a summary of mailbox commands supported by the Intel Xeon Processor E7-8800/4800/2800 Product Families processor CPU.

6.3.1 PECI Client Capabilities

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor PECI client is designed to support the following sideband functions:

- Processor and DRAM thermal management
- Platform manageability functions, including thermal, power and electrical error monitoring
- Processor interface tuning and diagnostics capabilities (Intel® Interconnect BIST [Intel® IBIST]).

6.3.1.1 Thermal Management

Processor fan speed control is managed by comparing PECI thermal readings against the processor-specific fan speed control reference point, or $T_{CONTROL}$. Both $T_{CONTROL}$ and PECI thermal readings are accessible via the processor PECI client. These variables are referenced to a common temperature, the TCC activation point, and are both defined as negative offsets from that reference. Algorithms for fan speed management using PECI thermal readings and the $T_{CONTROL}$ reference are documented in Section 6.3.2.6.

PECI-based access to DRAM thermal readings and throttling control coefficients provide a means for Board Management Controllers (BMCs) or other platform management devices to feed hints into on-die memory controller throttling algorithms. These control coefficients are accessible using PCI configuration space writes via PECI. The PECI-based configuration write functionality is defined in Section 6.3.2.5.

6.3.1.2 Platform Manageability

PECI allows full read access to error and status monitoring registers within the processor's PCI configuration space. It also provides insight into thermal monitoring functions such as TCC activation timers and thermal error logs.

6.3.1.3 Processor Interface Tuning and Diagnostics

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor Intel IBIST allows for in-field diagnostic capabilities in Intel QPI and memory controller interfaces. PECI provides a port to execute these diagnostics via its PCI Configuration read and write capabilities.

6.3.2 Client Command Suite

6.3.2.1 Ping()

Ping() is a required message for all PECI devices. This message is used to enumerate devices or determine if a device has been removed, been powered-off, etc. A Ping() sent to a device address always returns a non-zero Write FCS if the device at the targeted address is able to respond.

6.3.2.1.1 Command Format

The Ping() format is as follows:

Write Length: 0

Read Length: 0

Figure 6-6. Ping()

Byte #	0	1	2	3
Byte Definition	Client Address	Write Length 0x00	Read Length 0x00	FCS

An example Ping() command to PECI device address 0x30 is shown below.

Figure 6-7. Ping() Example

Byte #	0	1	2	3
Byte Definition	0x30	0x00	0x00	0xe1

6.3.2.2 GetDIB()

The processor PECI client implementation of GetDIB() includes an 8-byte response and provides information regarding client revision number and the number of supported domains. All processor PECI clients support the GetDIB() command.

6.3.2.2.1 Command Format

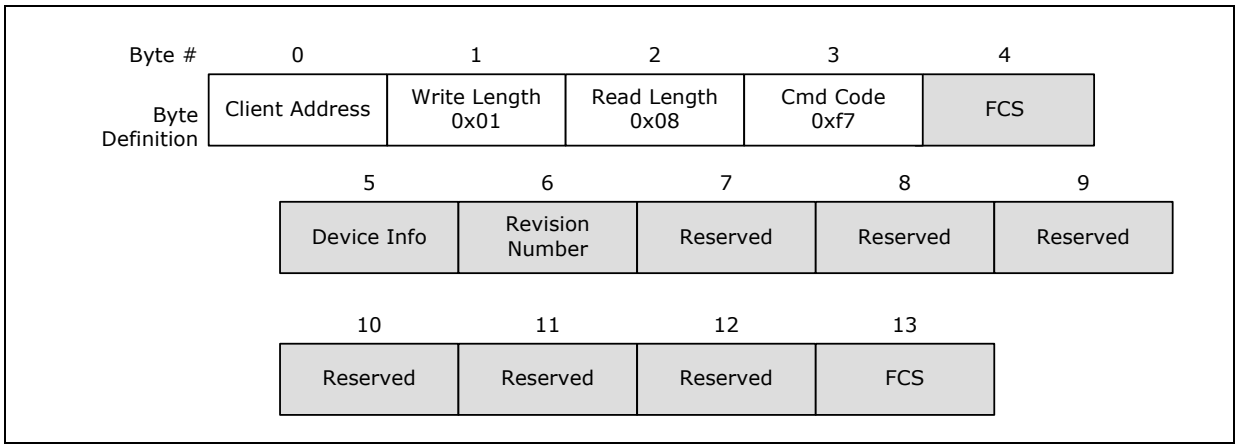
The GetDIB() format is as follows:

Write Length: 1

Read Length: 8

Command: 0xf7

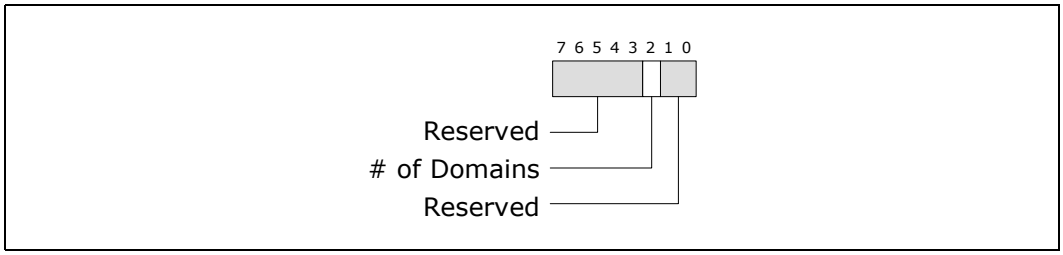
Figure 6-8. GetDIB()



6.3.2.2.2 Device Info

The Device Info byte gives details regarding the PECI client configuration. At a minimum, all clients supporting GetDIB will return the number of domains inside the package via this field. With any client, at least one domain (Domain 0) must exist. Therefore, the Number of Domains reported is defined as the number of domains in addition to Domain 0. For example, if the number 0b1 is returned, that would indicate that the PECI client supports two domains.

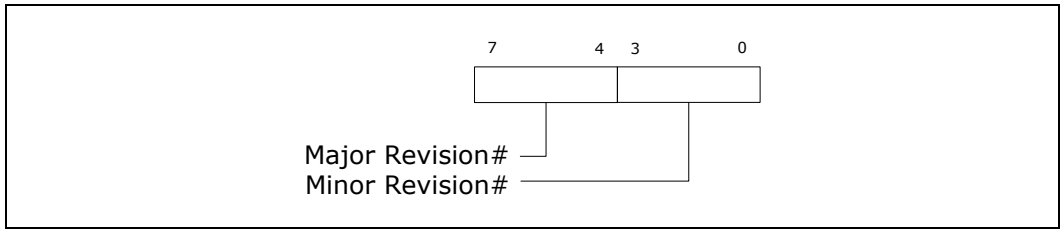
Figure 6-9. Device Info Field Definition



6.3.2.2.3 Revision Number

All clients that support the GetDIB command also support Revision Number reporting. The revision number may be used by a host or originator to manage different command suites or response codes from the client. Revision Number is always reported in the second byte of the GetDIB() response. The Revision Number always maps to the revision number of this document.

Figure 6-10. Revision Number Definition



6.3.2.3 GetTemp()

The GetTemp() command is used to retrieve the temperature from a target PECI address. The temperature is used by the external thermal management system to regulate the temperature on the die. The data is returned as a negative value representing the number of degrees centigrade below the Thermal Control Circuit Activation temperature of the PECI device. Note that a value of zero represents the temperature at which the Thermal Control Circuit activates. The actual value that the thermal management system uses as a control set point (Tcontrol) is also defined as a negative number below the Thermal Control Circuit Activation temperature. TCONTROL may be extracted from the processor by issuing a PECI Mailbox MbxGet() (see Section 6.3.2.8), or using a RDMSR instruction.

Refer to Section 6.3.6 for details regarding temperature data formatting.

6.3.2.3.1 Command Format

The GetTemp() format is as follows:

Write Length: 1

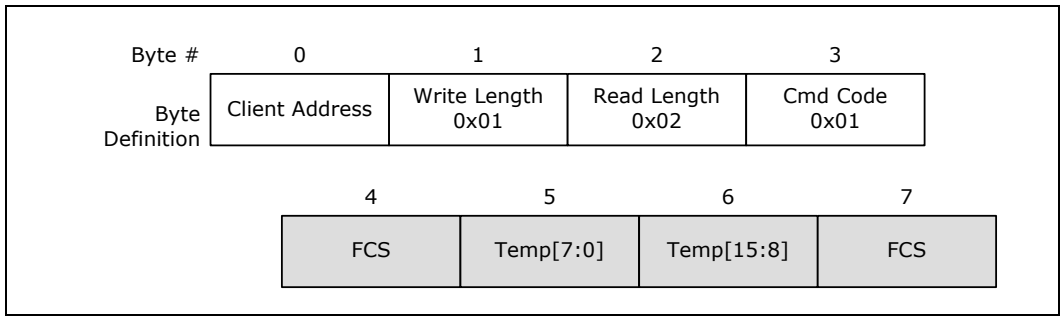
Read Length: 2

Command: 0x01

Multi-Domain Support: Yes (see Table 6-15)

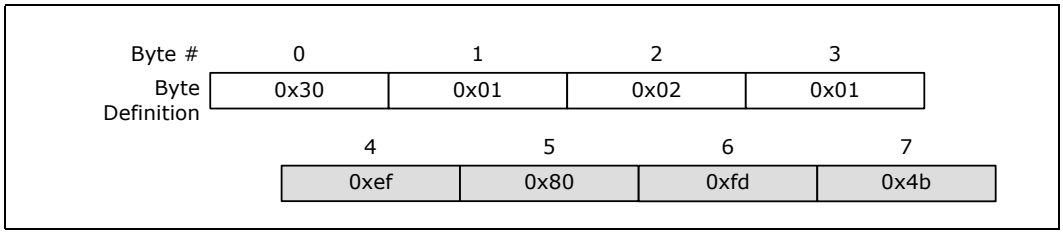
Description: Returns the current temperature for addressed processor PECI client.

Figure 6-11. GetTemp()



Example bus transaction for a thermal sensor device located at address 0x30 returning a value of negative 10°C:

Figure 6-12. GetTemp() Example



6.3.2.3.2 Supported Responses

The typical client response is a passing FCS and good thermal data. Under some conditions, the client's response will indicate a failure.

Table 6-6. GetTemp() Response Definition

Response	Meaning
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature.

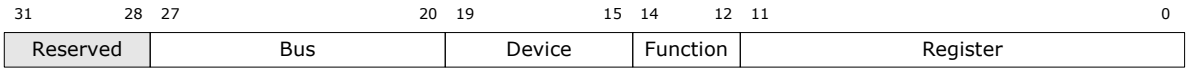
6.3.2.4 PCIConfigRd()

The PCIConfigRd() command gives sideband read access to the entire PCI configuration space maintained in the processor. This capability does not include support for route-through to downstream devices or sibling processors. The exact listing of supported devices, functions, and registers can be found in the *Intel® Xeon® Processor 7500 Series Datasheet Volume 2*. PECI originators may conduct a device/function/register enumeration sweep of this space by issuing reads in the same manner that BIOS would. A response of all 1's indicates that the device/function/register is unimplemented.

PCI configuration addresses are constructed as shown in the following diagram. Under normal in-band procedures, the Bus number (including any reserved bits) would be used to direct a read or write to the proper device. Since there is a one-to-one mapping between any given client address and the bus number, any request made with a bad Bus number is ignored and the client will respond with a 'pass' completion code but all 0's in the data. The only legal bus number is 0x00. The client will return all 1's in the data response and 'pass' for the completion code for all of the following conditions:

- Unimplemented Device
- Unimplemented Function
- Unimplemented Register

Figure 6-13. PCI Configuration Address



PCI configuration reads may be issued in byte, word, or dword granularities.

6.3.2.4.1 Command Format

The PCIConfigRd() format is as follows:

Write Length: 5

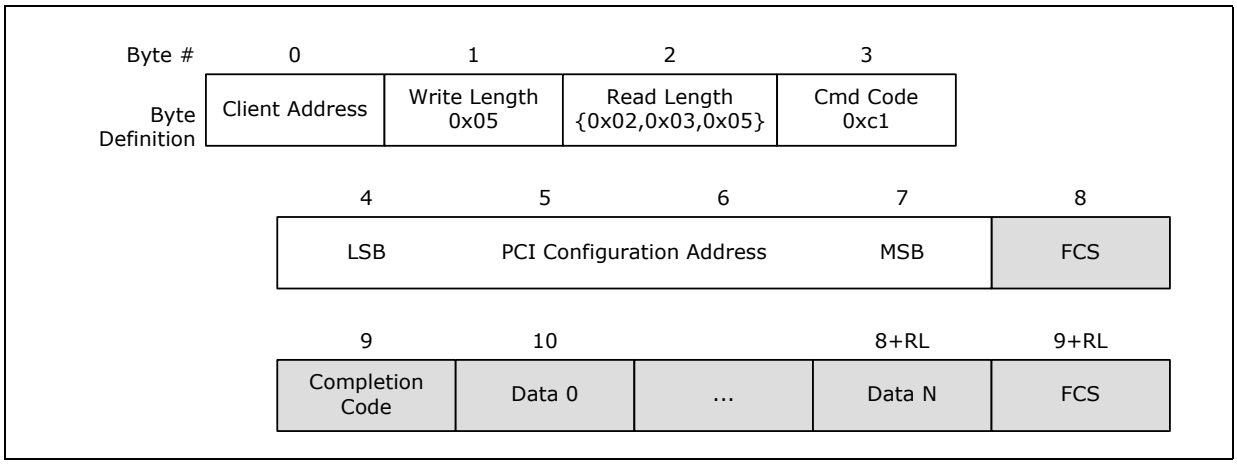
Read Length: 2 (byte data), 3 (word data), 5 (dword data)

Command: 0xc1

Multi-Domain Support: Yes (see Table 6-15)

Description: Returns the data maintained in the PCI configuration space at the PCI configuration address sent. The Read Length dictates the desired data return size. This command supports byte, word, and dword responses as well as a completion code. All command responses are prepended with a completion code that includes additional pass/fail status information. Refer to Section 6.3.4.2 for details regarding completion codes.

Figure 6-14. PCIConfigRd()



Note that the 4-byte PCI configuration address defined above is sent in standard PECI ordering with LSB first and MSB last.

6.3.2.4.2 Supported Responses

The typical client response is a passing FCS, a passing Completion Code (CC) and valid Data. Under some conditions, the client's response will indicate a failure.

Table 6-7. PCIConfigRd() Response Definition

Response	Meaning
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

6.3.2.5 PCIConfigWr()

The PCIConfigWr() command gives sideband write access to the PCI configuration space maintained in the processor. The exact listing of supported devices, functions is defined in the *Intel® Xeon® Processor 7500 Series Datasheet Volume 2*. PECI originators may conduct a device/function/register enumeration sweep of this space by issuing reads in the same manner that BIOS would.

PCI configuration addresses are constructed as shown in Figure 6-13, and this command is subject to the same address configuration rules as defined in Section 6.3.2.4. PCI configuration reads may be issued in byte, word, or dword granularities.

Because a PCIConfigWr() results in an update to potentially critical registers inside the processor, it includes an Assured Write FCS (AW FCS) byte as part of the write data payload. In the event that the AW FCS mismatches with the client-calculated FCS, the client will abort the write and will always respond with a bad Write FCS.

6.3.2.5.1 Command Format

The PCIConfigWr() format is as follows:

Write Length: 7 (byte), 8 (word), 10 (dword)

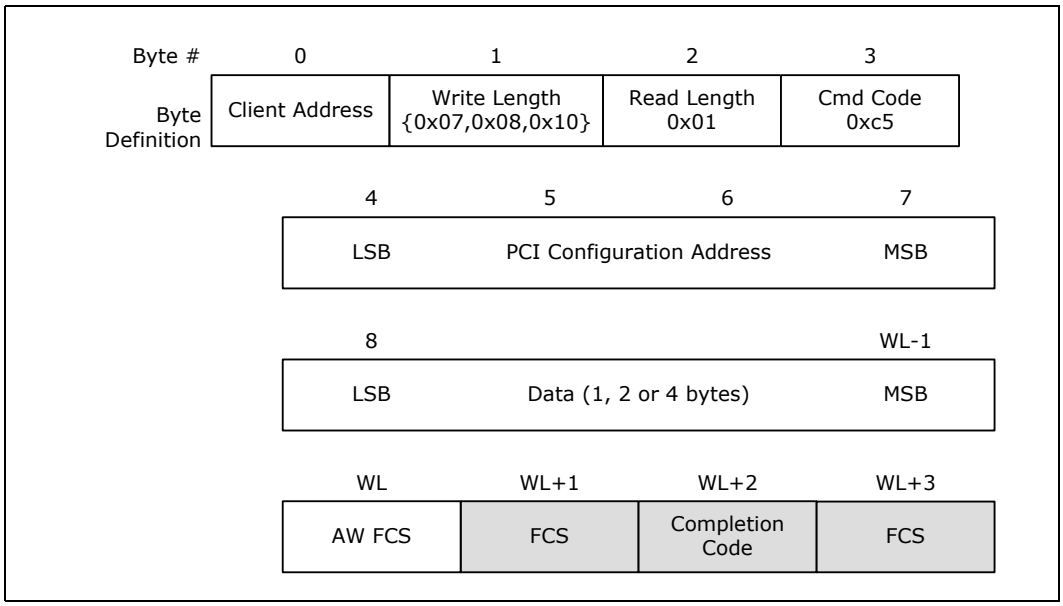
Read Length: 1

Command: 0xc5

Multi-Domain Support: Yes (see Table 6-15)

Description: Writes the data sent to the requested register address. Write Length dictates the desired write granularity. The command always returns a completion code indicating the pass/fail status information. Write commands issued to illegal Bus Numbers, or unimplemented Device / Function / Register addresses are ignored but return a passing completion code. Refer to Section 6.3.4.2 for details regarding completion codes.

Figure 6-15. PCIConfigWr()



Note that the 4-byte PCI configuration address and data defined above are sent in standard PECI ordering with LSB first and MSB last.

6.3.2.5.2 Supported Responses

The typical client response is a passing FCS, a passing Completion Code and valid Data. Under some conditions, the client's response will indicate a failure.

Table 6-8. PCIConfigWr() Response Definition

Response	Meaning
Bad FCS	Electrical error or AW FCS failure
Abort FCS	Illegal command formatting (mismatched RL/WL/Command Code)
CC: 0x40	Command passed, data is valid
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.

6.3.2.6 Mailbox

The PECI mailbox ("Mbx") is a generic interface to access a wide variety of internal processor states. A Mailbox request consists of sending a 1-byte request type and 4-byte data to the processor, followed by a 4-byte read of the response data. The following sections describe the Mailbox capabilities as well as the usage semantics for the MbxSend and MbxGet commands which are used to send and receive data.

6.3.2.6.1 Capabilities

Table 6-9. Mailbox Command Summary (Sheet 1 of 2)

Command Name	Request Type Code (byte)	MbxSend Data (dword)	MbxGet Data (dword)	Description
Ping	0x00	0x00	0x00	Verify the operability / existence of the Mailbox.
Thermal Status Read/Clear	0x01	Log bit clear mask	Thermal Status Register	Read the thermal status register and optionally clear any log bits. The thermal status has status and log bits indicating the state of processor TCC activation, external FORCEPR_N assertion, and Critical Temperature threshold crossings.
Counter Snapshot	0x03	0x00	0x00	Snapshots all PECI-based counters
Counter Clear	0x04	0x00	0x00	Concurrently clear and restart all counters.
Counter Read	0x05	Counter Number	Counter Data	Returns the counter number requested. 0: Total reference time 1: Total TCC Activation time counter
Icc-TDC Read	0x06	0x00	Icc-TDC	Returns the specified Icc-TDC of this part, in Amps.
Thermal Config Data Read	0x07	0x00	Thermal config data	Reads the thermal averaging constant.
Thermal Config Data Write	0x08	Thermal Config Data	0x00	Writes the thermal averaging constant.
Tcontrol Read	0x09	0x00	Tcontrol	Reads the fan speed control reference temperature, Tcontrol, in PECI temperature format.
T-state Throttling Control Read	0xB	0x00	ACPI T-state Control Word	Reads the PECI ACPI T-state throttling control word.

Table 6-9. Mailbox Command Summary (Sheet 2 of 2)

Command Name	Request Type Code (byte)	MbxSend Data (dword)	MbxGet Data (dword)	Description
T-state Throttling Control Write	0xC	ACPI T-state Control Word	0x00	Writes the PECI ACPI T-state throttling control word.
Average Temperature Read	0x21	0x00	Average Temperature Value	Intel Xeon Processor E7-8800/4800/2800 Product Families processor only: Reads the average temperature of all cores in PECI temperature format.
Get Uncore Temperature	0x22	0x00	Get _Uncore_ Temp	Reads the uncore temperature in PECI format.
Write P-state limit	0x23	0x00	WRITE_P_STATE_LIMIT	Sets an upper limit for P-state frequency ratio.
Read P-state limit	0x24	0x00	READ_P_STATE_LIMIT	Reads the programmed P-state limit if set.

Any MbxSend request with a request type not defined in Table 6-9 will result in a failing completion code.

More detailed command definitions follow.

6.3.2.6.2 Ping

The Mailbox interface may be checked by issuing a Mailbox 'Ping' command. If the command returns a passing completion code, it is functional. Under normal operating conditions, the Mailbox Ping command should always pass.

6.3.2.6.3 Thermal Status Read / Clear

The Thermal Status Read provides information on package level thermal status. Data includes:

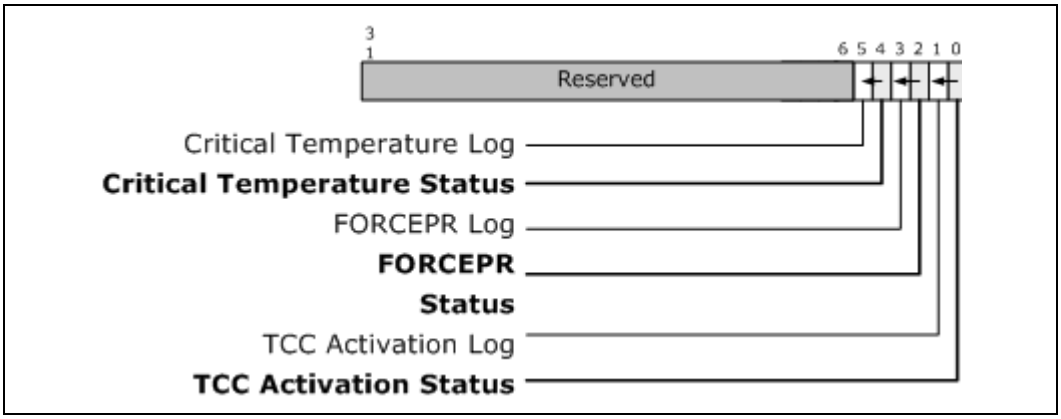
- The status of TCC activation / PROCHOT_N output
- FORCEPR_N input
- Critical Temperature

These status bits are a subset of the bits defined in the IA32_THERM_STATUS MSR on the processor, and more details on the meaning of these bits may be found in the *Intel® 64 and IA-32 Architectures Software Developer's Manual*, Vol. 3B.

Both status and sticky log bits are managed in this status word. All sticky log bits are set upon a rising edge of the associated status bit, and the log bits are cleared only by Thermal Status reads or a processor reset. A read of the Thermal Status Word always includes a log bit clear mask that allows the host to clear any or all log bits that it is interested in tracking.

A bit set to 0b0 in the log bit clear mask will result in clearing the associated log bit. If a mask bit is set to 0b0 and that bit is not a legal mask, a failing completion code will be returned. A bit set to 0b1 is ignored and results in no change to any sticky log bits. For example, to clear the TCC Activation Log bit and retain all other log bits, the Thermal Status Read should send a mask of 0xFFFFFFFD.

Figure 6-16. Thermal Status Word



6.3.2.6.4 Counter Snapshot / Read / Clear

A reference time and 'Thermally Constrained' time are managed in the processor. These two counters are managed via the Mailbox. These counters are valuable for detecting thermal runaway conditions where the TCC activation duty cycle reaches excessive levels.

The counters may be simultaneously snapshot, simultaneously cleared, or independently read. The simultaneous snapshot capability is provided in order to guarantee concurrent reads even with significant read latency over the PECI bus. Each counter is 32-bits wide.

Table 6-10. Counter Definition

Counter Name	Counter Number	Definition
Total Time	0x00	Counts the total time the processor has been executing with a resolution of approximately 1ms. This counter wraps at 32 bits.
Thermally Constrained Time	0x01	Counts the total time the processor has been operating at a lowered performance due to TCC activation. This timer includes the time required to ramp back up to the original P-state target after TCC activation expires. This timer does not include TCC activation time as a result of an external assertion of FORCEPR_N.

6.3.2.6.5 Icc-TDC Read

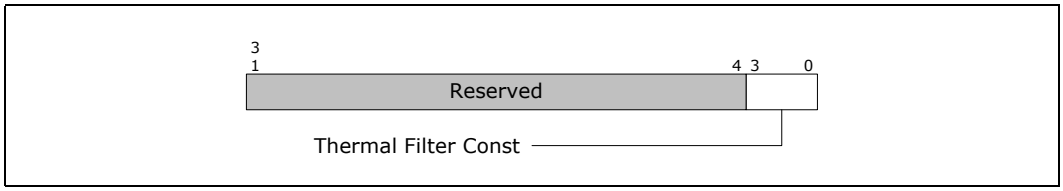
Icc-TDC is the Intel Xeon Processor E7-8800/4800/2800 Product Families processor TDC current draw specification. This data may be used to confirm matching Icc profiles of processors in MP configurations. It may also be used during the processor boot sequence to verify processor compatibility with motherboard Icc delivery capabilities.

This command returns Icc-TDC in units of 1 Amp.

6.3.2.6.6 Thermal Data Config Read / Write

The Thermal Data Configuration register allows the PECI host to control the window over which thermal data is filtered. The default window is 256 ms. The host may configure this window by writing a Thermal Filtering Constant as a power of two. E.g., sending a value of 9 results in a filtering window of 2^9 or 512 ms.

Figure 6-17. Thermal Data Configuration Register



6.3.2.6.7 TCONTROL Read

TCONTROL is used for fan speed control management. The TCONTROL limit may be read over PECI using this Mailbox function. Unlike the in-band MSR interface, this TCONTROL value is already adjusted to be in the native PECI temperature format of a 2-byte, 2's complement number.

6.3.2.6.8 T-state Throttling Control Read / Write

PECI offers the ability to enable and configure ACPI T-state (core clock modulation) throttling. ACPI T-state throttling forces all CPU cores into duty cycle clock modulation where the core toggles between C0 (clocks on) and C1 (clocks off) states at the specified duty cycle. This throttling reduces CPU performance to the duty cycle specified and, more importantly, results in processor power reduction.

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports software initiated T-state throttling and automatic T-state throttling as part of the internal Thermal Monitor response mechanism (upon TCC activation). The PECI T-state throttling control register read/write capability is managed only in the PECI domain. In-band software may not manipulate or read the PECI T-state control setting. In the event that multiple agents are requesting T-state throttling simultaneously, the CPU always gives priority to the lowest power setting, or the numerically lowest duty cycle.

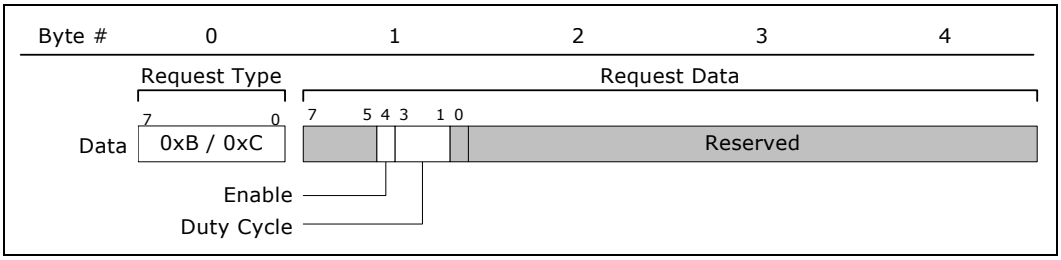
On Intel Xeon Processor E7-8800/4800/2800 Product Families processors, the only supported duty cycle is 12.5% (12.5% clocks on, 87.5% clocks off). It is expected that T-state throttling will be engaged only under emergency thermal or power conditions. Future products may support more duty cycles, as defined in the following table:

Table 6-11. ACPI T-state Duty Cycle Definition

Duty Cycle Code	Definition
0x0	Undefined
0x1	**12.5% clocks on / 87.5% clocks off**
0x2	25% clocks on / 75% clocks off
0x3	37.5% clocks on / 62.5% clocks off
0x4	50% clocks on / 50% clocks off
0x5	62.5% clocks on / 37.5% clocks off
0x6	75% clocks on / 25% clocks off
0x7	87.5% clocks on / 12.5% clocks off

The T-state control word is defined as follows:

Figure 6-18. ACPI T-state Throttling Control Read / Write Definition



6.3.2.6.9 Average Temperature Read

The Average Temperature Read mailbox command implemented by Intel® Xeon® processor 7500 series provides an alternative temperature assessment to that provided by the GetTemp() PECI command. Where GetTemp() returns the average of the hottest sense points on the processor, the Average Temp Read returns the average of all core temperature sense points. The values from each sensor are averaged and filtered. The data is returned as a negative value representing the number of degrees centigrade below the Thermal Control Circuit Activation temperature of the PECI device

6.3.2.6.10 Get Uncore Temperature

The Get Uncore Temperature command implemented by the processor is used to retrieve the uncore temperature from a target PECI address. The temperature can be used as an added input to the external thermal management system to regulate the temperature on the die. The data is returned as a negative value representing the number of degrees centigrade below the Thermal Control Circuit Activation temperature of the PECI device. Note that a value of zero represents the temperature at which the Thermal Control Circuit activates. The actual value that the thermal management system uses as a control set point (Tcontrol) is also defined as a negative number below the Thermal Control Circuit Activation temperature.

6.3.2.6.11 Write P-State Limit

This command creates a P-state frequency upper limit for OS requested P-states per socket. The default value for this variable will correspond to P0 for Intel Xeon Processor E7-8800/4800/2800 Product Families processors which support Intel Turbo Boost Technology, and P1 for the remaining Intel Xeon Processor E7-8800/4800/2800 Product Families processors. Any request for a frequency greater than P1 will be taken as a request to have all available P-states enabled.

Depending on the current package operating state, using this function may lead to a P-state transition.

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor expects a mailbox sideband limit request as a core clock multiplier ratio corresponding to a valid P-state defined in the ACPI table (ACPI table is visible to PECI Host Controller).

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports clock ratios between MaxNonTurboRatio (P1)+1 and MaxEfficiencyRatio (Pn) as allowable P-state requests, but it may expose only selective clock ratios as valid P-states in the ACPI table.

Should a requested value be below Pn, it will be clamped at Pn. Should a requested value be greater than P1, the value will be clipped to P1+1 for those Intel Xeon Processor E7-8800/4800/2800 Product Families processors which support Intel Turbo Boost Technology, and P1 for those which do not.

This setting is persistent across warm resets.

6.3.2.6.12 Read P-State Limit

This mailbox command is used by the PECI host to read out a socket's current sideband P-state frequency ratio upper limit. If the value written is greater than allowed by the ACPI table, the largest legal value will be returned. If the value written is lower than allowed by the ACPI table, the lowest legal value will be returned. A value of P1+1 indicates enabling of all available P-states.

6.3.2.7 MbxSend()

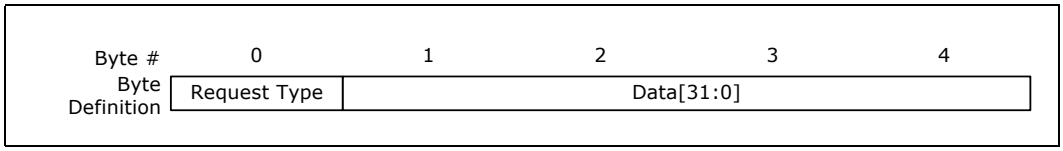
The MbxSend() command is utilized for sending requests to the generic Mailbox interface. Those requests are in turn serviced by the processor with some nominal latency and the result is deposited in the mailbox for reading. MbxGet() is used to retrieve the response and details are documented in Section 6.3.2.8.

The details of processor mailbox capabilities are described in Section 6.3.2.6.1, and many of the fundamental concepts of Mailbox ownership, release, and management are discussed in Section 6.3.2.9.

6.3.2.7.1 Write Data

Regardless of the function of the mailbox command, a request type modifier and 4-byte data payload must be sent. For Mailbox commands where the 4-byte data field is not applicable (for example, the command is a read), the data written should be all zeroes.

Figure 6-19. MbxSend() Command Data Format



Because a particular MbxSend() command may specify an update to potentially critical registers inside the processor, it includes an Assured Write FCS (AW FCS) byte as part of the write data payload. In the event that the AW FCS mismatches with the client-calculated FCS, the client will abort the write and will always respond with a bad Write FCS.

6.3.2.7.2 Command Format

The MbxSend() format is as follows:

Write Length: 7

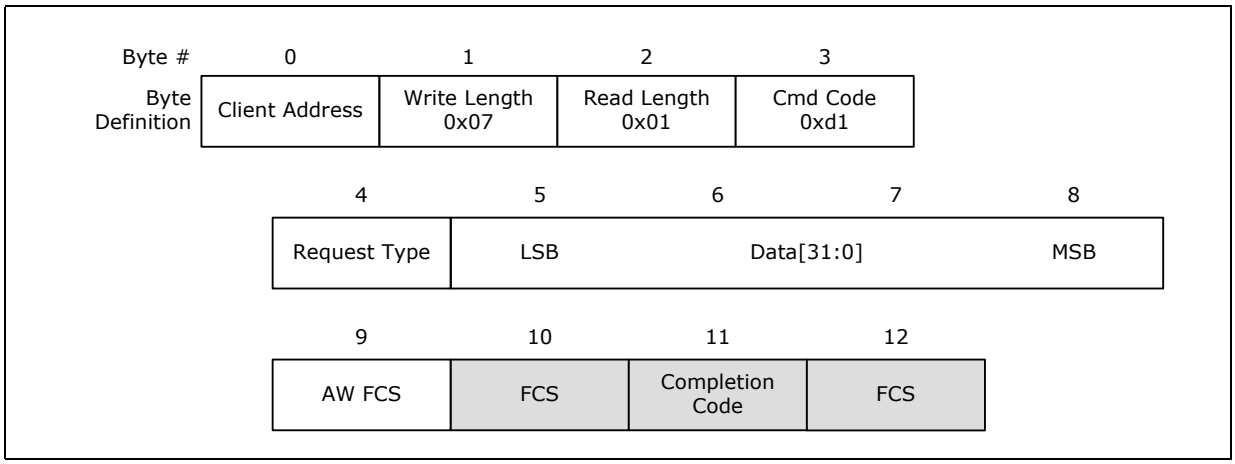
Read Length: 1

Command: 0xd1

Multi-Domain Support: Yes (see Table 6-15)

Description: Deposits the Request Type and associated 4-byte data in the Mailbox interface and returns a completion code byte with the details of the execution results. Refer to Section 6.3.4.2 for completion code definitions.

Figure 6-20. MbxSend()



Note that the 4-byte data defined above is sent in standard PECI ordering with LSB first and MSB last.

Table 6-12. MbxSend() Response Definition

Response	Meaning
Bad FCS	Electrical error
CC: 0x4X	Semaphore is granted with a Transaction ID of 'X'
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
CC: 0x86	Mailbox interface is unavailable or busy

If the MbxSend() response returns a bad Read FCS, the completion code can't be trusted and the semaphore may or may not be taken. In order to clean out the interface, an MbxGet() must be issued and the response data should be discarded.

6.3.2.8 MbxGet()

The MbxGet() command is utilized for retrieving response data from the generic Mailbox interface as well as for unlocking the acquired mailbox. Please refer to Section 6.3.2.7 for details regarding the MbxSend() command. Many of the fundamental concepts of Mailbox ownership, release, and management are discussed in Section 6.3.2.9.

6.3.2.8.1 Write Data

The MbxGet() command is designed to retrieve response data from a previously deposited request. In order to guarantee alignment between the temporally separated request (MbxSend) and response (MbxGet) commands, the originally granted Transaction ID (sent as part of the passing MbxSend() completion code) must be issued as part of the MbxGet() request.

Any mailbox request made with an illegal or unlocked Transaction ID will get a failed completion code response. If the Transaction ID matches an outstanding transaction ID associated with a locked mailbox, the command will complete successfully and the response data will be returned to the originator.

Unlike MbxSend(), no Assured Write protocol is necessary for this command because this is a read-only function.

6.3.2.8.2 Command Format

The MbxGet() format is as follows:

Write Length: 2

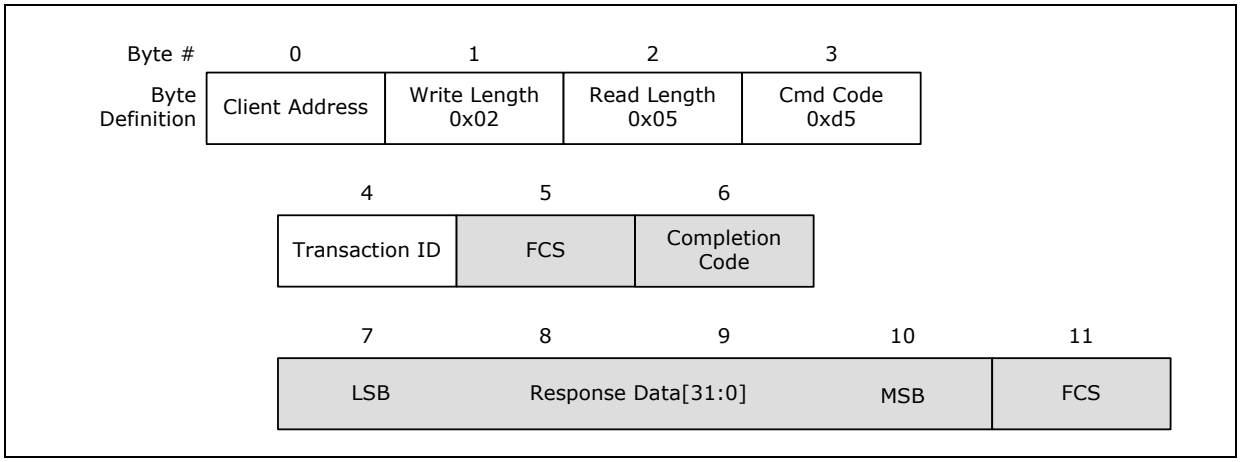
Read Length: 5

Command: 0xd5

Multi-Domain Support: Yes (see Table 6-15)

Description: Retrieves response data from mailbox and unlocks / releases that mailbox resource.

Figure 6-21. MbxGet()



Note that the 4-byte data response defined above is sent in standard PECI ordering with LSB first and MSB last.

Table 6-13. MbxGet() Response Definition

Response	Meaning
Aborted Write FCS	Response data is not ready. Command retry is appropriate.
CC: 0x40	Command passed, data is valid
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
CC: 0x81	Thermal configuration data was malformed or exceeded limits.
CC: 0x82	Thermal status mask is illegal
CC: 0x83	Invalid counter select
CC: 0x84	Invalid Machine Check Bank or Index

Table 6-13. MbxGet() Response Definition

Response	Meaning
CC: 0x85	Failure due to lack of Mailbox lock or invalid Transaction ID
CC: 0x86	Mailbox interface is unavailable or busy
CC: 0xFF	Unknown/Invalid Mailbox Request

6.3.2.9 Mailbox Usage Definition

6.3.2.9.1 Acquiring the Mailbox

The MbxSend() command is used to acquire control of the PECI mailbox and issue information regarding the specific request. The completion code response indicates whether or not the originator has acquired a lock on the mailbox, and that completion code always specifies the Transaction ID associated with that lock (see Section 6.3.2.9.2).

Once a mailbox has been acquired by an originating agent, future requests to acquire that mailbox will be denied with an 'interface busy' completion code response.

The lock on a mailbox is not achieved until the last bit of the MbxSend() Read FCS is transferred (in other words, it is not committed until the command completes). If the host aborts the command at any time prior to that bit transmission, the mailbox lock will be lost and it will remain available for any other agent to take control.

6.3.2.9.2 Transaction ID

For all MbxSend() commands that complete successfully, the passing completion code (0x4X) includes a 4-bit Transaction ID ('X'). That ID is the key to the mailbox and must be sent when retrieving response data and releasing the lock by using the MbxGet() command.

The Transaction ID is generated internally by the processor and has no relationship to the originator of the request. On Intel Xeon Processor E7-8800/4800/2800 Product Families processors, only a single outstanding Transaction ID is supported. Therefore, it is recommended that all devices requesting actions or data from the Mailbox complete their requests and release their semaphore in a timely manner.

In order to accommodate future designs, software or hardware utilizing the PECI mailbox must be capable of supporting Transaction IDs between 0 and 15.

6.3.2.9.3 Releasing the Mailbox

The mailbox associated with a particular Transaction ID is only unlocked / released upon successful transmission of the last bit of the Read FCS. If the originator aborts the transaction prior to transmission of this bit (presumably due to an FCS failure), the semaphore is maintained and the MbxGet() command may be retried.

6.3.2.9.4 Mailbox Timeouts

The mailbox is a shared resource that can result in artificial bandwidth conflicts among multiple querying processes that are sharing the same originator interface. The interface response time is quick, and with rare exception, back to back MbxSend() and MbxGet() commands should result in successful execution of the request and release of the mailbox. In order to guarantee timely retrieval of response data and mailbox release, the mailbox semaphore has a timeout policy. If the PECI bus has a cumulative '0 time of 1ms since the semaphore was acquired, the semaphore is automatically

cleared. In the event that this timeout occurs, the originating agent will receive a failed completion code upon issuing a MbxGet() command, or even worse, it may receive corrupt data if this MbxGet() command so happens to be interleaved with an MbxSend() from another process. Please refer to Table 6-13 for more information regarding failed completion codes from MbxGet() commands.

Timeouts are undesirable, and the best way to avoid them and guarantee valid data is for the originating agent to always issue MbxGet() commands immediately following MbxSend() commands.

Alternately, mailbox timeout can be disabled. The BIOS may write MSR MISC_POWER_MGMT (0x1AA), bit 11 to 0b1 in order to force a disable of this automatic timeout.

6.3.2.9.5 Response Latency

The PECI mailbox interface is designed to have response data available within plenty of margin to allow for back-to-back MbxSend() and MbxGet() requests. However, under rare circumstances that are out of the scope of this specification, it is possible that the response data is not available when the MbxGet() command is issued. Under these circumstances, the MbxGet() command will respond with an Abort FCS and the originator should re-issue the MbxGet() request.

6.3.3 Multi-Domain Commands

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor does not support multiple domains, but it is possible that future products will, and the following tables are included as a reference for domain-specific definitions.

Table 6-14. Domain ID Definition

Domain ID	Domain Number
0b01	0
0b10	1

Table 6-15. Multi-Domain Command Code Reference

Command Name	Domain 0 Code	Domain 1 Code
GetTemp()	0x01	0x02
PCIConfigRd()	0xC1	0xC2
PCIConfigWr()	0xC5	0xC6
MbxSend()	0xD1	0xD2
MbxGet()	0xD5	0xD6

6.3.4 Client Responses

6.3.4.1 Abort FCS

The Client responds with an Abort FCS under the following conditions:

- The decoded command is not understood or not supported on this processor (this includes good command codes with bad Read Length or Write Length bytes).
- Data is not ready.

- Assured Write FCS (AW FCS) failure. Note that under most circumstances, an Assured Write failure will appear as a bad FCS. However, when an originator issues a poorly formatted command with a miscalculated AW FCS, the client will intentionally abort the FCS in order to guarantee originator notification.

6.3.4.2 Completion Codes

Some PECI commands respond with a completion code byte. These codes are designed to communicate the pass/fail status of the command and also provide more detailed information regarding the class of pass or fail. For all commands listed in Section 6.3.2 that support completion codes, each command's completion codes is listed in its respective section. What follows are some generalizations regarding completion codes.

An originator that is decoding these commands can apply a simple mask to determine pass or fail. Bit 7 is always set on a failed command, and is cleared on a passing command.

Table 6-16. Completion Code Pass/Fail Mask

0xxx xxxxb	Command passed
1xxx xxxxb	Command failed

Table 6-17. Device Specific Completion Code (CC) Definition

Completion Code	Description
0x00..0x3F	Device specific pass code
0x40	Command Passed
0x4X	Command passed with a transaction ID of 'X' (0x40 | Transaction_ID[3:0])
0x50..0x7F	Device specific pass code
CC: 0x80	Error causing a response timeout. Either due to a rare, internal timing condition or a processor RESET condition or processor S1 state. Retry is appropriate outside of the RESET or S1 states.
CC: 0x81	Thermal configuration data was malformed or exceeded limits.
CC: 0x82	Thermal status mask is illegal
CC: 0x83	Invalid counter select
CC: 0x84	Invalid Machine Check Bank or Index
CC: 0x85	Failure due to lack of Mailbox lock or invalid Transaction ID
CC: 0x86	Mailbox interface is unavailable or busy
CC:0xFF	Unknown/Invalid Mailbox Request

Note: The codes explicitly defined in this table may be useful in PECI originator response algorithms. All reserved or undefined codes may be generated by a PECI client device, and the originating agent must be capable of tolerating any code. The Pass/Fail mask defined in Table 6-16 applies to all codes and general response policies may be based on that limited information.

6.3.5 Originator Responses

The simplest policy that an originator may employ in response to receipt of a failing completion code is to retry the request. However, certain completion codes or FCS responses are indicative of an error in command encoding and a retry will not result in a different response from the client. Furthermore, the message originator must have a response policy in the event of successive failure responses.

Refer to the definition of each command in Section 6.3.2 for a specific definition of possible command codes or FCS responses for a given command. The following response policy definition is generic, and more advanced response policies may be employed at the discretion of the originator developer.

Table 6-18. Originator Response Guidelines

Response	After 1 Attempt	After 3 attempts
Bad FCS	Retry	Fail with PECI client device error
Abort FCS	Retry	Fail with PECI client device error. May be due to illegal command codes.
CC: Fail	Retry	Either the PECI client doesn't support the current command code, or it has failed in its attempts to construct a response.
None (all 0's)	Force bus idle (1ms low), retry	Fail with PECI client device error. Client may be dead or otherwise non-responsive (in RESET or S1, for example).
CC: Pass	Pass	n/a
Good FCS	Pass	n/a

6.3.6 Temperature Data

6.3.6.1 Format

The temperature is formatted in a 16-bit, 2's complement value representing a number of 1/64 degrees centigrade. This format allows temperatures in a range of ±512°C to be reported to approximately a 0.016°C resolution.

Figure 6-22. Temperature Sensor Data Format

MSB Upper nibble					MSB Lower nibble					LSB Upper nibble					LSB Lower nibble			
S	x	x	x		x	x	x	x		x	x	x	x		x	x	x	x
Sign	Integer Value (0-511)											Fractional Value (~0.016)						

6.3.6.2 Interpretation

The resolution of the processor's Digital Thermal Sensor (DTS) is approximately 1°C, which can be confirmed by a RDMSR from IA32_THERM_STATUS MSR (0x19C) where it is architecturally defined. PECI temperatures are sent through a configurable low-pass filter prior to delivery in the GetTemp() response data. The output of this filter produces temperatures at the full 1/64°C resolution even though the DTS itself is not this accurate.

Temperature readings from the processor are always negative in a 2's complement format, and imply an offset from the reference TCC activation temperature. As an example, assume that the TCC activation temperature reference is 100°C. A PECI thermal reading of -10 indicates that the processor is running approximately 10°C below the TCC activation temperature, or 90°C. PECI temperature readings are not reliable at temperatures above TCC activation (since the processor is operating out of specification at this temperature). Therefore, the readings are never positive.

6.3.6.3 Temperature Filtering

The processor digital thermal sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. Coupled with the fact that typical fan speed controllers may only read temperatures at 4 Hz, it is necessary for the thermal readings to reflect thermal

trends and not instantaneous readings. Therefore, PECI supports a configurable low-pass temperature filtering function. By default, this filter results in a thermal reading that is a moving average of 256 samples taken at approximately 1msec intervals. This filter's depth, or smoothing factor, may be configured to between 1 sample and 1024 samples, in powers of 2. See the following equation for reference where the configurable variable is 'X'.

$$T_N = T_{N-1} + 1/2^X * (T_{SAMPLE} - T_{N-1})$$

Refer to Section 6.3.2.6.6 for the definition of the thermal configuration command.

6.3.6.4 Reserved Values

Several values well out of the operational range are reserved to signal temperature sensor errors. These are summarized in the following table:

Table 6-19. Error Codes and Descriptions

Error Code	Description
0x8000	General Sensor Error (GSE)

6.3.7 Client Management

6.3.7.1 Power-up Sequencing

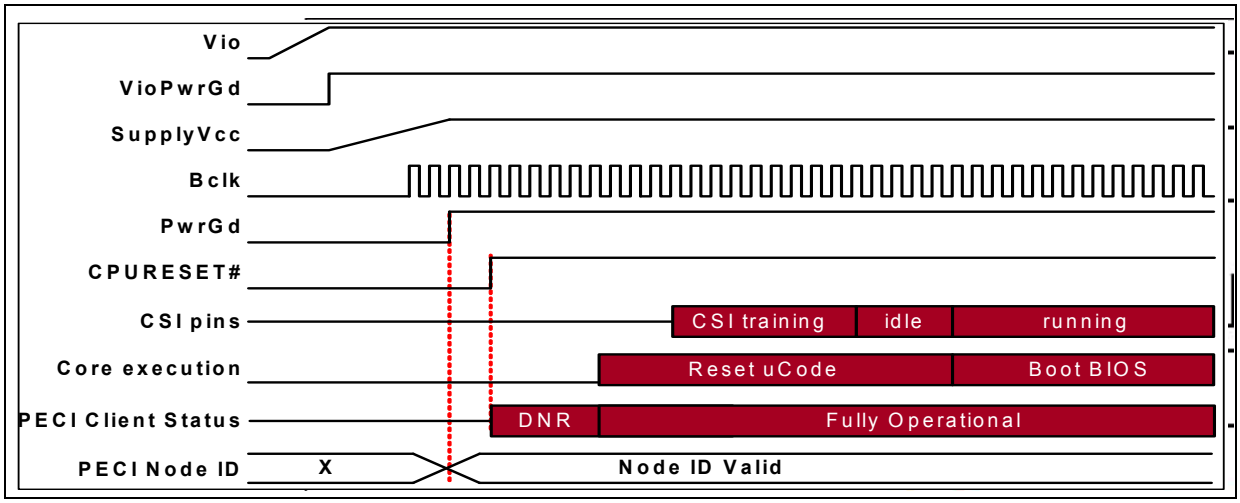
The PECI client is fully reset during processor RESET_N assertion. This means that any transactions on the bus will be completely ignored, and the host will read the response from the client as all zeroes. After processor RESET_N deassertion, the Intel Xeon Processor E7-8800/4800/2800 Product Families processor PECI client is operational enough to participate in timing negotiations and respond with reasonable data. However, the client data is not guaranteed to be fully populated until approximately 500 µS after processor RESET_N is deasserted. Until that time, data may not be ready for all commands. Note that PECI commands may time out frequently during boot. The client responses to each command are as follows:

Table 6-20. PECI Client Response During Power-Up (During 'Data Not Ready')

Command	Response
Ping()	Fully functional
GetDIB()	Fully functional
GetTemp()	Client responds with a 'hot' reading, or 0x0000
PCIConfigRd()	Fully functional
PCIConfigWr()	Fully functional
MbxSend()	Fully functional
MbxGet()	Client responds with Abort FCS (if MbxSend() has been previously issued)

In the event that the processor is tri-stated using power-on-configuration controls, the PECI client will also be tri-stated. Processor tri-state controls are described in Chapter 7.

Figure 6-23. PECI Power-up Timeline



6.3.7.2 Device Discovery

The PECI client is available on all processors, and positive identification of the PECI revision number can be achieved by issuing the GetDIB() command. Please refer to Section 6.3.2.2 for details on GetDIB response formatting.

6.3.7.3 Client Addressing

The PECI client assumes a default base address of 0x30. There are three SKT_ID# strapping pins that are used to strap each PECI socket to a different node ID (in addition to defining the processor's socket ID). Since SKT_ID# is active low, strapping a pin to ground results in value of 1 for that bit of the client ID, and strapping to Vio results in a value of 0 for that bit. The Intel Xeon processor 7500 series client addresses can therefore be strapped for values 0x30 through 0x37. These package pin straps are evaluated at the assertion of VCCPWRGOOD.

The client address may not be changed after VCCPWRGOOD assertion, until the next power cycle on the processor. Removal of a processor from its socket or tri-stating a processor in a MP configuration will have no impact to the remaining non-tri-stated PECI client address.

6.3.7.4 C-States

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor PECI client is fully functional under all core and package C-states. Support for package C-states is a function of processor SKU and platform capabilities.

Because the Intel Xeon Processor E7-8800/4800/2800 Product Families processor takes aggressive power savings actions under the deepest C-states, PECI requests may have an impact to platform power. The impact is documented below:

- Ping(), GetDIB(), GetTemp() and MbxGet() have no measurable impact on processor power under C-states.
- MbxSend(), PCIConfigRd() and PCIConfigWr() usage under package C-states may result in increased power consumption because the processor must temporarily return to a C0 state in order to execute the request. The exact power impact of a

pop-up to C0 varies by product SKU, the C-state from which the pop-up is initiated, and the negotiated T_{BIT}.

Table 6-21. Power Impact of PECI Commands vs. C-states

Command	Power Impact
Ping()	Not measurable
GetDIB()	Not measurable
GetTemp()	Not measurable
PCIConfigRd()	Requires a package 'pop-up' to a C0 state
PCIConfigWr()	Requires a package 'pop-up' to a C0 state
MbxSend()	Requires a package 'pop-up' to a C0 state
MbxGet()	Not measurable

6.3.7.5 S-States

The PECI client is always guaranteed to be operational under S0 and S1 sleep states. Under S3 and deeper sleep states, the PECI client response is undefined and, therefore, unreliable.

Table 6-22. PECI Client Response During S1

Command	Response
Ping()	Fully functional
GetDIB()	Fully functional
GetTemp()	Fully functional
PCIConfigRd()	Fully functional
PCIConfigWr()	Fully functional
MbxSend()	Fully functional
MbxGet()	Fully functional

6.3.7.6 Processor Reset

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor PECI client is fully reset on all RESET_N assertions. Upon deassertion of RESET_N, where power is maintained to the processor (otherwise known as a 'warm reset'), the following are true:

- The PECI client assumes a bus Idle state.
- The Thermal Filtering Constant is retained.
- The GetTemp() reading resets to 0x0000.
- Any transaction in progress is aborted by the client (as measured by the client no longer participating in the response).
- The processor client is otherwise reset to a default configuration.

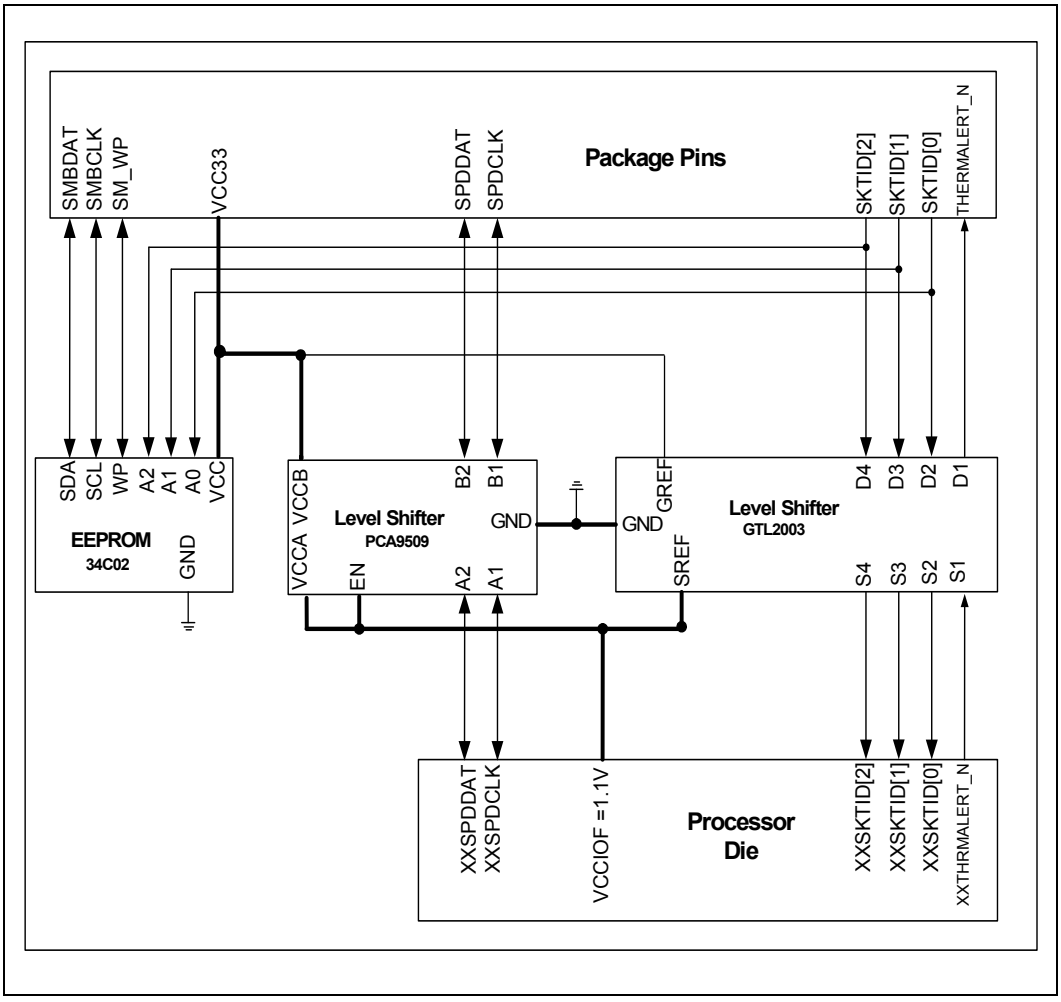
§

7 Features

7.1 Introduction

The Intel Xeon Processor E7-8800/4800/2800 Product Families processor package includes PECI 2.0, TAP and SMBus interfaces which allow access to processor's package information. The processor die is connected to the PECI2.0 and TAP, and these interfaces can be used for access to the configuration registers of the processor. The processor Information ROM (PIROM) and scratch EEROM, are accessed via the SMBus connection.

Figure 7-1. Logical Schematic of Intel® Xeon® Processor E7-8800/4800/2800 Product Families Package



Note: Actual implementation may vary. This figure is provided to offer a general understanding of the architecture.

7.2 Clock Control and Low Power States

The processor supports low power states at the individual thread, core, and package level for optimal power management.

7.2.1 Processor C-State Power Specifications

Table 7-1 lists C-State power specifications for various Intel Xeon Processor E7-8800/4800/2800 Product Families processor SKUs.

Table 7-1. Processor C-State Power Specifications

Package C-State[1]	Intel Xeon Processor E7-8800/4800/2800 Product Families processor 130W	Intel Xeon Processor E7-8800/4800/2800 Product Families processor 105W	Intel Xeon Processor E7-8800/4800/2800 Product Families processor 95W
C1E	56	54	54
C3	36	35	35
C6	31	29	29

Notes:

1. Values are with all cores in the specified C-State.

7.3 Sideband Access to Processor Information ROM via SMBus

7.3.1 Processor Information ROM

Offset/ Section	# of Bits	Function	Notes	Examples
Header				
00h	8	Data Format Revision	Two 4-bit hex digits	Start with 00h
01-02h	16	PIROM Size	Size in bytes (MSB first)	Use a decimal to hex transfer; 128 bytes = 0080h:
03h	8	Processor Data Address	Byte pointer, 00h if not present	0Eh
04h	8	Processor Core Data Address	Byte pointer, 00h if not present	1Bh
05h	8	Processor Uncore Data Address	Byte pointer, 00h if not present	2A
06h	8	Package Data Address	Byte pointer, 00h if not present	4Ch
07h	8	Part Number Data Address	Byte pointer, 00h if not present	54h
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present	66h
09h	8	Feature Data Address	Byte pointer, 00h if not present	6Ch
0Ah	8	Other Data Address	Byte pointer, 00h if not present	77h
0B-0Ch	16	Reserved	Reserved for future use	0000h
0Dh	8	Checksum	1 byte checksum	Add up by byte and take 2's complement
Processor Data				
0E-13h	48	S-spec Number	Six 8-bit ASCII characters	
14h	7/1	Sample/Production	First seven bits reserved	0b = Sample, 1b = Production 00000001 = production
15	6 2	Number of Cores Number of Threads	[7:2] = Number of cores [1:0] = Threads per core	00100010 = 8 cores with 2 threads each
16-17h	16	System Bus Speed	Four 4-bit hex digits (Mhz)	0133h = 133 MHz[1]
18-19	16	Reserved	Reserved for future use	0000h

Offset/ Section	# of Bits	Function	Notes	Examples
1Ah	8	Checksum	1 byte checksum	Add up by byte and take 2's complement
Processor Core Data				
1B-1Ch	16	CPUID	Four 4-bit hex digits	
1D-1Eh	16	Reserved	Reserved for future use	0000h
1F-20h	16	Maximum P1 Core Frequency	Non-Turbo Boost (Mhz) Four 4-bit hex digits (Mhz)	2000h = 2000 MHz[1]
21-22h	16	Maximum P0 Core Frequency	Turbo Boost (Mhz) Four 4-bit hex digits (Mhz)	2400h = 2400 MHz[1]
23-24h	16	Maximum Core Voltage ID	Four 4-bit hex digits (mV)	1500h = 1500 mV[1]
25-26h	16	Minimum Core Voltage ID	Four 4-bit hex digits (mV)	1000h = 1000 mV[1]
27h	8	Core Voltage Tolerance, High	Allowable positive DC shift Two 4-bit hex digits (mV)	15h = 15mV[1]
28h	8	Core Voltage Tolerance, Low	Allowable negative DC shift Two 4-bit hex digits (mV)	15h = 15mV[1]
29h	8	Checksum	1 byte checksum	Add up by byte and take 2's complement
Processor Uncore Data				
2A-2Bh	16	Maximum Intel QPI Link Transfer Rate	Four 4-bit hex digits (in MT/s)	6400h = 6400 MT/s[1] 5866h = 5866 MT/s[1]
2C-2Dh	16	Minimum Intel QPI Link Transfer Rate	Four 4-bit hex digits (in MT/s)	4800h = 4800 MT/s[1]
2E-31h	32	Intel QPI Version Number	Four 8-bit ASCII Characters	01.0
32h	7/1	Intel TXT	First seven bits reserved	00000001 = supported 00000000 = unsupported
33-34h	16	Maximum Intel SMI Transfer Rate	Four 4-bit hex digits (in MT/s)	6400h = 6400 MT/s[1] 5866h = 5866 MT/s
35-36h	16	Minimum Intel SMI Transfer Rate	Four 4-bit hex digits (in MT/s)	4800h = 4800 MT/s[1]
37-38h	16	VIO Voltage ID	Four 4-bit hex digits (mV)	1125h = 1125 mV[1]
39h	8	VIO Voltage Tolerance, High	Edge finger tolerance Two 4-bit hex digits (mV)	15h = 15 mV[1]
3Ah	8	VIO Voltage Tolerance, Low	Edge finger tolerance Two 4-bit hex digits (mV)	15h = 15 mV[1]
3B-3Eh	32	Reserved	Reserved for future use	00000000h
3F-40h	16	L2 Cache Size	Decimal (Kb) Per CPU Core	0100h = 256 Kb
41-42h	16	L3 Cache Size	Decimal (Kb)	6000h = 24576 Kb, 4800h = 18432 Kb, 3000h = 12288 Kb
43-44	16	Cache Voltage ID	Four 4-bit hex digits (mV)	1500h = 1500 mV[1]
45h	8	Cache Voltage Tolerance, High	Allowable positive DC shift Two 4-bit hex digits (mV)	15h = 15 mV[1]
46h	8	Cache Voltage Tolerance, Low	Allowable negative DC shift Two 4-bit hex digits (mV)	15h = 15 mV[1]
47-4Ah	32	Reserved	Reserved for future use	00000000h
4Bh	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.
Package				
4C-4Fh	32	Package Revision	Four 8-bit ASCII characters	01.0
50h	6/2	Substrate Revision Software ID	First 6 bits reserved	000000**
51-52h	16	Reserved	Reserved for future use	0000h
53h	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.

Offset/ Section	# of Bits	Function	Notes	Examples
Part Numbers				
54-5Ah	56	Processor Family Number	Seven 8-bit ASCII characters	AT80604
5B-62h	64	Processor SKU Number	Seven 8-bit ASCII characters	003771AA
63-64h	16	Reserved	Reserved for future use	0000h
65h	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.
Thermal Reference				
66h	8	Recommended THERMALERT_N assertion threshold value	MSB is Reserved	0h = 0C[1]
67h	8	Thermal calibration offset value	MSB is Reserved	0h = 0C[1]
68h	8	T_{CASE} Maximum	Maximum case temperature Two 4-bit hex digits (mV)	69h = 69°C[1]
69-6Ah	16	Thermal Design Power	Four 4-bit hex digits (in Watts)	0130h = 130 Watts[1]
6Bh	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.
Features				
6C-6Fh	32	Processor Core Feature Flags	From CPUID function 1, EDX contents	4387FBFFh
70h	8	Processor Feature Flags	Eight features - Binary 1 indicates functional feature	10001101
71h	8	Additional Processor Feature Flags	Eight additional features - Binary 1 indicates functional feature	01110101
72	6/2	Multiprocessor Support	00b = UP, 01b = DP, 10b = S2S, 11b = MP/SMS	00000011 = MP/SMS
73h	4/4	Number of Devices in TAP Chain	First four bits reserved One 4-bit hex digit - Bits	*0h[1]
74-75h	16	Reserved	Reserved for future use	0000h
76h	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.
Other				
77-7Eh	64	Processor Serial/Electronic Signature	Coded binary	N/A
7Fh	8	Checksum	1 byte checksum	Add up by byte and take 2's complement.

Notes:

1. Uses Binary Coded Decimal (BCD) translation.

7.3.2 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 kΩ) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected by Intel.

7.3.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The PIROM responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. Table 7-2 illustrates the Read Byte command. Table 7-3 illustrates the Write Byte command.

In the tables, 'S' represents a SMBus start bit, 'P' represents a stop bit, 'A' represents an acknowledge (ACK), and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the PIROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits.

The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the PIROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

Table 7-2. Read Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	S	Slave Address	Read	A	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 7-3. Write Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	Data	A	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

7.4 SMBus Memory Component Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form "10100XXZb". The "XX" bits are defined by pull-up and pull-down of the SKTID[1:0] pins. Note that SKTID[2] does not affect the SMBus address for the memory component. These address pins are pulled down weakly (10 k) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus (or only support a partial implementation). The "Z" bit is the read/write bit for the serial bus transaction.

Note that addresses of the form "0000XXXXb" are Reserved and should not be generated by an SMBus master.

Table 7-4 describes the address pin connections and how they affect the addressing of the memory component.

Table 7-4. Memory Device SMBus Addressing

Address (Hex)	Upper Address[1]	Device Select			R/W
	Bits 7-4	SKTID[2]	SKTID[1] Bit 2	SKTID[0] Bit 1	Bit 0
A0h/A1h	10100	10100	0	0	X
A2h/A3h	10100	10100	0	1	X
A4h/A5h	10100	10100	1	0	X
A6h/A7h	10100	10100	1	1	X

Note:
1. This addressing scheme will support up to 4 processors on a single SMBus.

7.5 Managing Data in the PIROM

The PIROM consists of the following sections:

- Header
- Processor Data
- Processor Core Data
- Processor Uncore Data
- Cache Data
- Package Data
- Part Number Data
- Thermal Reference Data
- Feature Data
- Other Data

Details on each of these sections are described below.

Note: Reserved fields or bits SHOULD be programmed to zeros. However, OEMs should not rely on this model.

7.5.1 Header

To maintain backward compatibility, the Header defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

Example: Code looking for the processor uncore data of a processor would read offset 05h to find a value of 29. 29 is the first address within the 'Processor Uncore Data' section of the PIROM.

7.5.1.1 DFR: Data Format Revision

This location identifies the data format revision of the PIROM data structure. Writes to this register have no effect.

Offset:	00h
Bit	**Description**
7:0	**Data Format Revision** The data format revision is used whenever fields within the PIROM are redefined. The initial definition will begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field will be incremented. 00h: Reserved 01h: Initial definition 02h: Second revision 03h: Third revision 04h: Fourth revision 05h:Fifth revision *(Defined by this document)* 06h-FFh: Reserved

7.5.1.2 PISIZE: PIROM Size

This location identifies the PIROM size. Writes to this register have no effect.

Offset:	01h-02h
Bit	**Description**
15:0	**PIROM Size** The PIROM size provides the size of the device in hex bytes. The MSB is at location 01h; the LSB is at location 02h. 0000h - 007Fh: Reserved 0080h: 128 byte PIROM size 0081- FFFFh: Reserved

7.5.1.3 PDA: Processor Data Address

This location provides the offset to the Processor Data Section. Writes to this register have no effect.

Offset:	03h
Bit	**Description**
7:0	**Processor Data Address** Byte pointer to the Processor Data section 00h: Processor Data section not present 01h - 0Dh: Reserved 0Eh: Processor Data section pointer value 0Fh-FFh: Reserved

7.5.1.4 PCDA: Processor Core Data Address

This location provides the offset to the Processor Core Data Section. Writes to this register have no effect.

Offset: 04h	
Bit	**Description**
7:0	**Processor Core Data Address** Byte pointer to the Processor Core Data section 00h: Processor Core Data section not present 01h - 09h: Reserved 1Ah: Processor Core Data section pointer value 1Bh-FFh: Reserved

7.5.1.5 PUDA: Processor Uncore Data Address

This location provides the offset to the Processor Uncore Data Section. Writes to this register have no effect.

Offset: 05h	
Bit	**Description**
7:0	**Processor Uncore Data Address** Byte pointer to the Processor Uncore Data section 00h: Processor Uncore Data section not present 01h - 28h: Reserved 29h: Processor Uncore Data section pointer value 2Ah-FFh: Reserved

7.5.1.6 PDA: Package Data Address

This location provides the offset to the Package Data Section. Writes to this register have no effect.

Offset: 06h	
Bit	**Description**
7:0	**Package Data Address** Byte pointer to the Package Data section 00h: Package Data section not present 01h - 4Ah: Reserved 4Bh: Package Data section pointer value 4Ch-FFh: Reserved

7.5.1.7 PNDA: Part Number Data Address

This location provides the offset to the Part Number Data Section. Writes to this register have no effect.

Offset: 07h	
Bit	**Description**
7:0	**Part Number Data Address** Byte pointer to the Part Number Data section 00h: Part Number Data section not present 01h - 52h: Reserved 53h: Part Number Data section pointer value 54h-FFh: Reserved

7.5.1.8 TRDA: Thermal Reference Data Address

This location provides the offset to the Thermal Reference Data Section. Writes to this register have no effect.

Offset: 08h	
Bit	**Description**
7:0	**Thermal Reference Data Address** Byte pointer to the Thermal Reference Data section 00h: Thermal Reference Data section not present 01h - 64h: Reserved 65h: Thermal Reference Data section pointer value 66h-FFh: Reserved

7.5.1.9 FDA: Feature Data Address

This location provides the offset to the Feature Data Section. Writes to this register have no effect.

Offset: 09h	
Bit	**Description**
7:0	**Feature Data Address** Byte pointer to the Feature Data section 00h: Feature Data section not present 01h - 6Ah: Reserved 6Bh: Feature Data section pointer value 6Ch-FFh: Reserved

7.5.1.10 ODA: Other Data Address

This location provides the offset to the Other Data Section. Writes to this register have no effect.

Offset: 0Ah	
Bit	**Description**
7:0	**Other Data Address** Byte pointer to the Other Data section 00h: Other Data section not present 01h - 78h: Reserved 79h: Other Data section pointer value 7Ah- FFh: Reserved

7.5.1.11 RES1: Reserved 1

This location is reserved. Writes to this register have no effect.

Offset: 0Bh-0Ch	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.1.12 HCKS: Header Checksum

This location provides the checksum of the Header Section. Writes to this register have no effect.

Offset: 0Dh	
Bit	**Description**
7:0	**Header Checksum** One-byte checksum of the Header Section 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.2 Processor Data

This section contains three pieces of data:

- The S-spec of the part in ASCII format.
- (1) 2-bit field to declare if the part is a pre-production sample or a production unit.
- The system bus speed in BCD format

7.5.2.1 SQNUM: S-Spec Number

This location provides the S-Spec number of the processor. The S-spec field is six ASCII characters wide and is programmed with the same spec value as marked on the processor. If the value is less than six characters in length, leading spaces (20h) are programmed in this field. Writes to this register have no effect.

Offset: 0Eh-13h	
Bit	**Description**
47:40	**Character 6** S-Spec or 20h 00h-0FFh: ASCII character
39:32	**Character 5** S-Spec or 20h 00h-0FFh: ASCII character
31:24	**Character 4** S-Spec character 00h-0FFh: ASCII character
23:16	**Character 3** S-Spec character 00h-0FFh: ASCII character
15:8	**Character 2** S-Spec character 00h-0FFh: ASCII character
7:0	**Character 1** S-Spec character 00h-0FFh: ASCII character

7.5.2.2 SAMPROD: Sample/Production

This location contains the sample/production field, which is a two-bit field and is LSB aligned. All sample material will use a value of 00b. All S-spec material will use a value of 01b. All other values are reserved. Writes to this register have no effect.

Example: A processor with an Sxxxx mark (production unit) will use 01h at offset 14h.

Offset: 14h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**Sample/Production** Sample or Production indictor 00b: Sample 01b: Production 10b-11b: Reserved

7.5.2.3 Processor Thread and Core Information

This location contains information regarding the number of cores and threads on the processor. Writes to this register have no effect. Data format is binary.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor has up to 10 cores and two threads per core.

Offset: 15h	
Bit	**Description**
7:2	Number of cores
1:0	Number of threads per core

7.5.2.4 SBS: System Bus Speed

This location contains the system bus frequency information. Systems may need to read this offset to decide if all installed processors support the same system bus speed. The data provided is the speed, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: A processor with system buss speed of 1.066GHz will have a value of 1066h.

Offset: 16h-17h	
Bit	**Description**
15:0	**System Bus Speed** 0000h-FFFFh: MHz

7.5.2.5 RES2: Reserved 2

This location is reserved. Writes to this register have no effect.

Offset: 18h-19h	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.2.6 PDCKS: Processor Data Checksum

This location provides the checksum of the Processor Data Section. Writes to this register have no effect.

Offset: 1Ah	
Bit	**Description**
7:0	**Processor Data Checksum** One-byte checksum of the Processor Data Section 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.3 Processor Core Data

This section contains silicon-related data relevant to the processor cores.

7.5.3.1 CPUID: CPUID

This location contains the CPUID, Processor Type, Family, Model and Stepping. The CPUID field is a copy of the results in EAX[15:0] from Function 1 of the CPUID instruction. Writes to this register have no effect. Data format is hexidecimal.

Offset: 1Bh-1Ch	
Bit	**Description**
15:13	**Reserved** 00b-11b: Reserved
12:12	**Processor Type** 0b-1b: Processor Type
11:8	**Processor Family** 0h-Fh: Processor Family
7:4	**Processor Model** 0h-Fh: Processor Model
3:0	**Processor Stepping** 0h-Fh: Processor Stepping

7.5.3.2 RES3: Reserved 3

This locations are reserved. Writes to this register have no effect.

Offset: 1Dh-1Eh	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.3.3 MP1CF: Maximum P1 Core Frequency

This location contains the maximum non-Turbo Boost core frequency for the processor. The frequency should equate to the markings on the processor and/or the S-spec speed even if the parts are not limited or locked to the intended speed. Format of this field is in MHz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

Example: A 2.666 GHz processor will have a value of 2666h.

Offset: 1F-20h	
Bit	**Description**
15:0	**Maximum P1 Core Frequency** 0000h-FFFFh: MHz

7.5.3.4 MP0CF: Maximum P0 Core Frequency

This location contains the maximum Turbo Boost core frequency for the processor. This is the maximum intended speed for the part under any functional conditions. Format of this field is in MHz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

Example: A processor with a maximum Turbo Boost frequency of 2.666 GHz will have a value of 2666h.

Offset: 21h-22h	
Bit	**Description**
15:0	**Maximum P0 Core Frequency** 0000h-FFFFh: MHz

7.5.3.5 MAXVID: Maximum Core VID

This location contains the maximum Core VID (Voltage Identification) voltage that may be requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect.

Example: A voltage of 1.350 V maximum core VID would contain 1350h.

Offset: 23h-24h	
Bit	**Description**
15:0	**Maximum Core VID** 0000h-FFFFh: mV

7.5.3.6 MINVID: Minimum Core VID

This location contains the Minimum Core VID (Voltage Identification) voltage that may be requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect.

Example: A voltage of 1.000 V maximum core VID would contain 1000h.

Offset: 25h-26h	
Bit	**Description**
15:0	**Maximum Core VID** 0000h-FFFFh: mV

7.5.3.7 VTH: Core Voltage Tolerance, High

This location contains the maximum Core Voltage Tolerance DC offset high. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: 50 mV tolerance would be saved as 50h.

Offset: 27h	
Bit	**Description**
7:0	**Core Voltage Tolerance, High** 00h-FFh: mV

7.5.3.8 VTL: Core Voltage Tolerance, Low

This location contains the maximum Core Voltage Tolerance DC offset low. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: 50 mV tolerance would be saved as 50h.

Offset: 28h	
Bit	**Description**
7:0	**Core Voltage Tolerance, Low** 00h-FFh: mV

7.5.3.9 PDCKS: Processor Core Data Checksum

This location provides the checksum of the Processor Core Data Section. Writes to this register have no effect.

Offset: 29h	
Bit	**Description**
7:0	**Processor Core Data Checksum** One-byte checksum of the Processor Data Section 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.4 Processor Uncore Data

This section contains silicon-related data relevant to the processor Uncore.

7.5.4.1 MAXQPI: Maximum Intel QPI Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same Intel QPI Link Transfer Rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports a maximum Intel QPI link transfer rate of 6.4 GT/s. Therefore, offset 2Ah-2Bh has a value of 6400.

Offset: 2Ah-2Bh	
Bit	**Description**
15:0	**Maximum Intel QPI Transfer Rate** 0000h-FFFFh: MHz

7.5.4.2 MINQPI: Minimum Operating Intel QPI Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same Intel QPI Link Transfer Rate. This does not relate to the “link power up” transfer rate of 1/4th Ref Clk. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports a minimum operating Intel QPI link transfer rate of 4.8 GT/s. Therefore, offset 2Bh-2Ch has a value of 4800.

Offset: 2Ch-2Dh	
Bit	**Description**
15:0	**Minimum Intel QPI Transfer Rate** 0000h-FFFFh: MHz

7.5.4.3 QPIVN: Intel QPI Version Number

The Intel QPI Version Number is provided as four 8-bit ASCII characters. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports Intel QPI Version Number 1.0. Therefore, offset 2Eh-31h has an ASCII value of "01.0", which is 30, 31, 2E, 30.

Offset: 2Eh-31h	
Bit	**Description**
31:0	**Intel QPI Version Number** 00000000h-FFFFFFFFh: MHz

7.5.4.4 TXT: TXT

This location contains the TXT location, which is a two-bit field and is LSB aligned. A value of 00b indicates TXT is not supported. A value of 01b indicates TXT is supported. Writes to this register have no effect.

Example: A processor supporting TXT will have offset 32h set to 01h.

Offset: 32h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**TXT** TXT support indicator 00b: Not supported 01b: Supported 10b-11b: Reserved

7.5.4.5 MAXSMI: Maximum Intel SMI Transfer Rate

Systems may need to read this offset to decide on compatible processors and Intel 7500 scalable memory buffer capabilities. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports a maximum Intel SMI transfer rate of 6.4 GT/s. Therefore, offset 33h-34h has a value of 6400h.

Offset: 33h-34h	
Bit	**Description**
15:0	**Maximum Intel SMI Transfer Rate** 0000h-FFFFh: MHz

7.5.4.6 MINSMI: Minimum Intel SMI Transfer Rate

This listing provides the minimum "operating" Intel SMI transfer rate. Systems may need to read this offset to decide if processors and Intel 7500 scalable memory buffer s support the same Intel SMI Transfer Rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor supports a minimum operating Intel SMI transfer rate of 4.8 GT/s. Therefore, offset 35h-36h has a hex value of 4800h.

Offset: 35h-36h	
Bit	**Description**
15:0	**Minimum Intel SMI Transfer Rate** 0000h-FFFFh: MHz

7.5.4.7 VIOVID: VIO VID

Offset 37h-38h is the Processor VIO VID (Voltage Identification) field and contains the voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

Example: A voltage of 1.350 V maximum core VID would contain 1350h in Offset 36-37h.

Offset: 37h-38h	
Bit	**Description**
15:0	**VIO VID** 0000h-FFFFh: mV

7.5.4.8 VIOVTH: VIO Voltage Tolerance, High

Offset 39h contains the VIO voltage tolerance, high. This is the maximum voltage swing above the required voltage allowed. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: A 50 mV tolerance would be saved as 50h.

Offset: 39h	
Bit	**Description**
7:0	**VIO Voltage Tolerance, High** 00h-FFh: mV

7.5.4.9 VIOVTL: Voltage Tolerance, Low

Offset 3Ah contains the VIO voltage tolerance, low. This is the minimum voltage swing under the required voltage allowed. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: A 50 mV tolerance would be saved as 50h.

Offset: 3Ah	
Bit	**Description**
7:0	**Core Voltage Tolerance, Low** 00h-FFh: mV

7.5.4.10 RES4: Reserved 4

This location is reserved. Writes to this register have no effect.

Offset: 3Bh-3Eh	
Bit	**Description**
31:0	**RESERVED** 00000000h-FFFFFFFFh: Reserved

7.5.4.11 L2SIZE: L2 Cache Size

This location contains the size of the level-two cache in kilobytes. Writes to this register have no effect. Data format is decimal.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor has a 2.5 MB L2 cache. Thus, offset 3Fh-40h will contain a value of 0A00h.

7.5.4.12 L3SIZE: L3 Cache Size

Offset: 3Fh-40h	
Bit	**Description**
15:0	**L2 Cache Size** 0000h-FFFFh: KB

This location contains the size of the level-three cache in kilobytes. Writes to this register have no effect. Data format is decimal.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor has up to a 30 MB L3 cache. Thus, offset 41h-42h will contain a value of 8700h.

Offset: 41h-42h	
Bit	**Description**
15:0	**L3 Cache Size** 0000h-FFFFh: KB

7.5.4.13 CVID: Cache Voltage ID

This field contains the voltage requested via the CVID pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default CVID setting. Writes to this register have no effect.

Example: A voltage of 1.350 V CVID would contain an Offset 43-44h value of 1350h.

Offset: 43h-44h	
Bit	**Description**
15:0	**Cache Voltage ID** 0000h-FFFFh: mV

7.5.4.14 CVTH: Cache Voltage Tolerance, High

This location contains the maximum Cache Voltage Tolerance DC offset high. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: A 50 mV tolerance would be saved as 50h.

Offset: 45h	
Bit	**Description**
7:0	**Cache Voltage Tolerance, High** 00h-FFh: mV

7.5.4.15 CVTL: Cache Voltage Tolerance, Low

This location contains the maximum Cache Voltage Tolerance DC offset low. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: A 50 mV tolerance would be saved as 50h.

Offset: 46h	
Bit	**Description**
7:0	**Cache Voltage Tolerance, Low** 00h-FFh: mV

7.5.4.16 RES5: Reserved 5

This location is reserved. Writes to this register have no effect.

Offset: 47h-4Ah	
Bit	**Description**
31:0	**RESERVED** 00000000h-FFFFFFFFh: Reserved

7.5.4.17 PUDCKS: Processor Uncore Data Checksum

This location provides the checksum of the Processor Uncore Data Section. Writes to this register have no effect.

Offset: 4Bh	
Bit	**Description**
7:0	**Processor Uncore Data Checksum** One-byte checksum of the Processor Uncore Data Section 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.5 Package Data

This section contains substrate and other package related data.

7.5.5.1 PREV: Package Revision

This location tracks the highest level package revision. It is provided in an ASCII format of four characters (8 bits x 4 characters = 32 bits). The package is documented as 1.0, 2.0, etc. If only three ASCII characters are consumed, a leading space is provided in the data field. Writes to this register have no effect.

Example: The Intel Xeon Processor E7-8800/4800/2800 Product Families processor utilizes the first revision of the LGA-1567 package. Thus, at offset 4C-4F-35h, the data is a space followed by 1.0. In hex, this would be 20h, 31h, 2Eh, 30h.

Offset: 4Ch-4Fh	
Bit	**Description**
31:24	**Character 4** ASCII character or 20h 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

7.5.5.2 Substrate Revision Software ID

This location is a place holder for the Substrate Revision Software ID. Writes to this register have no effect.

Offset: 50h	
Bit	**Description**
7:0	**Substrate Revision Software ID** 00h-FFh: Reserved

7.5.5.3 RES6: Reserved 6

This location is reserved. Writes to this register have no effect.

Offset: 51h-52h	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.5.4 PDCKS: Package Data Checksum

This location provides the checksum of the Package Data Section. Writes to this register have no effect.

Offset: 53h	
Bit	**Description**
7:0	**Package Data Checksum** One-byte checksum of the Package Data Section 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.6 Part Number Data

This section provides device traceability.

7.5.6.1 PFN: Processor Family Number

This location contains seven ASCII characters reflecting the Intel® family number for the processor. This number is the same on all Intel Xeon Processor E7-8800/4800/2800 Product Families processors. Combined with the Processor SKU Number below, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification found in Chapter 3. Writes to this register have no effect.

Example: A processor with a part number of AT80604******** will have the following data found at offset 38-3Eh: 41h, 54h, 38h, 30h, 36h, 30h, 34h.

Offset: 54h-5Ah	
Bit	**Description**
55:48	**Character 7** ASCII character or 20h 00h-0FFh: ASCII character
47:40	**Character 6** ASCII character or 20h 00h-0FFh: ASCII character
39:32	**Character 5** ASCII character or 20h 00h-0FFh: ASCII character
31:24	**Character 4** ASCII character 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

7.5.6.2 PSN: Processor SKU Number

This location contains eight ASCII characters reflecting the Intel® SKU number for the processor. Added to the end of the Processor Family Number above, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification found in Chapter 3. Writes to this register have no effect.

Example: A processor with a part number of *******003771AA will have the following data found at offset 58-62h: 30h, 30h, 33h, 37h, 37h, 31h, 41h, 41h.

Offset: 5Bh=62h	
Bit	**Description**
63:56	**Character 8** 00h-0FFh: ASCII character
55:48	**Character 7** ASCII character or 20h 00h-0FFh: ASCII character
47:40	**Character 6** ASCII character or 20h 00h-0FFh: ASCII character
39:32	**Character 5** ASCII character or 20h 00h-0FFh: ASCII character
31:24	**Character 4** ASCII character 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

7.5.6.3 RES7: Reserved 7

This location is reserved. Writes to this register have no effect.

Offset: 63h-64h	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.6.4 PNDCKS: Part Number Data Checksum

This location provides the checksum of the Part Number Data Section. Writes to this register have no effect.

Offset: 65h	
Bit	**Description**
7:0	**Part Number Data Checksum** One-byte checksum of the Part Number Data Checksum 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.7 Thermal Reference Data

7.5.7.1 TUT: Thermalert Upper Threshold

This location is a place holder for the Thermalert Upper Threshold Byte. Writes to this register have no effect.

Offset:	66h
Bit	**Description**
7:0	**Thermalert Upper Threshold** 0000h-FFFFh: Reserved

7.5.7.2 TCO: Thermal Calibration Offset

This location is a place holder for the Thermal Calibration Offset Byte. Writes to this register have no effect.

Offset:	67h
Bit	**Description**
7:0	**Thermal Calibration Offset** 0000h-FFFFh: Reserved

7.5.7.3 TCASE: T_{CASE} Maximum

This location provides the maximum T_{CASE} for the processor. The field reflects temperature in degrees Celsius in binary coded decimal format. This data can be found in Chapter 6. The thermal specifications are specified at the case Integrated Heat Spreader (IHS). Writes to this register have no effect.

Example: A temperature of 66°C would contain a value of 66h.

Offset:	68h
Bit	**Description**
7:0	**T_{CASE} Maximum** 00h-FFh: Degrees Celsius

7.5.7.4 TDP: Thermal Design Power

This location contains the maximum Thermal Design Power for the part. The field reflects power in watts in binary coded decimal format. Writes to this register have no effect. A zero value means that the value was not programmed.

Example: A 130W TDP would be saved as 0130h.

Offset:	69h-6Ah
Bit	**Description**
15:0	**Thermal Design Power** 0000h-FFFFh: Watts

7.5.7.5 TRDCKS: Thermal Reference Data Checksum

This location provides the checksum of the Thermal Reference Data Section. Writes to this register have no effect.

Offset:	6Bh
Bit	**Description**
7:0	**Thermal Reference Data Checksum** One-byte checksum of the of Thermal Reference Data Checksum 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.8 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

7.5.8.1 PCFF: Processor Core Feature Flags

This location contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. Writes to this register have no effect.

Example: A value of BFEBFBFFh can be found at offset 6C - 6Fh.

Offset:	6Ch-6Fh
Bit	**Description**
31:0	**Processor Core Feature Flags** 00000000h-FFFFFFFFF: Feature Flags

7.5.8.2 PFF: Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.

Note: Bit 5 and Bit 6 are mutually exclusive (only one bit will be set).

Offset:	70h
Bit	**Description**
7	Multi-Core (set if the processor is a multi-core processor)
6	Serial signature (set if there is a serial signature at offset 5B- 62h)
5	Electronic signature present (set if there is a electronic signature at 5B- 62h)
4	Thermal Sense Device present (set if an SMBus thermal sensor is on package)
3	Reserved
2	OEM EEPROM present (set if there is a scratch ROM at offset 80 - FFh)
1	Core VID present (set if there is a VID provided by the processor)
0	L3 Cache present (set if there is a level-3 cache on the processor)

Bits are set when a feature is present, and cleared when they are not.

7.5.8.3 APFF: Additional Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.

Offset: 71h	
Bit	**Description**
7	Reserved
6	Intel® Cache Safe Technology
5	Extended Halt State (C1E)
4	Intel® Virtualization Technology
3	Execute Disable
2	Intel® 64
1	Intel® Thermal Monitor 2
0	Enhanced Intel SpeedStep® Technology

Bits are set when a feature is present, and cleared when they are not.

7.5.8.4 MPSUP: Multiprocessor Support

This location contains 2 bits for representing the supported number of physical processors on the bus. These two bits are LSB aligned where 00b equates to non-scalable 2 socket (2S) operation, 01b to scalable 2 socket (S2S), 10 to scalable 4 socket (S4S), and scalable 8 socket (S8S). Intel Xeon Processor E7-8800/4800/2800 Product Families processor is a S2S, S4S, or S8S processor. The first six bits in this field are reserved for future use. Writes to this register have no effect.

Example: A scalable 8 socket processor will have a value of 03h at offset 71h.

Offset: 72h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**Multiprocessor Support** 2S, S2S, S4S or S8S indicator 00b: Non-Scalable 2 Socket 01b: Scalable 2 Socket 10b: Scalable 4 Socket 11b: Scalable 8 Socket

7.5.8.5 TCDC: Tap Chain Device Count

At offset 73, a 4-bit hex digit is used to tell how many devices are in the TAP Chain. Because the Intel Xeon Processor E7-8800/4800/2800 Product Families processor has ten cores, this field would be set to Ah.

Offset:	73h
Bit	**Description**
7:0	**TAP Chain Device Count** 0000h-FFFFh: Reserved

7.5.8.6 RES9: Reserved 9

This location is reserved. Writes to this register have no effect.

Offset:	74h-75h
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

7.5.8.7 TRDCKS: Thermal Reference Data Checksum

This location provides the checksum of the Thermal Reference Data Section. Writes to this register have no effect.

Offset:	76h
Bit	**Description**
7:0	**Thermal Reference Data Checksum** One-byte checksum of the Thermal Reference Data Checksum 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.9 Other Data

This section contains a large reserved area, and items added after the original format for the Intel Xeon Processor E7-8800/4800/2800 Product Families processor PIROM was set.

7.5.9.1 PS/ESIG: Processor Serial/Electronic Signature

This location contains a 64-bit identification number. The value in this field is either a serial signature or an electronic signature. Writes to this register have no effect.

Offset:	77h-7Eh
Bit	**Description**
63:0	**Processor Serial/Electronic Signature** 0000000000000000h-FFFFFFFFFFFFFFFFh: Electronic Signature

7.5.9.2 ODCKS: Other Data Checksum

This location provides the checksum for the Other Data Section. Writes to this register have no effect.

Offset: 7Fh	
Bit	**Description**
7:0	**Other Data Checksum** One-byte checksum of the Other Data Checksum 00h- FFh: See Section 7.5.10 for calculation of this value.

7.5.10 Checksums

The PIROM includes multiple checksums. Table 7-5 includes the checksum values for each section defined in the 128-byte ROM.

Table 7-5. 128-Byte ROM Checksum Values

Section	Checksum Address
Header	0Dh
Processor Data	1Ah
Processor Core Data	29h
Processor Uncore Data	4Bh
Package Data	53h
Part Number Data	65h
Feature Data	76h
Other Data	7Fh

Checksums are automatically calculated and programmed by Intel®. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. This result is then negated to provide the checksum.

Example: For a byte string of AA445Ch, the resulting checksum will be B6h.

AA = 10101010 44 = 01000100 5C = 0101100

AA + 44 + 5C = 01001010

Negate the sum: 10110101 +1 = **101101 (B6h)**

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8 Debug Tools Specifications

For debug purposes, the socket LS pin definition has allocated signals to install a logic analyzer probe head to observe Intel QPI traffic.

8.1 Logic Analyzer Interface

Due to the complexity of Intel Xeon Processor E7-8800/4800/2800 Product Families processor-based multiprocessor systems, the Logic Analyzer Interface (LAI) is critical in providing the ability to probe and capture high-speed signals. There are two sets of considerations to keep in mind when designing a Intel Xeon Processor E7-8800/4800/2800 Product Families processor-based system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Intel Xeon Processor E7-8800/4800/2800 Product Families processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

Instrumented Intel QPI links will require equalization settings unique for that topology. The platform will need to load updated optimized equalization settings for instrumented links. The method of obtaining the new set of E.Q settings is via the Signal Integrity Support Tools for Advanced Interfaces (SISTAI) tools, following the same procedures.

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