HM628128/HM628128I Series

T-46-23-14

131,072-Word × 8-Bit High Speed Hi-CMOS Static RAM

■ DESCRIPTION

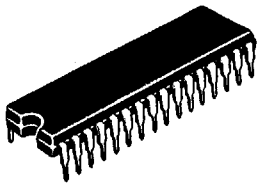
The Hitachi HM628128 is a CMOS static RAM organized 128k-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology. The HM628128I is available in industrial temperature range (−40 to +85°C).

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 8 × 20 mm TSOP with a thickness of 1.2 mm, 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, is available for high density mounting.

■ FEATURES

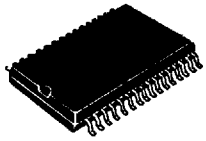
- High Speed: Fast access time .....70/85/100/120ns (max.)
- Low Power
  - Standby: .....10 μW (typ.) (L-version)
  - Operation: .....75 mW (typ.)
- Single 5V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L & SL)
  - 2 chip selection for battery back up.

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

(TFP-32DA)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

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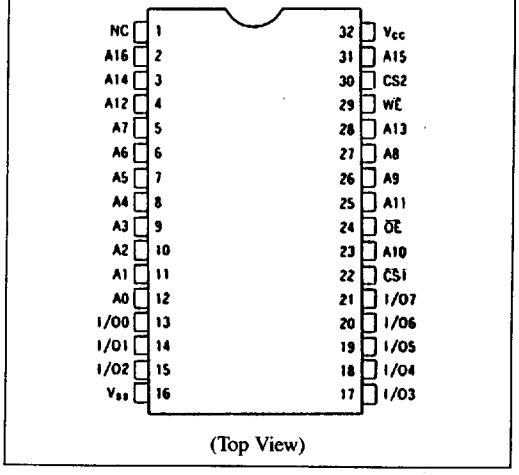
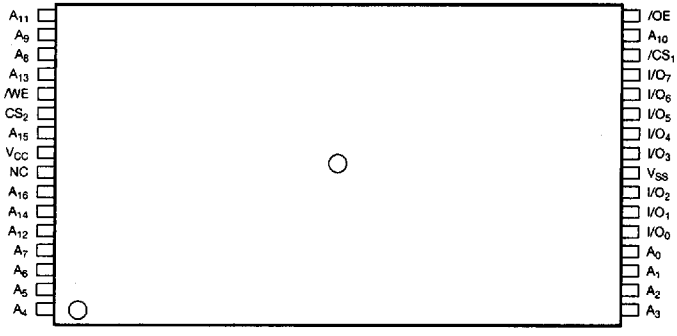
■ PIN ARRANGEMENT

(DP-32 & FP-32D)



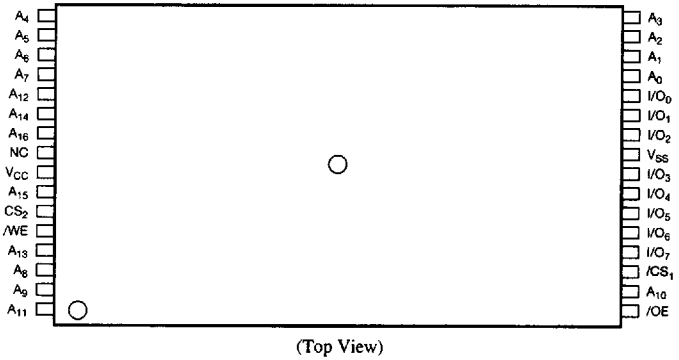
(Top View)

(TFP-32DA)



(Top View)

(TFP-32DAR)



(Top View)

Block Diagram

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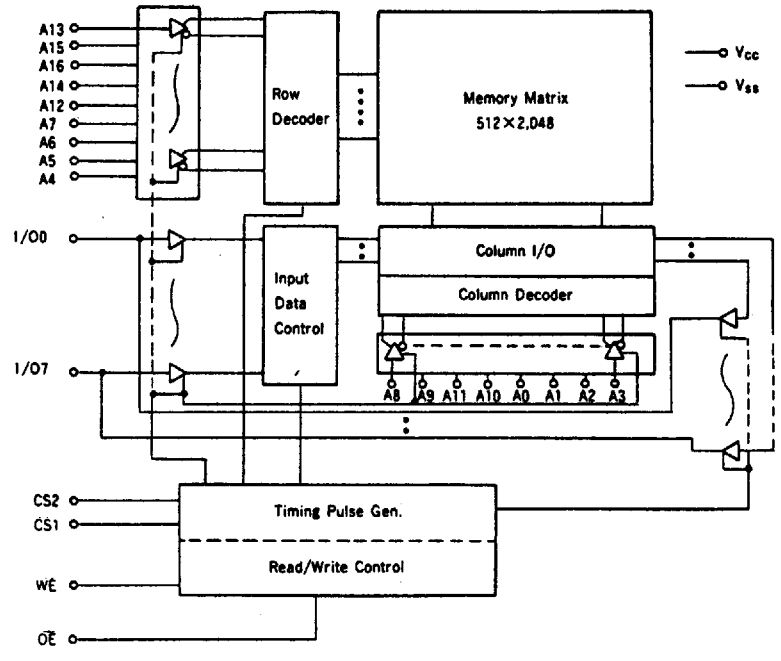

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■ ORDERING INFORMATION

Part No.	Access	Package	Part No.	Access	Package
HM628128P-7	70ns	600 mil 32 pin Plastic DIP (DP-32)	HM628128LP-7SL	70ns	600 mil 32 pin Plastic DIP (DP-32)
HM628128P-8	85ns		HM628128LP-8SL	85ns	
HM628128P-10	100ns		HM628128LP-10SL	100ns	
HM628128P-12	120ns		HM628128LP-12SL	120ns	
HM628128LP-7	70ns				
HM628128LP-8	85ns				
HM628128LP-10	100ns				
HM628128LP-12	120ns				
HM628128FP-7	70ns	525 mil 32 pin Plastic SOP (FP-32D)	HM628128LFP-7SL	70ns	525 mil 32 pin Plastic SOP (FP-32D)
HM628128FP-8	85ns		HM628128LFP-8SL	85ns	
HM628128FP-10	100ns		HM628128LFP-10SL	100ns	
HM628128FP-12	120ns		HM628128LFP-12SL	120ns	
HM628128LFP-7	70ns				
HM628128LFP-8	85ns				
HM628128LFP-10	100ns				
HM628128LFP-12	120ns				

• TSOP SERIES

Type No.	Access Time	Package
HM628128T-7	70 ns	8mm×20mm 32-Pin TSOP (Normal Type) (TFP-32DA)
HM628128T-8	85 ns	
HM628128T-10	100 ns	
HM628128T-12	120 ns	
HM628128LT-7	70 ns	
HM628128LT-8	85 ns	
HM628128LT-10	100 ns	
HM628128LT-12	120 ns	
HM628128LT-7L	70 ns	
HM628128LT-8L	85 ns	
HM628128LT-10L	100 ns	
HM628128LT-12L	120 ns	
HM628128R-7	70 ns	8mm×20mm 32-Pin TSOP (Reverse Type) (TFP-32DAR)
HM628128R-8	85 ns	
HM628128R-10	100 ns	
HM628128R-12	120 ns	
HM628128LR-7	70 ns	
HM628128LR-8	85 ns	
HM628128LR-10	100 ns	
HM628128LR-12	120 ns	
HM628128LR-7L	70 ns	
HM628128LR-8L	85 ns	
HM628128LR-10L	100 ns	
HM628128LR-12L	120 ns	

• INDUSTRIAL TEMPERATURE SERIES

Type No.	Access Time	Package
HM628128PI-8	85 ns	600-mil 32-Pin Plastic DIP (DP-32)
HM628128PI-10	100 ns	
HM628128PI-12	120 ns	
HM628128LPI-8	85 ns	
HM628128LPI-10	100 ns	
HM628128LPI-12	120 ns	
HM628128FPI-8	85 ns	525-mil 32-Pin Plastic SOP (FP-32)
HM628128FPI-10	100 ns	
HM628128FPI-12	120 ns	
HM628128LFPI-8	85 ns	
HM628128LFPI-10	100 ns	
HM628128LFPI-12	120 ns	

Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature (HM628128 Series)	T_{opr}	0 to +70	°C
Operating temperature (HM628128I Series)	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias (HM628128 Series)	T_{bias}	−10 to +85	°C
Storage temperature under bias (HM628128I Series)	T_{bias}	−40 to +85	°C

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions

(Ta=0 to +70°C, for HM628128 Series, Ta=−40° to +85°C for HM628128I Series)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	−0.3*1	—	0.8	V	

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics

(Ta=0 to +70°C, for HM628128 Series, Ta=−40° to +85°C for HM628128I Series, V_{CC}=5 V ± 10%, V_{SS}=0 V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	μA	Vin=V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	15	35 (45)	mA	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, others=V_{IH}/V_{IL}, $I_{I/O}$=0 mA (HM628128I Series)
Operating Power supply current	I_{CC1}	—	45	70 (80)	mA	Min. cycle, duty=100%, $\overline{CS1}$=V_{IL}, CS2=V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$=0 mA (HM628128I Series)
	I_{CC2}	—	15	30 (40)	mA	Cycle time = 1μs, duty = 100%, $I_{I/O}$=0 mA, CS1≤0.2V, CS2≥ V_{CC} −0.2V, V_{IH}≥V_{CC}−0.2V, V_{IL}≤0.2V (HM628128I Series)
Standby V_{CC} current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$=V_{IH}, CS2=V_{IH} or CS2=V_{IL}
Standby V_{CC} current (1): DC	I_{SB1}	—	0.02	2	mA	Vin≥ 0 V, CS1≥ V_{CC} −0.2V, CS2≥ V_{CC} −0.2V or 0 V≤ CS2≤ 0.2 V
		—	2*2	100*2	μA	
		—	2*3	50*3		
Output low voltage	V_{OL}	—	—	0.4	0	I_{OL}=2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}= −1.0 mA

Note: 1. Typical values are at V_{CC}=5.0V, Ta=+25°C and specified loading.
2. This characteristics is guaranteed only for L-version.
3. This characteristics is guaranteed only for SL-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	CI/O	—	—	10	pF	VI/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta=0 to +70°C, for HM628128 Series, Ta=−40 to +85°C for HM628128I Series, V_{CC}=5 V ± 10%, unless otherwise noted)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V for HM628128 Series
  0.5 V to 2.5 V for HM628128I Series
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5V
- Output load: 1 TTL Gate and CL (100pF)
  (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128I-8 HM628128-8		HM628128I-10 HM628128-10		HM628128I-12 HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	tRC	70	—	85	—	100	—	120	—	ns	
Address access time	tAA	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	tCO1	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	tCO2	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	tOE	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	tLZ1	10	—	10	—	10	—	10	—	ns	*1, *2,
Chip selection (CS2) to output in low-Z	tLZ2	10	—	10	—	10	—	10	—	ns	*1, *2,
Output enable ($\overline{OE}$) to output in low-Z	tOLZ	5	—	5	—	5	—	5	—	ns	*1, *2,
Chip deselection ($\overline{CS1}$) to output in high-Z	tHZ1	0	25	0	30	0	35	0	45	ns	*1, *2,
Chip deselection (CS2) to output in high-Z	tHZ2	0	25	0	30	0	35	0	45	ns	*1, *2,
Output disable ($\overline{OE}$) to output in high-Z	tOHZ	0	25	0	30	0	35	0	45	ns	*1, *2,
Output hold from address change	tOH	10	—	10	—	10	—	10	—	ns	

Read Cycle Timing

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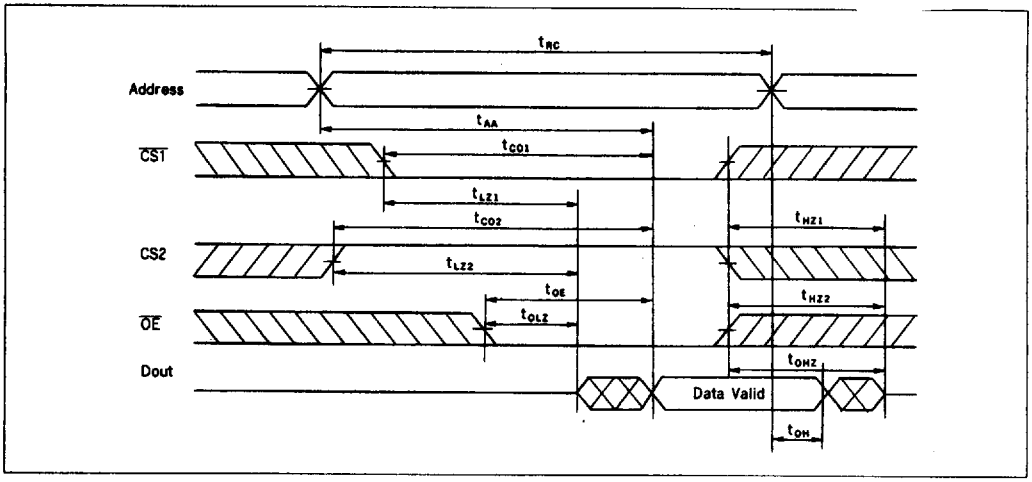

Notes: *1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
*3. $\overline{WE}$ is high for read cycle.

Write Cycle

Parameter	Symbol	HM628128-7		HM628128I-8 HM628128-8		HM628128I-10 HM628128-10		HM628128I-12 HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	80	—	85	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	t_{AW}	60	—	75	—	80	—	85	—	ns	
Write pulse width	t_{WP}	50	—	55	—	60	—	70	—	ns	
Write recovery time	t_{WR}	5	—	5 (10)	—	5 (10)	—	10 (15)	—	ns	*12
		10	—	10 (15)	—	10 (15)	—	15 (15)	—	ns	*11 *12
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	t_{DW}	30	—	35	—	40	—	45	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns	*10

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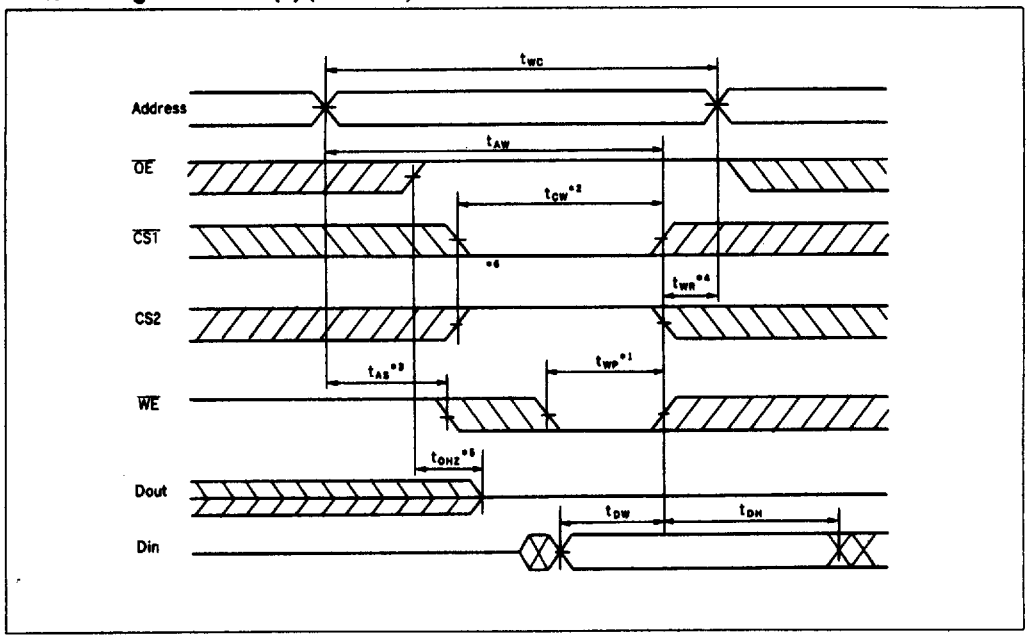
Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)

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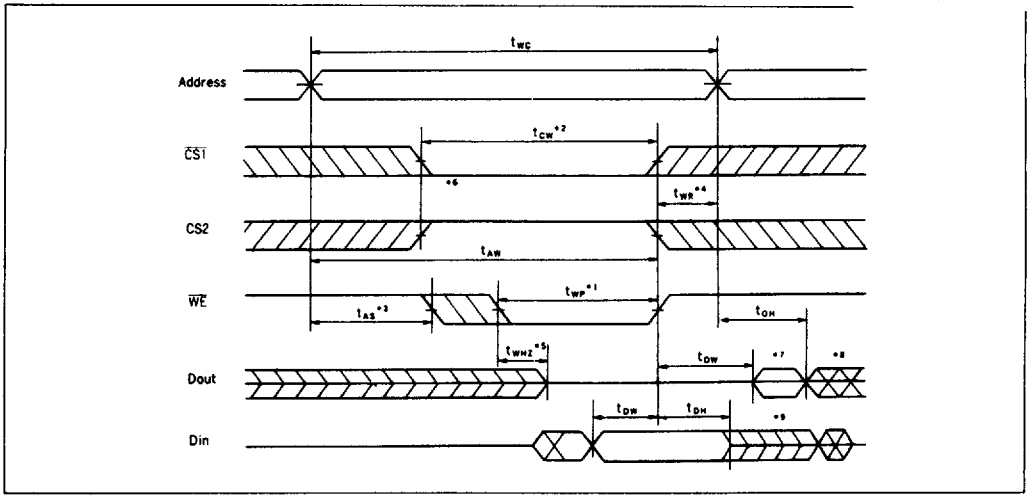

Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

*7. Dout is the same phase of the latest written data in this write cycle.

*8. Dout is the read data of next address.

*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

*10. This parameter is sampled and not 100% tested.

*11. This value is measured from CS2 going low to the end of write cycle.

*12. Parenthesis denote specification for HM6281281 Series only.

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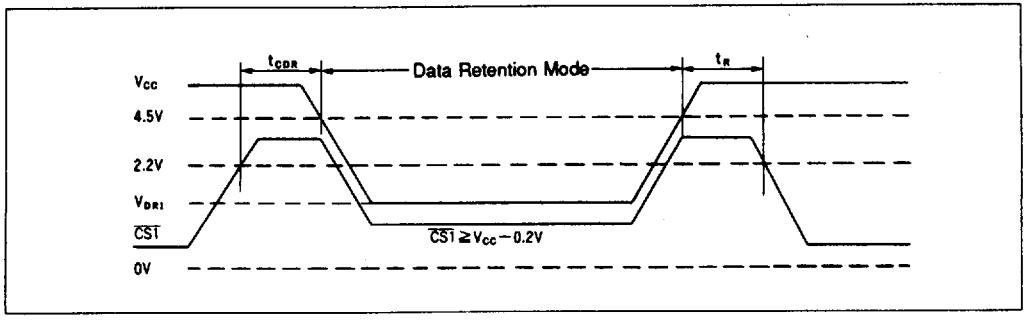
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C) for HM628128 Series, Ta = −40 to +85°C for HM628128I Series.

(This characteristics is guaranteed only for L & SL version.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions*2
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}			50*13	μA	V_{CC} = 3.0 V, Vin ≥ 0V $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} −0.2 V or 0 V ≤ CS2 ≤ 2.0V
				15*14		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5*15	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



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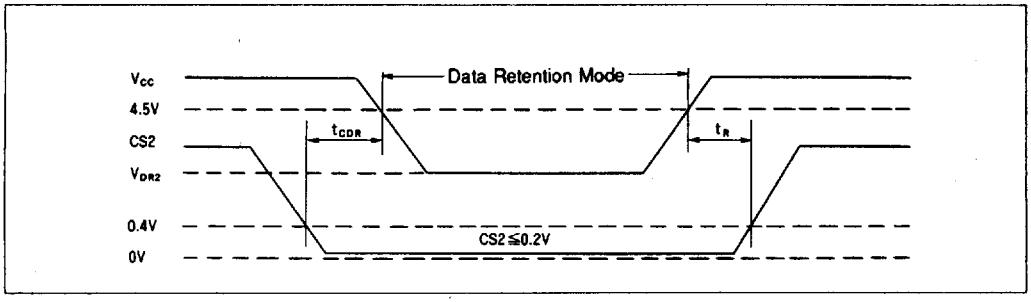
Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)



Note: 13. *1: for L-version and 20 uA max. at Ta=0 to 40°C
*2: for SL-version and 3uA max. at Ta=0 to 40°C.

14. CS2 controls address buffer, WE buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} -0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, $\overline{WE}$ $\overline{OE}$, I/O) can be in the high impedance state.

15. V_{CC} rise time must be more than 50ms when V_{CC} rise time is less than 50ms, t_R must be 50ms or more.

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