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# HN58V1001 Series

1M EEPROM (128-kword  $\times$  8-bit)  
Ready/ $\overline{\text{Busy}}$  and  $\overline{\text{RES}}$  function

# HITACHI

ADE-203-314G (Z)  
Rev. 7.0  
Oct. 31, 1997

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## Description

The Hitachi HN58V1001 is a electrically erasable and programmable ROM organized as 131072-word  $\times$  8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make the write operations faster.

## Features

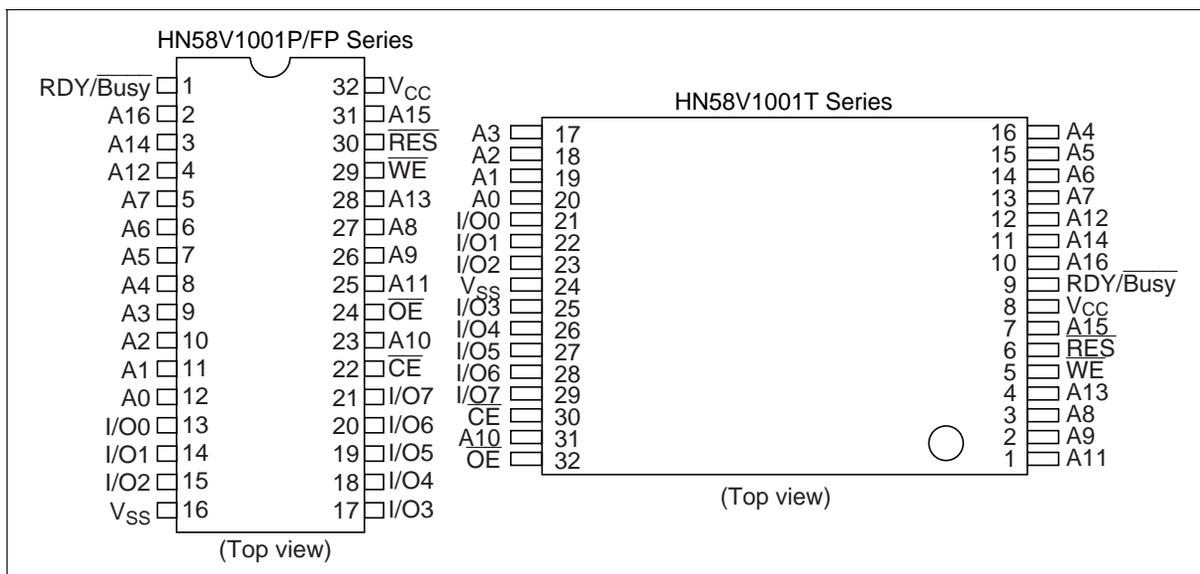
- Single 3 V supply: 2.7 V to 5.5 V
- Access time: 250 ns (max)
- Power dissipation
  - Active: 20 mW/MHz, (typ)
  - Standby: 110  $\mu$ W (max)
- On-chip latches: address, data,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$
- Automatic byte write: 15 ms (max)
- Automatic page write (128 bytes): 15 ms (max)
- $\overline{\text{Data}}$  polling and  $\overline{\text{RDY/Busy}}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- $10^4$  erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by  $\overline{\text{RES}}$  pin

# HN58V1001 Series

## Ordering Information

Type No.	Access time	Package
HN58V1001P-25	250 ns	600 mil 32-pin plastic DIP (DP-32)
HN58V1001FP-25	250 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58V1001T-25	250 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

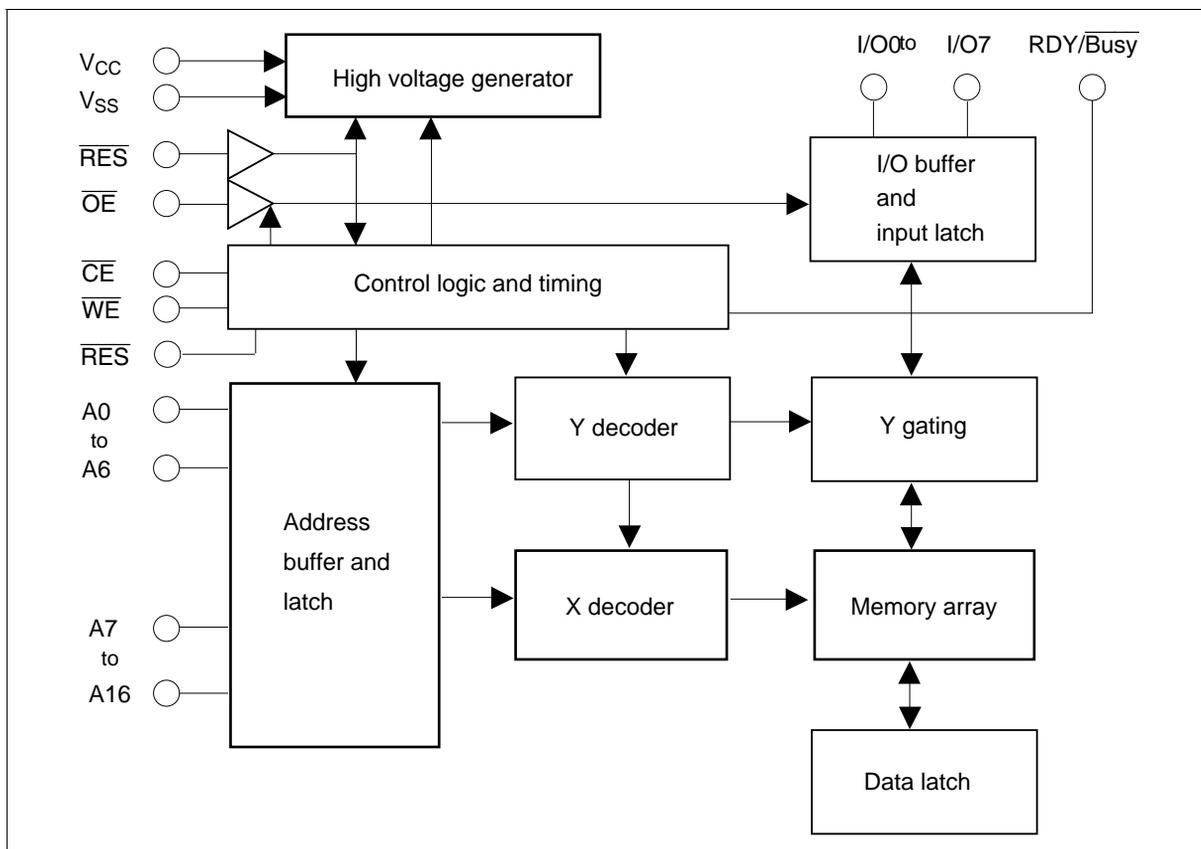
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
OE	Output enable
CE	Chip enable
WE	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
RDY/Busy	Ready busy
RES	Reset

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	$\overline{RDY/Busy}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub> *1	High-Z	Dout
Standby	V <sub>IH</sub>	x*2	x	x	High-Z	High-Z
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>H</sub>	High-Z to V <sub>OL</sub>	Din
Deselect	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>H</sub>	High-Z	High-Z
Write Inhibit	x	x	V <sub>IH</sub>	x	—	—
	x	V <sub>IL</sub>	x	x	—	—
Data Polling	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>OL</sub>	Dout (I/O7)
Program reset	x	x	x	V <sub>IL</sub>	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.

2. x : Don't care

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.6 to +7.0	V
Input voltage relative to $V_{SS}$	$V_{in}$	-0.5* <sup>1</sup> to +7.0	V
Operating temperature range* <sup>2</sup>	$T_{opr}$	0 to +70	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C

Notes: 1.  $V_{in}$  min = -3.0 V for pulse width  $\leq$  50 ns  
 2. Including electrical characteristics and data retention

## Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.0	5.5	V
	$V_{SS}$	0	0	0	V
Input voltage	$V_{IL}$	-0.3* <sup>1</sup>	—	0.8	V
	$V_{IH}$	1.9* <sup>2</sup>	—	$V_{CC} + 0.3$	V
	$V_H$	$V_{CC} - 0.5$	—	$V_{CC} + 1.0$	V
Operating temperature	$T_{opr}$	0	—	70	°C

Notes: 1.  $V_{IL}$  (min): -1.0 V for pulse width  $\leq$  50 ns  
 2.  $V_{IH}$  (min): 2.2 V for  $V_{CC} = 3.6$  to 5.5 V

## DC Characteristics ( $T_a = 0$ to +70 °C, $V_{CC} = 2.7$ V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2* <sup>1</sup>	$\mu$ A	$V_{CC} = 3.6$ V, $V_{in} = 3.6$ V
Output leakage current	$I_{LO}$	—	—	2	$\mu$ A	$V_{CC} = 3.6$ V, $V_{out} = 3.6/0.4$ V
Standby $V_{CC}$ current	$I_{CC1}$	—	—	20	$\mu$ A	$\overline{CE} = V_{CC}$
	$I_{CC2}$	—	—	1	mA	$\overline{CE} = V_{IH}$
Operating $V_{CC}$ current	$I_{CC3}$	—	—	6	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 1 $\mu$ s at $V_{CC} = 3.3$ V
		—	—	15	mA	$I_{out} = 0$ mA, Duty = 100%, Cycle = 250 ns at $V_{CC} = 3.3$ V
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA
Output high voltage	$V_{OH}$	$V_{CC} \times 0.8$	—	—	V	$I_{OH} = -400$ $\mu$ A

Notes: 1.  $I_{LI}$  on  $\overline{RES}$ : 100  $\mu$ A (max)

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

**AC Characteristics** ( $T_a = 0\text{ to }+70\text{ }^\circ\text{C}$ ,  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ )

**Test Conditions**

- Input pulse levels: 0.4 V to 2.4 V  
0 V to  $V_{CC}$  ( $\overline{\text{RES}}$  pin)
- Input rise and fall time: 20 ns
- Output load: 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V, 1.8 V

**Read Cycle**
**HN58V1001-25**

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	$t_{\text{ACC}}$	—	250	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{CE}}$ to output delay	$t_{\text{CE}}$	—	250	ns	$\overline{\text{OE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{OE}}$ to output delay	$t_{\text{OE}}$	10	120	ns	$\overline{\text{CE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
Address to output hold	$t_{\text{OH}}$	0	—	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{OE}}$ ( $\overline{\text{CE}}$ ) high to output float*1	$t_{\text{DF}}$	0	50	ns	$\overline{\text{CE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{RES}}$ low to output float*1	$t_{\text{DFR}}$	0	350	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$
$\overline{\text{RES}}$ to output delay	$t_{\text{RR}}$	0	600	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , $\overline{\text{WE}} = V_{\text{IH}}$

## Write Cycle

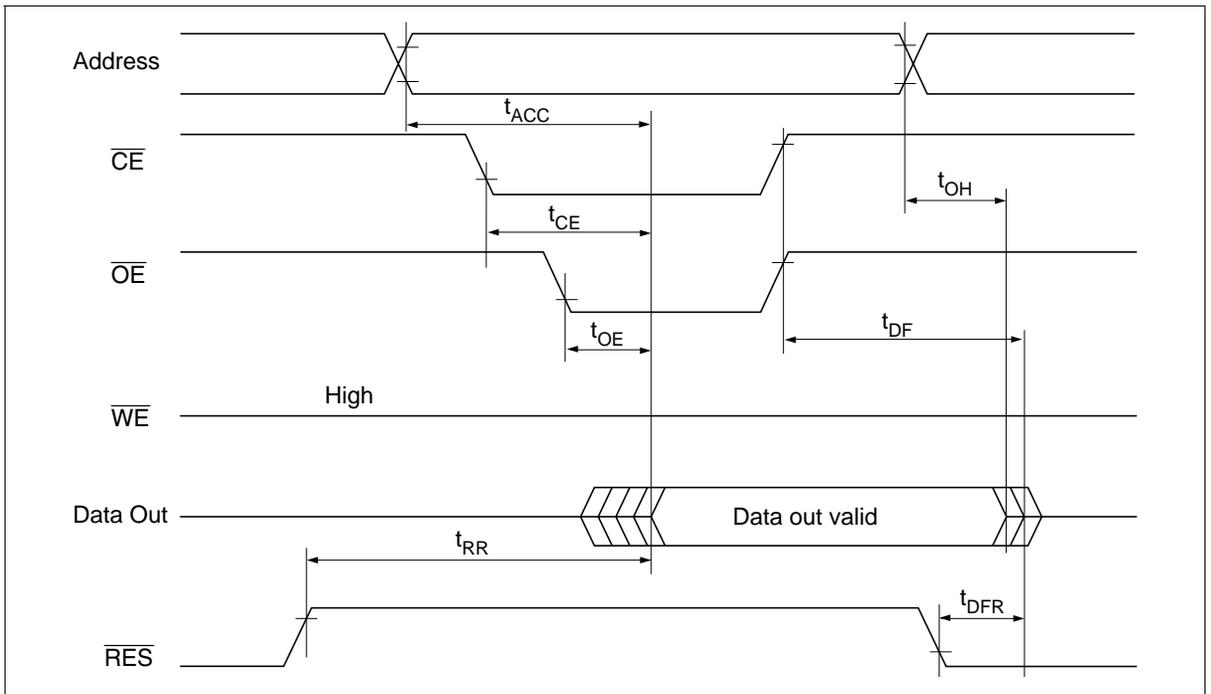
Parameter	Symbol	Min <sup>+2</sup>	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	0	—	—	ns	
Address hold time	$t_{AH}$	150	—	—	ns	
$\overline{CE}$ to write setup time ( $\overline{WE}$ controlled)	$t_{CS}$	0	—	—	ns	
$\overline{CE}$ hold time ( $\overline{WE}$ controlled)	$t_{CH}$	0	—	—	ns	
$\overline{WE}$ to write setup time ( $\overline{CE}$ controlled)	$t_{WS}$	0	—	—	ns	
$\overline{WE}$ hold time ( $\overline{CE}$ controlled)	$t_{WH}$	0	—	—	ns	
$\overline{OE}$ to write setup time	$t_{OES}$	0	—	—	ns	
$\overline{OE}$ hold time	$t_{OEh}$	0	—	—	ns	
Data setup time	$t_{DS}$	100	—	—	ns	
Data hold time	$t_{DH}$	10	—	—	ns	
$\overline{WE}$ pulse width ( $\overline{WE}$ controlled)	$t_{WP}$	250	—	—	ns	
$\overline{CE}$ pulse width ( $\overline{CE}$ controlled)	$t_{CW}$	250	—	—	ns	
Data latch time	$t_{DL}$	750	—	—	ns	
Byte load cycle	$t_{BLC}$	1.0	—	30	$\mu$ s	
Byte load window	$t_{BL}$	100	—	—	$\mu$ s	
Write cycle time	$t_{WC}$	—	—	15 <sup>*3</sup>	ms	
Time to device busy	$t_{DB}$	120	—	—	ns	
Write start time	$t_{DW}$	250 <sup>*4</sup>	—	—	ns	
Reset protect time	$t_{RP}$	100	—	—	$\mu$ s	
Reset high time <sup>*5</sup>	$t_{RES}$	1	—	—	$\mu$ s	

Notes: 1.  $t_{DF}$  and  $t_{DFR}$  are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

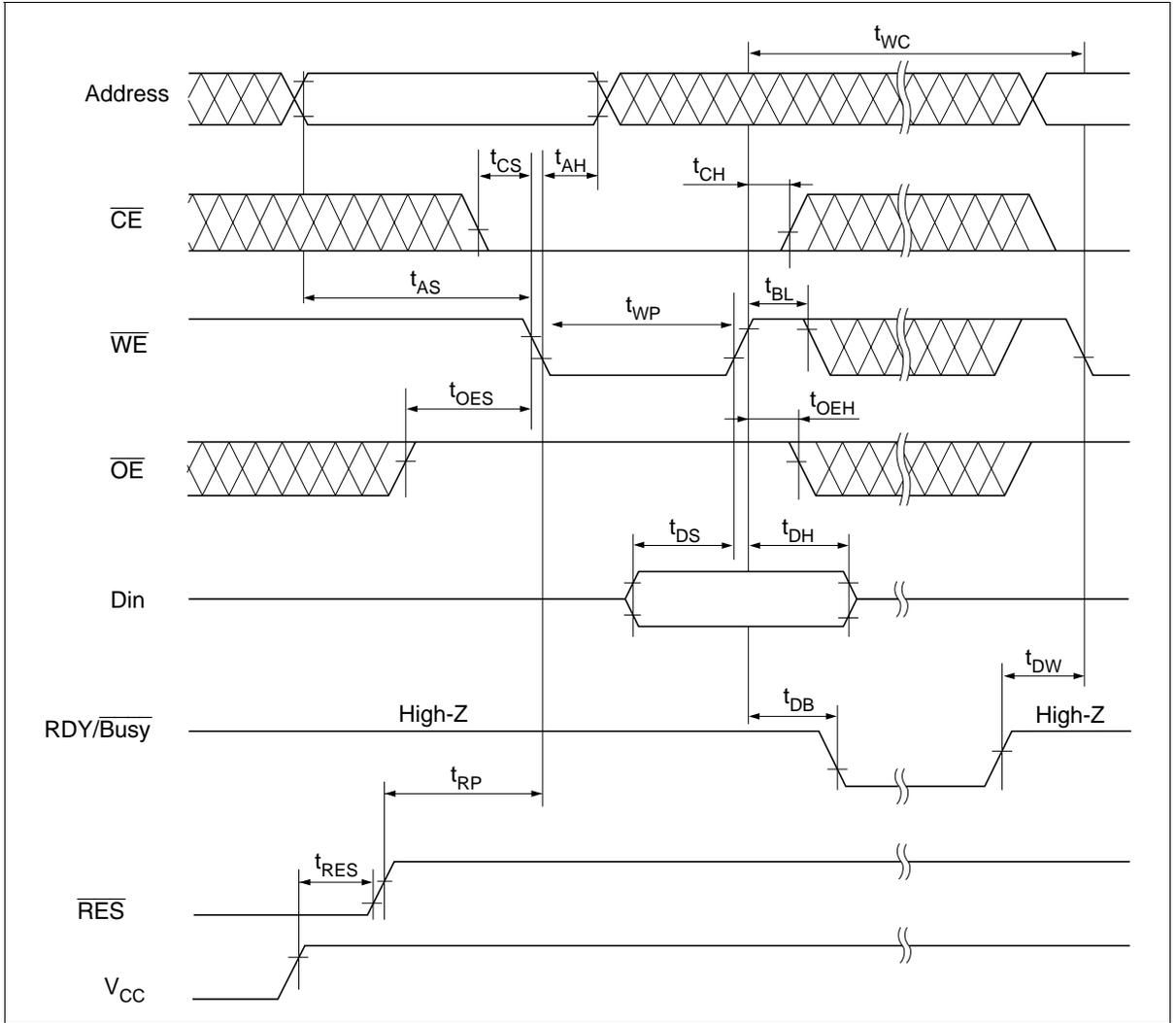
2. Use this device in longer cycle than this value.
3.  $t_{WC}$  must be longer than this value unless polling techniques or  $\overline{RDY}/\overline{Busy}$  are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after  $t_{DW}$  if polling techniques or  $\overline{RDY}/\overline{Busy}$  are used.
5. This parameter is sampled and not 100% tested.
6. A7 to A16 are page addresses and must be same within the page write operation.
7. See AC read characteristics.

Timing Waveforms

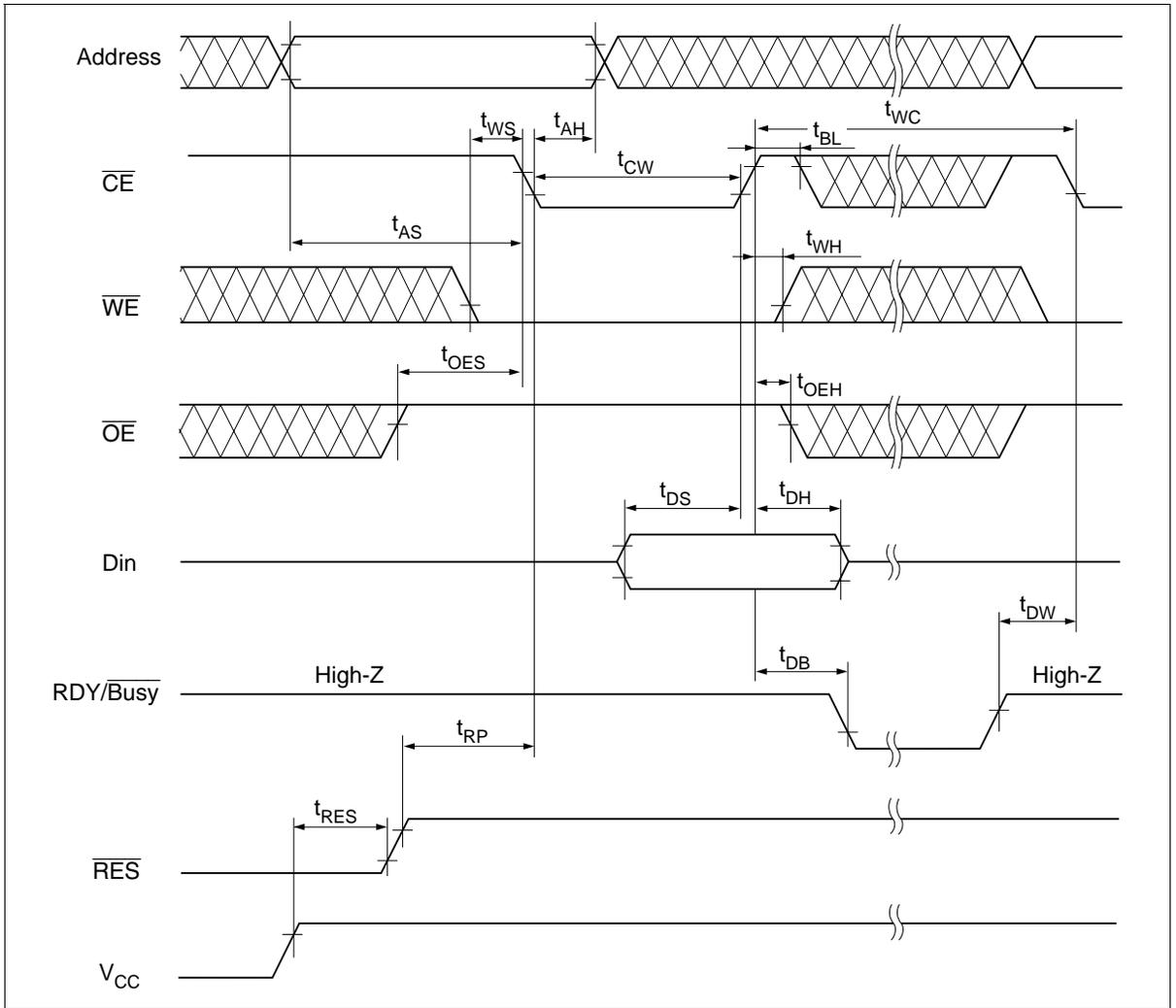
Read Timing Waveform



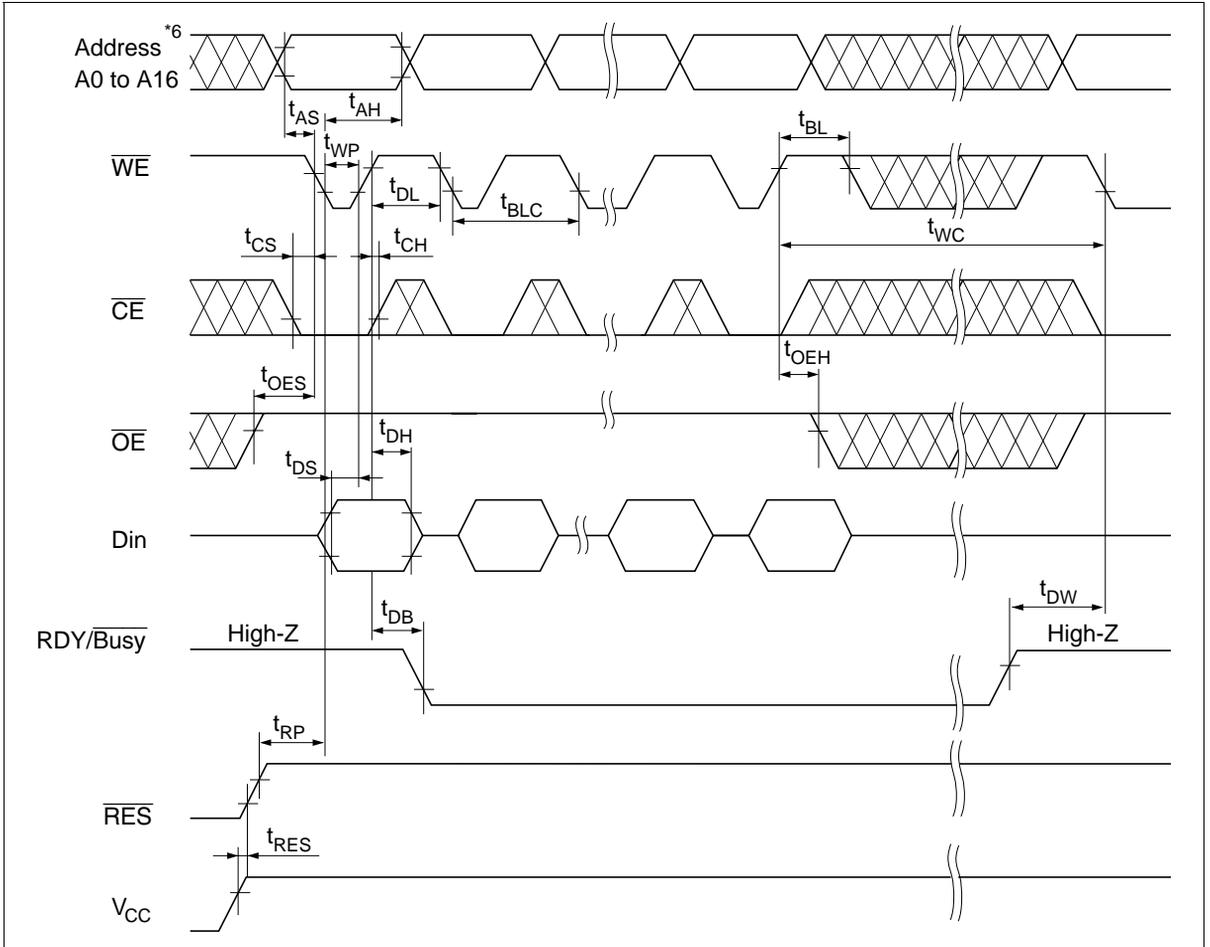
## Byte Write Timing Waveform (1) ( $\overline{WE}$ Controlled)



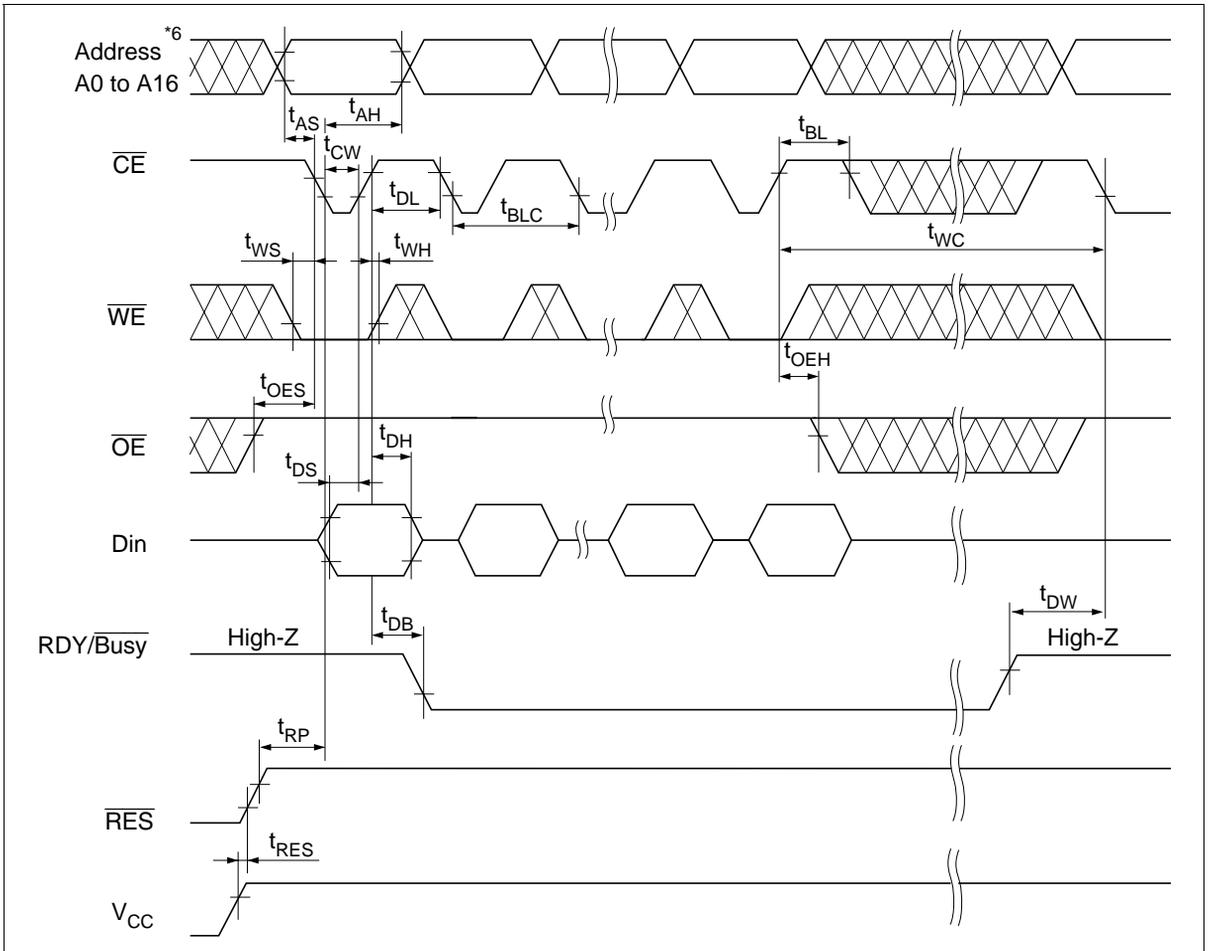
Byte Write Timing Waveform (2) ( $\overline{CE}$  Controlled)



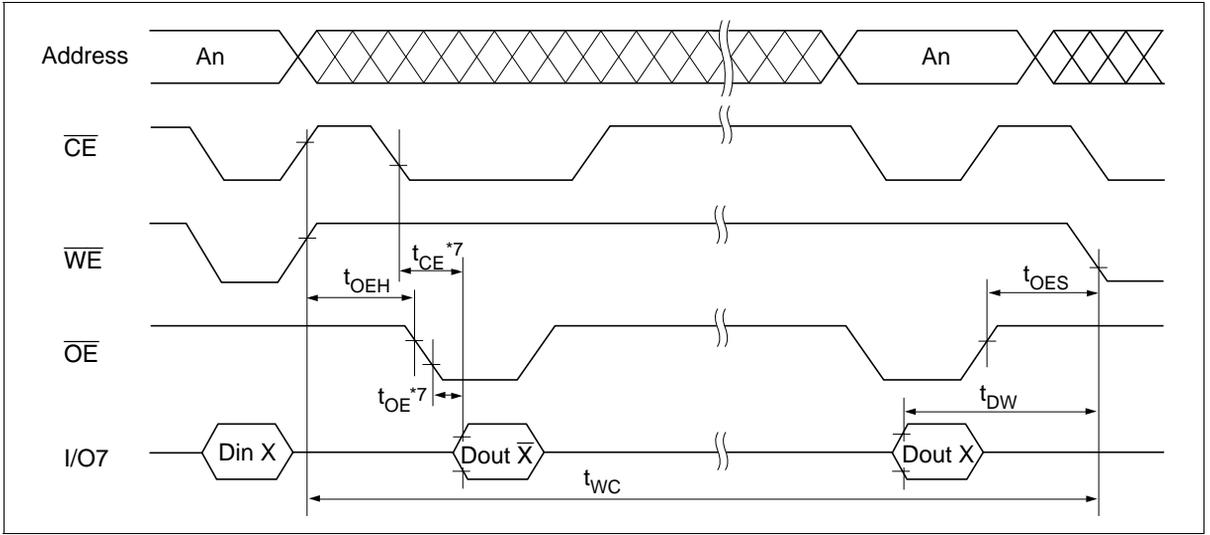
## Page Write Timing Waveform (1) ( $\overline{\text{WE}}$ Controlled)



Page Write Timing Waveform (2) ( $\overline{\text{CE}}$  Controlled)



## Data Polling Timing Waveform

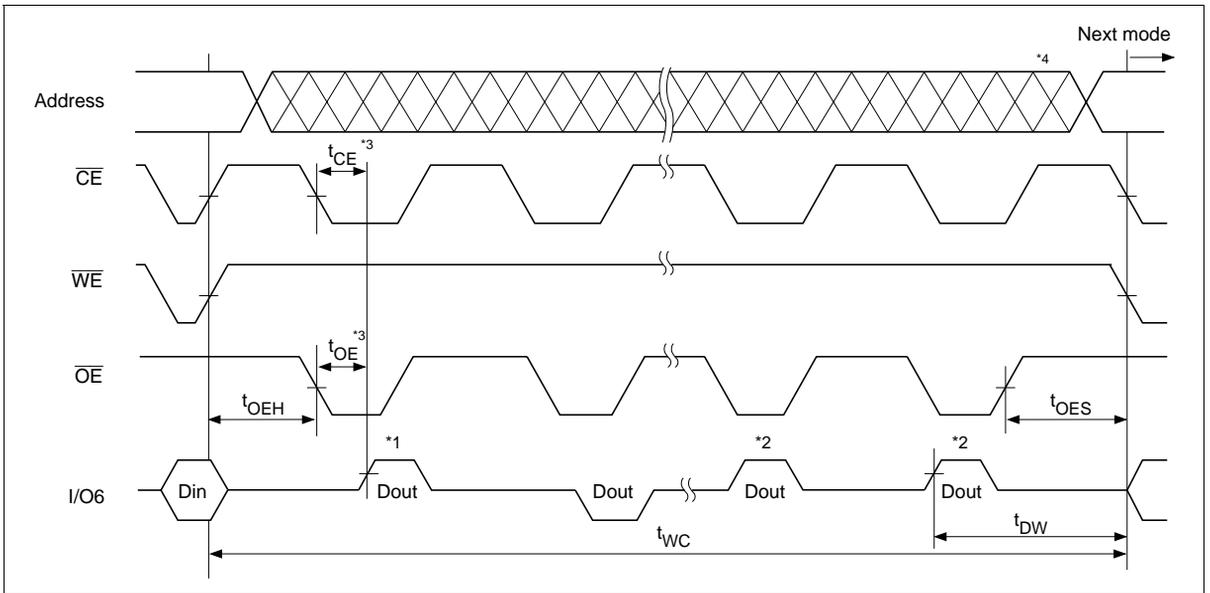


**Toggle bit**

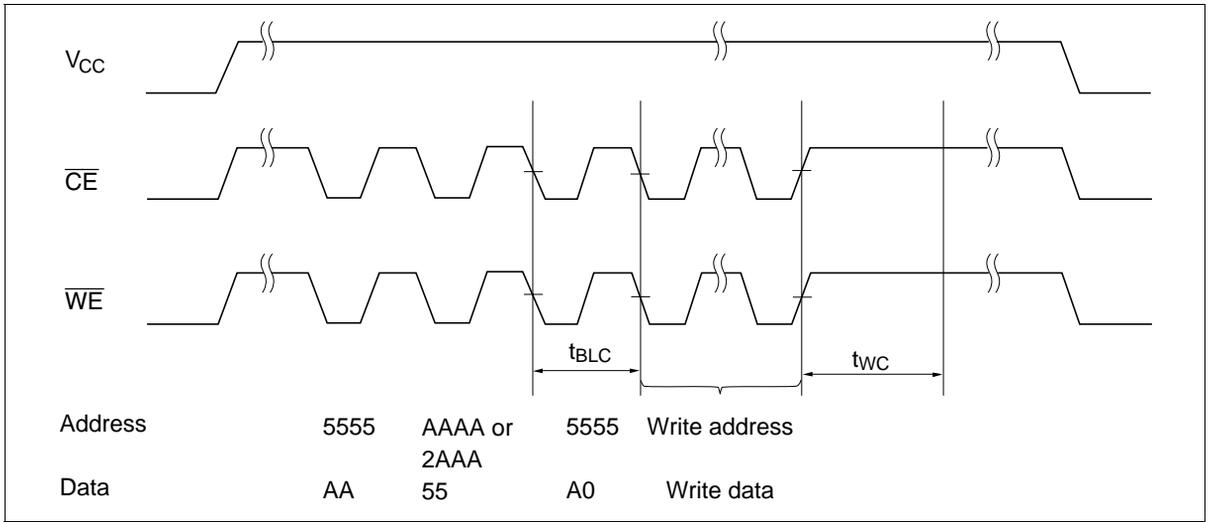
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

- Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any location can be used, but the address must be fixed.

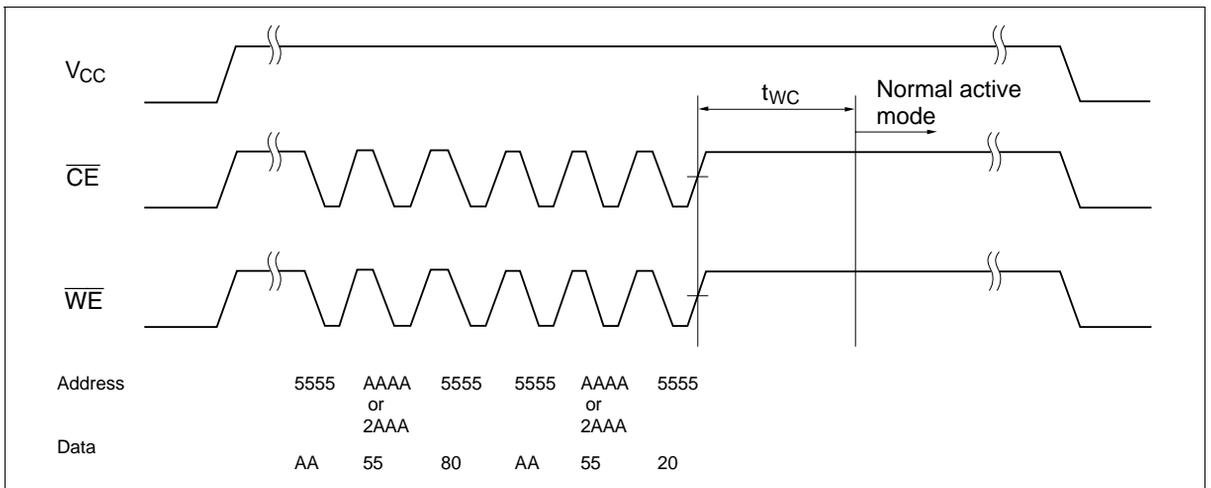
**Toggle bit Waveform**



## Software Data Protection Timing Waveform (1) (in protection mode)



## Software Data Protection Timing Waveform (2) (in non-protection mode)



## Functional Description

### Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 127 bytes can be written in the same manner. Each additional byte load cycle must be started within 30  $\mu$ s from the preceding falling edge of  $\overline{WE}$  or  $\overline{CE}$ . When  $\overline{CE}$  or  $\overline{WE}$  is kept high for 100  $\mu$ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

### Data Polling

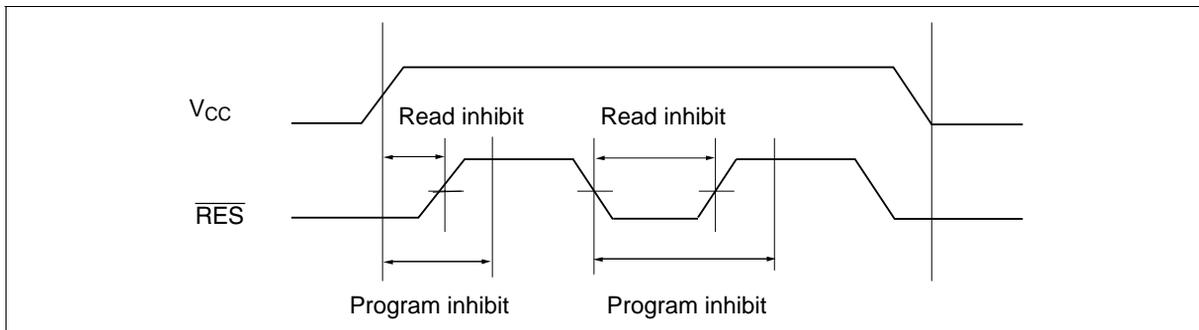
Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

### RDY/ $\overline{Busy}$ Signal

RDY/ $\overline{Busy}$  signal also allows status of the EEPROM to be determined. The RDY/ $\overline{Busy}$  signal has high impedance except in write cycle and is lowered to  $V_{OL}$  after the first write signal. At the end of write cycle, the RDY/ $\overline{Busy}$  signal changes state to high impedance.

### $\overline{RES}$ Signal

When  $\overline{RES}$  is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping  $\overline{RES}$  low when  $V_{CC}$  is switched.  $\overline{RES}$  should be high during read and programming because it doesn't provide a latch function.



### $\overline{WE}$ , $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , and data is latched by the rising edge of  $\overline{WE}$  or  $\overline{CE}$ .

## Write/Erase Endurance and Data Retention Time

The endurance is  $10^4$  cycles in case of the page programming and  $10^3$  cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than  $10^4$  cycles.

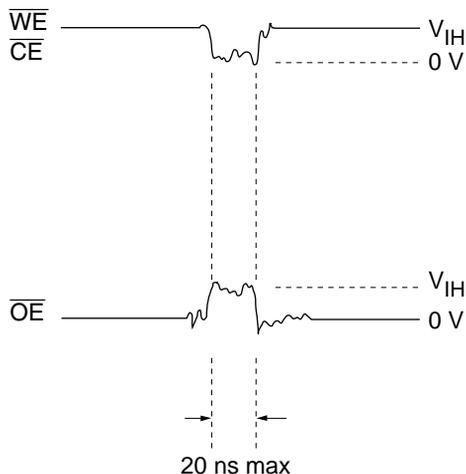
## Data Protection

### 1. Data Protection against Noise on Control Pins ( $\overline{CE}$ , $\overline{OE}$ , $\overline{WE}$ ) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less in program mode.

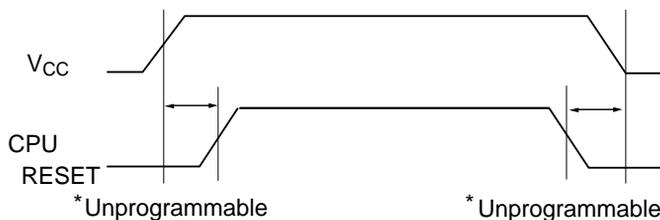
Be careful not to allow noise of a width of more than 20 ns on the control pins.



## 2. Data Protection at $V_{CC}$ On/Off

When  $V_{CC}$  is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

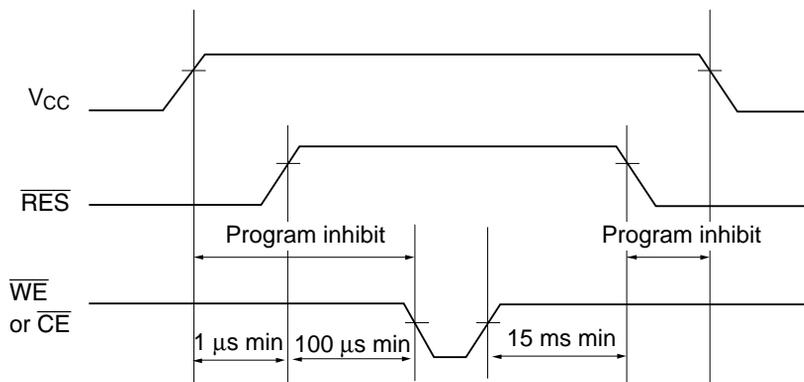
Note: The EEPROM should be kept in unprogrammable state during  $V_{CC}$  on/off by using CPU RESET signal.



### (1) Protection by $\overline{RES}$

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's  $\overline{RES}$  pin.  $\overline{RES}$  should be kept  $V_{SS}$  level during  $V_{CC}$  on/off.

The EEPROM brakes off programming operation when  $\overline{RES}$  becomes low, programming operation doesn't finish correctly in case that  $\overline{RES}$  falls low during programming operation.  $\overline{RES}$  should be kept high for 15 ms after the last data input.

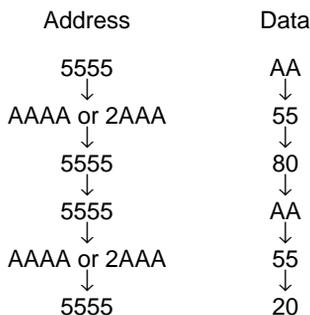


## 3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.



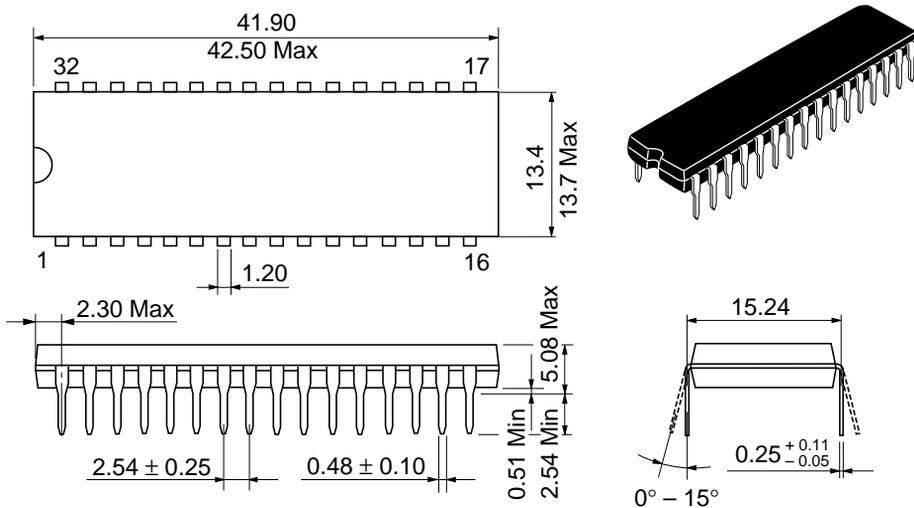
The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Hitachi sales offices.

## Package Dimensions

### HN58V1001P Series (DP-32)

Unit: mm



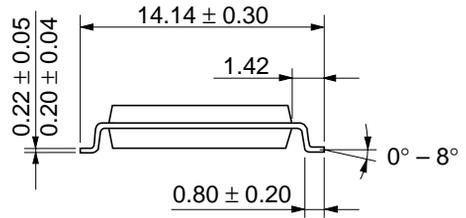
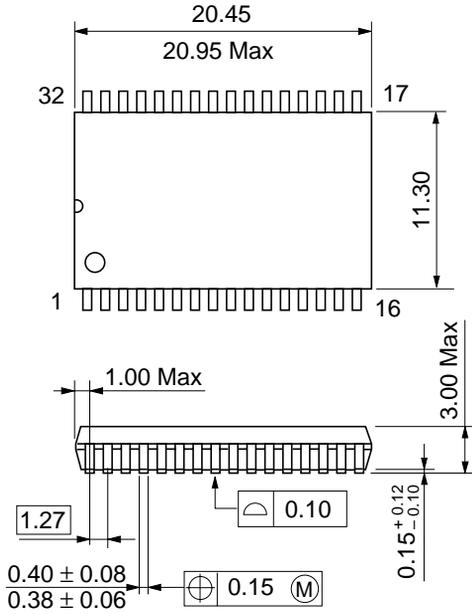
Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

# HN58V1001 Series

## Package Dimensions (cont.)

### HN58V1001FP Series (FP-32D)

Unit: mm



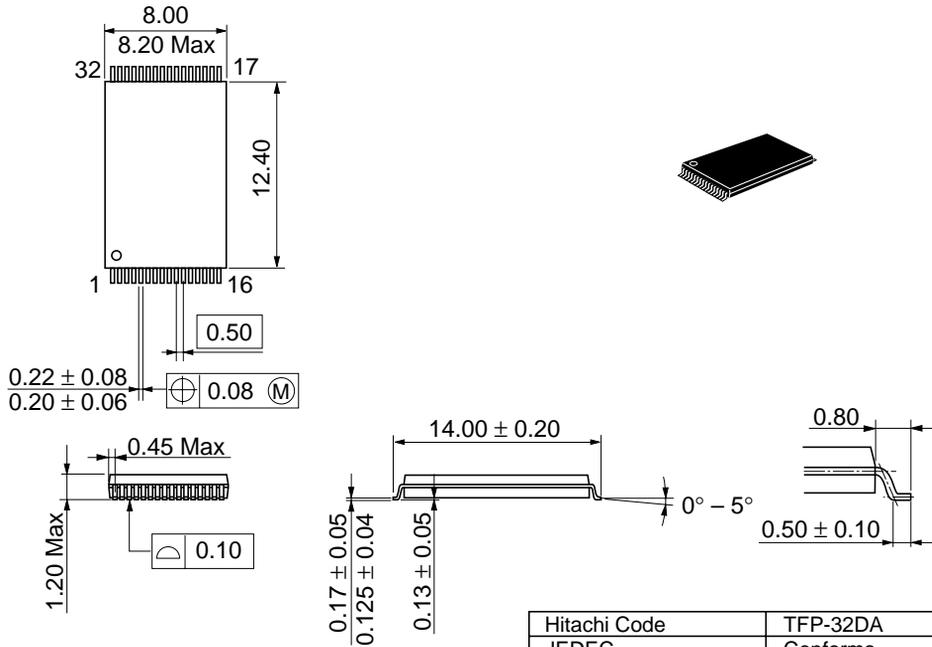
Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

## Package Dimensions (cont.)

### HN58V1001T Series (TFP-32DA)

Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	TFP-32DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.26 g

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