M29W641D

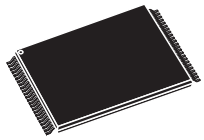
64 Mbit (4Mb x16, Uniform Block) 3V Supply Flash Memory

PRODUCT PREVIEW

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V Core Power Supply
  - V_{CCQ} = 1.8V to 3.6V for Input/Output
  - V_{PP} =12 V for Fast Program (optional)
- ACCESS TIME: 70, 90 ns
- PROGRAMMING TIME
  - 10 µs typical
  - Double Word Programming Option
- 128 MAIN MEMORY BLOCKS
  - 32 KWords each
- JEDEC Standard Command Set
- PROGRAM/ERASE CONTROLLER
  - Embedded Program and Erase algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- V_{PP} Pin for FAST PROGRAM
- $\overline{WP}$ Pin for WRITE PROTECT of First or Last Block
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE (CFI)
- EXTENDED MEMORY BLOCK
  - Extra block used as security block or to store additional information
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code M29W641D: 22C7h

Figure 1. Packages



TSOP48 (N)
12 x 20mm

This is preliminary information on a new product now in development. Details are subject to change without notice.

TABLE OF CONTENTS

SUMMARY DESCRIPTION 5

Figure 2. Logic Diagram 5
Table 1. Signal Names 5
Figure 3. TSOP Connections 6

SIGNAL DESCRIPTIONS 7

Address Inputs (A0-A21). 7
Data Inputs/Outputs (DQ0-DQ7). 7
Data Inputs/Outputs (DQ8-DQ15). 7
Chip Enable (E). 7
Output Enable (G). 7
Write Enable (W). 7
Write Protect (WP). 7
Reset/Block Temporary Unprotect (RP). 7
V_{PP} (V_{PP}). 7
V_{CC} Supply Voltage (2.7V to 3.6V). 7
V_{CCQ} Supply Voltage (1.8V to 3.6V). 7
V_{SS} Ground. 7

Bus Operations 8

Bus Read. 9
Bus Write. 9
Output Disable. 9
Standby. 9
Automatic Standby. 9

Special Bus Operations 9

Electronic Signature. 9
Block Protect and Chip Unprotect. 9
Block Protect and Chip Unprotect. 9
Table 2. Bus Operations 8

COMMAND INTERFACE 10

Read/Reset Command. 10
Auto Select Command. 10
Program Command. 10
Unlock Bypass Command. 11
Unlock Bypass Program Command. 11
Unlock Bypass Reset Command. 11
Chip Erase Command. 11
Block Erase Command. 12
Erase Suspend Command. 12
Erase Resume Command. 12
Enter Extended Block Command 12

Exit Extended Block Command. 12
Table 3. Commands 13
Table 4. Program, Erase Times and Program, Erase Endurance Cycles 13

STATUS REGISTER 14

Data Polling Bit (DQ7). 14
Toggle Bit (DQ6).. 14
Error Bit (DQ5). 14
Erase Timer Bit (DQ3). 14
Alternative Toggle Bit (DQ2).. 14
Table 5. Status Register Bits 15
Figure 4. Data Polling Flowchart 15
Figure 5. Data Toggle Flowchart 15

MAXIMUM RATING. 16

Table 6. Absolute Maximum Ratings 16

DC and AC PARAMETERS 17

Table 7. Operating and AC Measurement Conditions. 17
Figure 6. AC Measurement I/O Waveform 17
Figure 7. AC Measurement Load Circuit 17
Table 8. Device Capacitance. 17
Table 9. DC Characteristics. 18
Figure 8. Read Mode AC Waveforms 19
Table 10. Read AC Characteristics 19
Figure 9. Write AC Waveforms, Write Enable Controlled 20
Table 11. Write AC Characteristics, Write Enable Controlled 20
Figure 10. Write AC Waveforms, Chip Enable Controlled. 21
Table 12. Write AC Characteristics, Chip Enable Controlled 21
Figure 11. Reset/Block Temporary Unprotect AC Waveforms 22
Table 13. Reset/Block Temporary Unprotect AC Characteristics 22
Figure 12. Accelerated Program Timing Waveforms. 22

PACKAGE MECHANICAL 23

TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline 23
TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data 23

PART NUMBERING 24

Table 14. Ordering Information Scheme 24

REVISION HISTORY. 25

Table 15. Document Revision History 25

APPENDIX A. BLOCK ADDRESSES. 26

Table 16. Block Addresses 26

APPENDIX B. COMMON FLASH INTERFACE (CFI) 30
Table 17. Query Structure Overview 30
Table 18. CFI Query Identification String 30
Table 19. CFI Query System Interface Information 31
Table 20. Device Geometry Definition 31
Table 21. Primary Algorithm-Specific Extended Query Table 32
Table 22. Security Code Area 32

APPENDIX C. BLOCK PROTECTION 33

Programmer Technique 33

In-System Technique 33
Table 23. Programmer Technique Bus Operations 33
Figure 13. Programmer Equipment Group Protect Flowchart 34
Figure 14. Programmer Equipment Chip Unprotect Flowchart 35
Figure 15. In-System Equipment Group Protect Flowchart 36
Figure 16. In-System Equipment Chip Unprotect Flowchart 37

SUMMARY DESCRIPTION

The M29W641D is a 64 Mbit (4Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

V_{CCQ} allows to drive the I/O pin down to 1.8 V. An optional 12 V V_{PP} power supply is provided to speed up customer programming.

First or last block can be protected from accidental programming or erasure (if $\overline{WP}$=VIL).

Each block can be erased independently so it is possible to preserve valid data while old data is erased. The blocks can be protected to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is delivered with all the bits erased (set to 1).

Figure 2. Logic Diagram

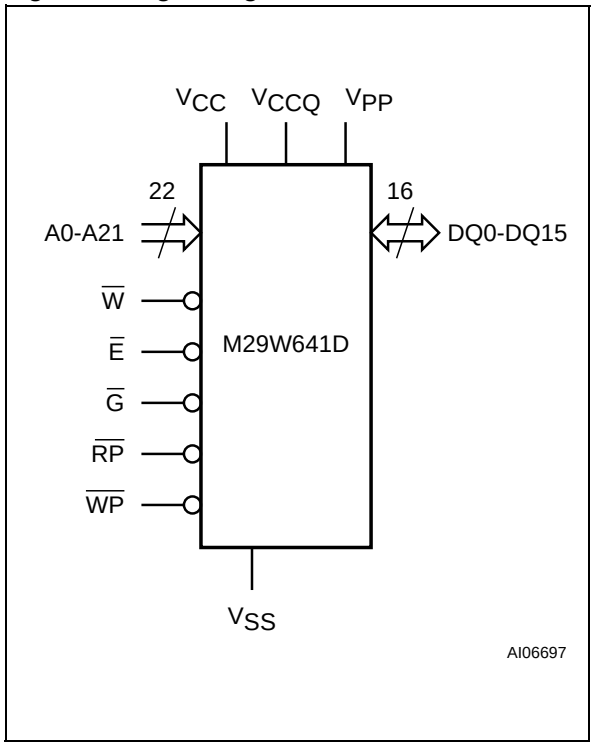
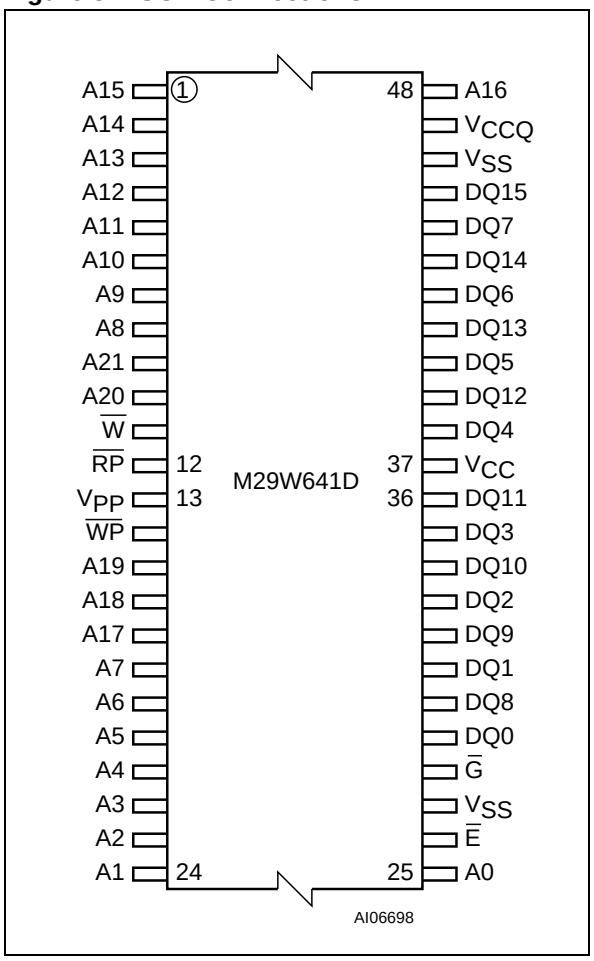


Table 1. Signal Names

A0-A21	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$\overline{WP}$	Write Protect
V_{CC}	Supply Voltage
V_{CCQ}	Supply Voltage for Input/Output
V_{PP}	Supply Voltage for Fast Program (optional)
V_{SS}	Ground

Figure 3. TSOP Connections



SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A21). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ0-DQ7). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ8-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

Write Protect ($\overline{WP}$). The Write Protect pin provides a hardware method of protecting either the first or last block. The Write Protect pin must not be left floating or unconnected.

When Write Protect is Low, V_{IL}, the memory protects either the first or last block; Program and Erase operations in this block are ignored while Write Protect is Low.

When Write Protect is High, V_{IH}, the memory reverts to the previous protection status for this block. Program and Erase operations can now modify the data in this block unless the block is protected using Block Protection.

Reset/Block Temporary Unprotect ($\overline{RP}$). The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if Write Protect ($\overline{WP}$) is at V_{IL}, then one of the two outermost blocks will remain protected even if RP is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, Table 13 and Figure 11, Reset/Block Temporary Unprotect AC Characteristics, for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

V_{PP} (V_{PP}). When the V_{PP} pin is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When the pin is returned to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the Command Interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}, see Figure 12.

Never raise the pin to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

A 0.1µF capacitor should be connected between the V_{PP} pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

V_{CC} Supply Voltage (2.7V to 3.6V). V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase operations, I_{CC3}.

V_{CCQ} Supply Voltage (1.8V to 3.6V). V_{CCQ} provides the power supply for Input and Output.

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Table 2. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A21	Data Inputs/Outputs DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	22C7h
Extended MemoryBlock Verify Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	98h (factory locked, $\overline{WP}$ protects highest block) 18h (not factory locked, $\overline{WP}$ protects highest block) 88h (factory locked, $\overline{WP}$ protects lowest block) 08h (not factory locked, $\overline{WP}$ protects lowest block)

Note: X = V_{IL} or V_{IH}.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Table 2, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 8, Read Mode AC Waveforms, and Table 10, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figure 9 and Figure 10, Write AC Waveforms, and Table 11 and Table 12, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 9, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 2, Bus Operations.

Block Protect and Chip Unprotect. Groups of blocks can be protected against accidental Program or Erase. The whole chip can be unprotected to allow the data inside the blocks to be changed.

Write Protect ($\overline{WP}$) can be used to protect one of the outermost blocks. When Write Protect ($\overline{WP}$) is at V_{IL} one of the two outermost blocks is protected and remains protected regardless of the Block Protection Status or the Reset/Block Temporary Unprotect pin status. For the M29W641DH, it is the highest addressed block that can be protected. For the M29W641DL, it is the lowest.

Block Protect and Chip Unprotect operations are described in Appendix C.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

See Table 3 for a summary of the commands.

Read/Reset Command.

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the timeout of a Block erase operation then the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

Auto Select Command.

The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued. Read CFI Query and Read/Reset commands are accepted in Auto Select mode, all other commands are ignored.

In Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Manufacturer Code for STMicroelectronics is 0020h.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Device Code for the M29W641D is 22C7h.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A12-A21 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

Read CFI Query Command.

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. This command is valid when the device is in the Read Array mode, or when the device is in Autoselected mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Autoselected mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Autoselected mode.

See Appendix B, Table 17 to Table 22 for details on the information contained in the Common Flash Interface (CFI) memory area.

Program Command.

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 4. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Fast Program Commands

There is a Fast Program command available to improve the programming throughput, by writing several adjacent words or bytes in parallel: the Double Word Program command.

Double Word Program Command. The Double Word Program command is used to write a page of two adjacent words in parallel. The two words must differ only for the address A0.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend.

Programming should not be attempted when V_{PP} is not at V_{PPH}.

After programming has started, Bus Read operations in the Bank being programmed output the Status Register content, while Bus Read operations to the other Bank output the contents of the memory array.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Fast Program commands cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Typical Program times are given in Table 4, Program, Erase Times and Program, Erase Endurance Cycles.

Unlock Bypass Command.

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

When V_{PP} is applied to the V_{PP} pin the memory automatically enters the Unlock Bypass mode and the Unlock Bypass Program command can be issued immediately.

Unlock Bypass Program Command.

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the cycle time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

The memory offers accelerated program operations through the V_{PP} pin. When the system asserts V_{PP} on the V_{PP} pin, the memory automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The memory uses the higher voltage on the V_{PP} pin, to accelerate the Unlock Bypass Program operation.

Never raise the V_{PP} pin to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

Unlock Bypass Reset Command.

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass Mode.

Chip Erase Command.

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 4. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

Block Erase Command.

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register section for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command. Typical block erase times are given in Table 4. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Erase Suspend Command.

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within 50 µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

Erase Resume Command.

The Erase Resume command must be used to restart the Program/Erase Controller after an Erase Suspend. The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

Enter Extended Block Command

The device has an extra 32 KWord block (Extended Block) that can only be accessed using the Enter Extended Block command. Three Bus write cycles are required to issue the Extended Block command. Once the command has been issued the device enters Extended Block mode where all Bus Read or Write operations to the Boot Block addresses access the Extended Block. Therefore in Extended Block mode the Boot Blocks are not accessible. All commands are accepted by the command interface.

To exit from the Extended Block mode the Exit Extended Block command must be issued.

The Extended Block can be protected, however once protected the protection cannot be undone.

Exit Extended Block Command.

The Exit Extended Block command is used to exit from the Extended Block mode and return the device to Read mode. Four Bus Write operations are required to issue the command.

Block Protect and Chip Unprotect Commands.

Groups of blocks can be protected against accidental Program or Erase. The whole chip can be unprotected to allow the data inside the blocks to be changed.

Block Protect and Chip Unprotect operations are described in Appendix C.

Table 3. Commands

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Double Word Program	3	555	50	PA0	PD0	PA1	PD1						
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	X	B0										
Erase Resume	1	X	30										
Read CFI Query	1	55	98										
Enter Extended Block	3	555	AA	2AA	55	555	88						
Exit Extended Block	4	555	AA	2AA	55	555	90	X	00				

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal.

Table 4. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1)	Typical after 100k W/E Cycles (1)	Max	Unit
Chip Erase		80	80	400	s
Block Erase (32 KWords)		0.8		6	s
Program (Word)		10		200	µs
Double Word Program		10		200	µs
Chip Program (Word by Word)		40		200	s
Chip Program (Double Word)		10		100	s
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. T_A = 25°C, V_{CC} = 3.3V.

STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in Table 5, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 4, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 5, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 5. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2
Program	Any Address	$\overline{DQ7}$	Toggle	0	–	–
Program During Erase Suspend	Any Address	$\overline{DQ7}$	Toggle	0	–	–
Program Error	Any Address	$\overline{DQ7}$	Toggle	1	–	–
Chip Erase	Any Address	0	Toggle	0	1	Toggle
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle
	Non-Erasing Block	0	Toggle	0	0	No Toggle
Block Erase	Erasing Block	0	Toggle	0	1	Toggle
	Non-Erasing Block	0	Toggle	0	1	No Toggle
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle
	Non-Erasing Block	Data read as normal				
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle
	Faulty Block Address	0	Toggle	1	1	Toggle

Note: Unspecified data bits should be ignored.

Figure 4. Data Polling Flowchart

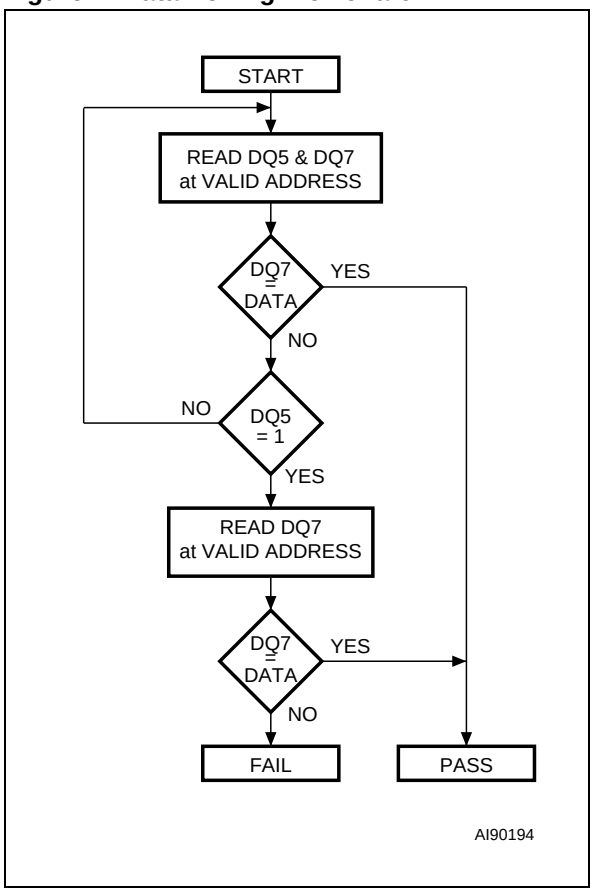
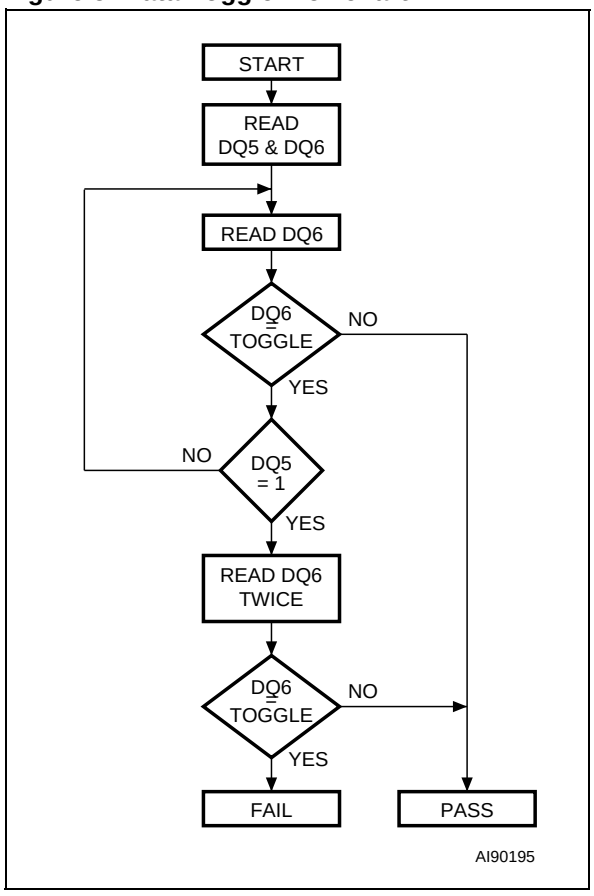


Figure 5. Data Toggle Flowchart



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage (1,2)	–0.6	V_{CC} +0.6	V
V_{CC}	Supply Voltage	–0.6	4	V
V_{ID}	Identification Voltage	–0.6	13.5	V
V_{PP}(3)	Program Voltage	–0.6	13.5	V

Note: 1. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.
3. V_{PP} must not remain at 12V for more than a total of 80hrs.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter	M29W641D				Unit
	70		90		
	Min	Max	Min	Max	
V_{CC} Supply Voltage	3.0	3.6	2.7	3.6	V
Ambient Operating Temperature	–40	85	–40	85	°C
Load Capacitance (C_L)	30		30		pF
Input Rise and Fall Times		10		10	ns
Input Pulse Voltages	0 to V_{CC}		0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 6. AC Measurement I/O Waveform

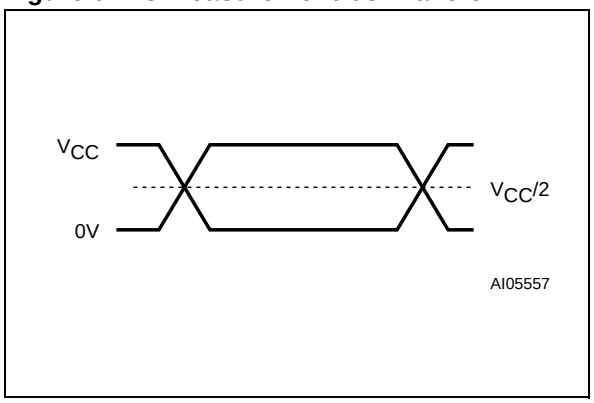


Figure 7. AC Measurement Load Circuit

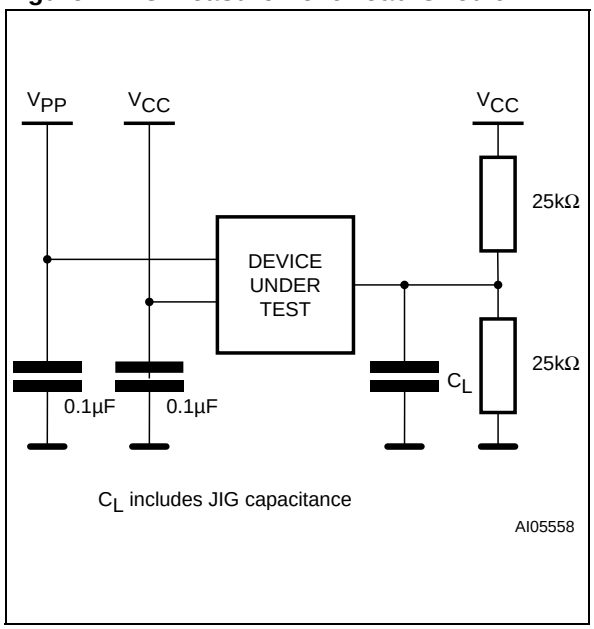


Table 8. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 9. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6 MHz			10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$			100	µA
I_{CC3}	Supply Current (Program/ Erase)	Program/Erase Controller active	V_{PP} pin = V_{IL} or V_{IH}		20	mA
			V_{PP} pin = V_{PP}		20	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			$0.7V_{CC}$	V_{CC} +0.3	V
V_{PP}	Voltage for V_{PP} Program Acceleration	V_{CC} = 3.0V ±10%		11.5	12.5	V
I_{PP}	Current for V_{PP} Program Acceleration	V_{CC} = 3.0V ±10%			15	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA		V_{CC} – 0.4		V
V_{ID}	Identification Voltage			11.5	12.5	V
I_{ID}	Identification Current	A9 = V_{ID}			100	µA
V_{LKO} (1)	Program/Erase Lockout Supply Voltage			1.8	2.3	V

Note: 1. Sampled only, not 100% tested.

Figure 8. Read Mode AC Waveforms

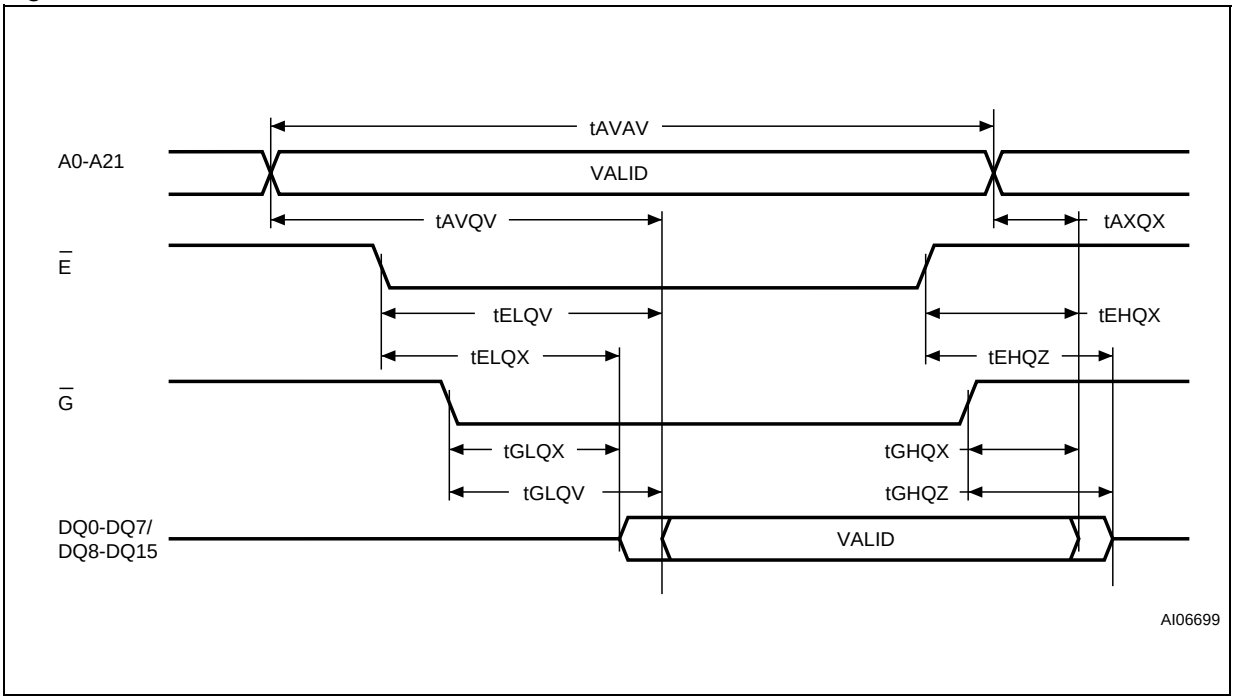


Table 10. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29W641D		Unit
					70	90	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	70	90	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	70	90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	70	90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	30	35	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	25	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	25	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

Note: 1. Sampled only, not 100% tested.

Figure 9. Write AC Waveforms, Write Enable Controlled

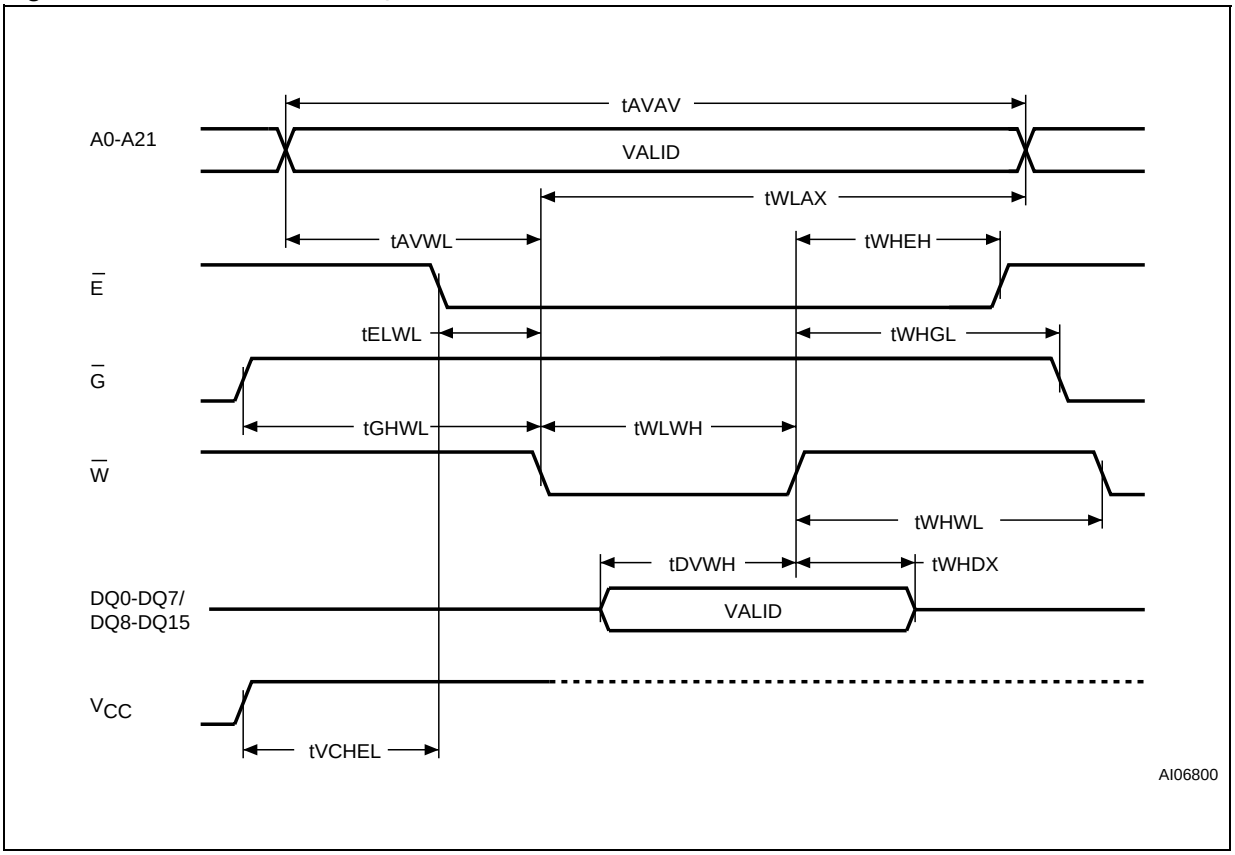


Table 11. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M29W641D		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	50	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	50	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	50	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

Figure 10. Write AC Waveforms, Chip Enable Controlled

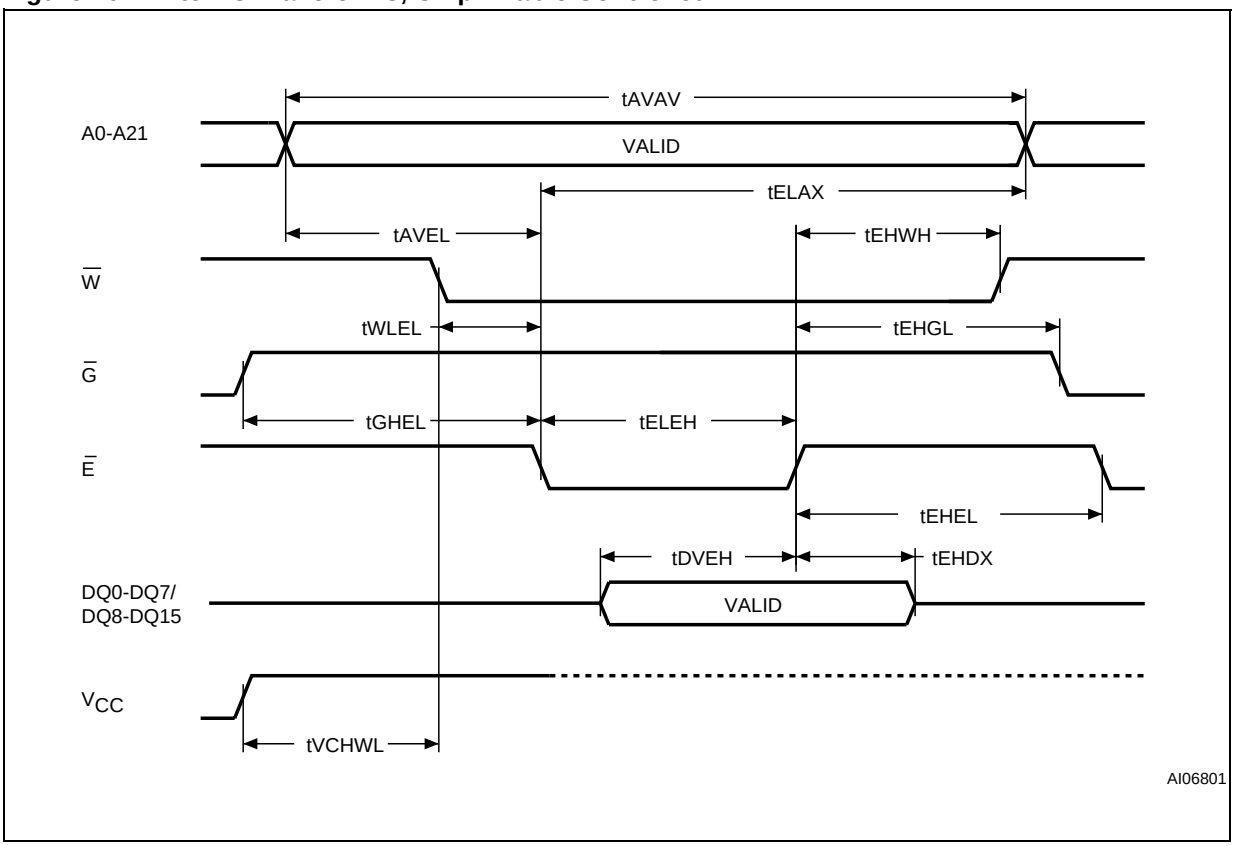


Table 12. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M29W641D		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	50	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	50	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	50	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

Figure 11. Reset/Block Temporary Unprotect AC Waveforms

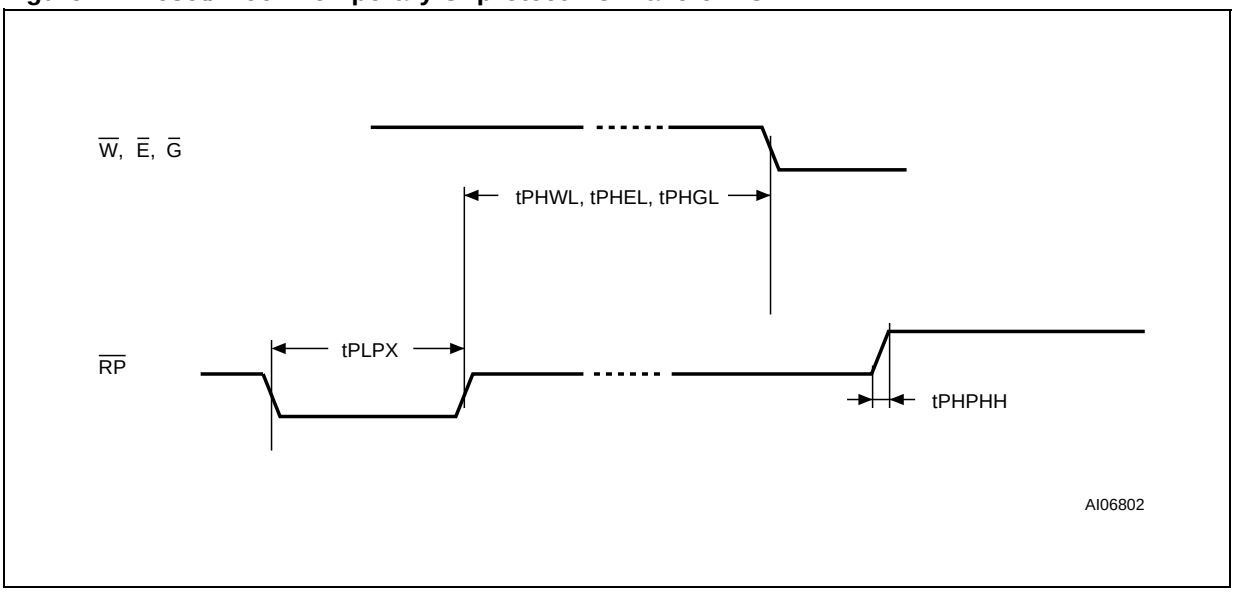
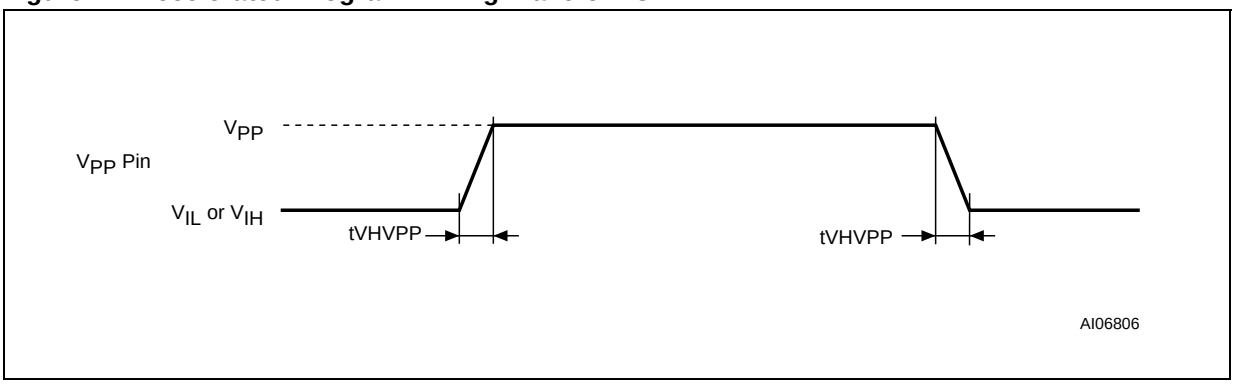


Table 13. Reset/Block Temporary Unprotect AC Characteristics

Symbol	Alt	Parameter		M29W641D		Unit
				70	90	
t_{PHWL} (1) t_{PHEL} t_{PHGL} (1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	Min	500	500	ns
t_{PHPHH} (1)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	Min	500	500	ns
t_{VHVPP} (1)		V_{PP} Rise and Fall Time	Min	250	250	ns

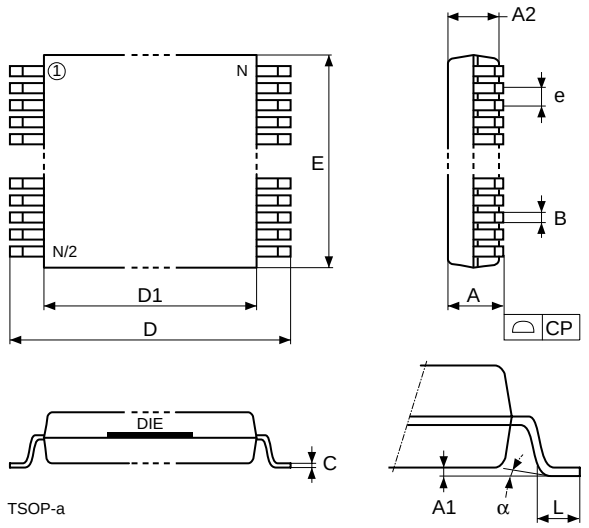
Note: 1. Sampled only, not 100% tested.

Figure 12. Accelerated Program Timing Waveforms



PACKAGE MECHANICAL

TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline



Note: Drawing is not to scale.

TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0279
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

PART NUMBERING

Table 14. Ordering Information Scheme

Example: M29W641D L 70 N 1 T

Device Type
M29

Operating Voltage
W = V_{CC} = 2.7 to 3.6V

Device Function
641D = 64 Mbit (x16), Uniform Block

Array Matrix
H = Protection on highest address block
L = Protection on lowest address block

Speed
70 = 70 ns
90 = 90 ns

Package
N = TSOP48: 12 x 20 mm

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to 1. For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 15. Document Revision History

Date	Version	Revision Details
30-Apr-2002	-01	Document released

APPENDIX A. BLOCK ADDRESSES

Table 16. Block Addresses

Block	KWords	Protection Block Group	Address Range
0	32	Protection Group	000000h–007FFFh (1)
1	32		008000h–00FFFFh
2	32		010000h–017FFFh
3	32		018000h–01FFFFh
4	32	Protection Group	020000h–027FFFh
5	32		028000h–02FFFFh
6	32		030000h–037FFFh
7	32		038000h–03FFFFh
8	32	Protection Group	040000h–047FFFh
9	32		048000h–04FFFFh
10	32		050000h–057FFFh
11	32		058000h–05FFFFh
12	32	Protection Group	060000h–067FFFh
13	32		068000h–06FFFFh
14	32		070000h–077FFFh
15	32		078000h–07FFFFh
16	32	Protection Group	080000h–087FFFh
17	32		088000h–08FFFFh
18	32		090000h–097FFFh
19	32		098000h–09FFFFh
20	32	Protection Group	0A0000h–0A7FFFh
21	32		0A8000h–0AFFFFh
22	32		0B0000h–0B7FFFh
23	32		0B8000h–0BFFFFh
24	32	Protection Group	0C0000h–0C7FFFh
25	32		0C8000h–0CFFFFh
26	32		0D0000h–0D7FFFh
27	32		0D8000h–0DFFFFh
28	32	Protection Group	0E0000h–0E7FFFh
29	32		0E8000h–0EFFFFh
30	32		0F0000h–0F7FFFh
31	32		0F8000h–0FFFFFh

Block	KWords	Protection Block Group	Address Range
32	32	Protection Group	100000h–107FFFh
33	32		108000h–10FFFFh
34	32		110000h–117FFFh
35	32		118000h–11FFFFh
36	32	Protection Group	120000h–127FFFh
37	32		128000h–12FFFFh
38	32		130000h–137FFFh
39	32		138000h–13FFFFh
40	32	Protection Group	140000h–147FFFh
41	32		148000h–14FFFFh
42	32		150000h–157FFFh
43	32		158000h–15FFFFh
44	32	Protection Group	160000h–167FFFh
45	32		168000h–16FFFFh
46	32		170000h–177FFFh
47	32		178000h–17FFFFh
48	32	Protection Group	180000h–187FFFh
49	32		188000h–18FFFFh
50	32		190000h–197FFFh
51	32		198000h–19FFFFh
52	32	Protection Group	1A0000h–1A7FFFh
53	32		1A8000h–1AFFFFh
54	32		1B0000h–1B7FFFh
55	32		1B8000h–1BFFFFh
56	32	Protection Group	1C0000h–1C7FFFh
57	32		1C8000h–1CFFFFh
58	32		1D0000h–1D7FFFh
59	32		1D8000h–1DFFFFh
60	32	Protection Group	1E0000h–1E7FFFh
61	32		1E8000h–1EFFFFh
62	32		1F0000h–1F7FFFh
63	32		1F8000h–1FFFFFh
64	32	Protection Group	200000h–207FFFh
65	32		208000h–20FFFFh
66	32		210000h–217FFFh
67	32		218000h–21FFFFh

Block	KWords	Protection Block Group	Address Range
68	32	Protection Group	220000h–227FFFh
69	32		228000h–22FFFFh
70	32		230000h–237FFFh
71	32		238000h–23FFFFh
72	32	Protection Group	240000h–247FFFh
73	32		248000h–24FFFFh
74	32		250000h–257FFFh
75	32		258000h–25FFFFh
76	32	Protection Group	260000h–267FFFh
77	32		268000h–26FFFFh
78	32		270000h–277FFFh
79	32		278000h–27FFFFh
80	32	Protection Group	280000h–287FFFh
81	32		288000h–28FFFFh
82	32		290000h–297FFFh
83	32		298000h–29FFFFh
84	32	Protection Group	2A0000h–2A7FFFh
85	32		2A8000h–2AFFFFh
86	32		2B0000h–2B7FFFh
87	32		2B8000h–2BFFFFh
88	32	Protection Group	2C0000h–2C7FFFh
89	32		2C8000h–2CFFFFh
90	32		2D0000h–2D7FFFh
91	32		2D8000h–2DFFFFh
92	32	Protection Group	2E0000h–2E7FFFh
93	32		2E8000h–2EFFFFh
94	32		2F0000h–2F7FFFh
95	32		2F8000h–2FFFFFh
96	32	Protection Group	300000h–307FFFh
97	32		308000h–30FFFFh
98	32		310000h–317FFFh
99	32		318000h–31FFFFh
100	32	Protection Group	320000h–327FFFh
101	32		328000h–32FFFFh
102	32		330000h–337FFFh
103	32		338000h–33FFFFh

Block	KWords	Protection Block Group	Address Range
104	32	Protection Group	340000h–347FFFh
105	32		348000h–34FFFFh
106	32		350000h–357FFFh
107	32		358000h–35FFFFh
108	32	Protection Group	360000h–367FFFh
109	32		368000h–36FFFFh
110	32		370000h–377FFFh
111	32		378000h–37FFFFh
112	32	Protection Group	380000h–387FFFh
113	32		388000h–38FFFFh
114	32		390000h–397FFFh
115	32		398000h–39FFFFh
116	32	Protection Group	3A0000h–3A7FFFh
117	32		3A8000h–3AFFFFh
118	32		3B0000h–3B7FFFh
119	32		3B8000h–3BFFFFh
120	32	Protection Group	3C0000h–3C7FFFh
121	32		3C8000h–3CFFFFh
122	32		3D0000h–3D7FFFh
123	32		3D8000h–3DFFFFh
124	32	Protection Group	3E0000h–3E7FFFh
125	32		3E8000h–3EFFFFh
126	32		3F0000h–3F7FFFh
127	32		3F8000h–3FFFFFh

Note: 1. Used as the Extended Block Addresses in Extended Block mode.

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Table 17 to Table 22 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 22, Security Code Area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST.

Table 17. Query Structure Overview

Address	Sub-section Name	Description
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
40h	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
61h	Security Code Area	64 bit unique device number

Note: Query data are always presented on the lowest order data outputs.

Table 18. CFI Query Identification String

Address	Data	Description	Value
10h	0051h	Query Unique ASCII String "QRY"	“Q”
11h	0052h		"R"
12h	0059h		"Y"
13h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	0000h		
15h	0040h	Address for Primary Algorithm extended Query table (see Table 20)	P = 40h
16h	0000h		
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	0000h		
19h	0000h	Address for Alternate Algorithm extended Query table	NA
1Ah	0000h		

Note: Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 19. CFI Query System Interface Information

Address	Data	Description	Value
1Bh	0027h	V_{CC} Logic Supply Minimum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	2.7V
1Ch	0036h	V_{CC} Logic Supply Maximum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	3.6V
1Dh	00B5h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5V
1Eh	00C5h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5V
1Fh	0004h	Typical timeout per single word program = 2^n µs	16µs
20h	0000h	Typical timeout for minimum size write buffer program = 2^n µs	NA
21h	000Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	0000h	Typical timeout for full chip erase = 2^n ms	NA
23h	0004h	Maximum timeout for word program = 2^n times typical	256 µs
24h	0000h	Maximum timeout for write buffer program = 2^n times typical	NA
25h	0003h	Maximum timeout per individual block erase = 2^n times typical	8 s
26h	0000h	Maximum timeout for chip erase = 2^n times typical	NA

Table 20. Device Geometry Definition

Address	Data	Description	Value
27h	0017h	Device Size = 2^n in number of bytes	8 MByte
28h 29h	0001h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh	0000h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	NA
2Ch	0001h	Number of Erase Block Regions. It specifies the number of regions containing contiguous Erase Blocks of the same size.	1
2Dh 2Eh	003Eh 0000h	Region 1 Information Number of identical size erase block = 003Eh+1	64
2Fh 30h	0000h 0000h	Region 1 Information Block size in Region 1 = 0100h * 256 byte	64 Kbyte

Table 21. Primary Algorithm-Specific Extended Query Table

Address	Data	Description	Value
40h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
41h	0052h		"R"
42h	0049h		"I"
43h	0031h	Major version number, ASCII	"1"
44h	0030h	Minor version number, ASCII	"0"
45h	0000h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	0004h	Block Protection 00 = not supported, x = number of sectors per protection group	4
48h	0001h	Temporary Block Unprotect 00 = not supported, 01 = supported	Yes
49h	0004h	Block Protect /Unprotect 04 = M29W400B	4
4Ah	0000h	Simultaneous Operations, 00 = not supported	No
4Bh	0000h	Burst Mode, 00 = not supported, 01 = supported	No
4Ch	0000h	Page Mode, 00 = not supported, 01 = 4 page word, 02 = 8 page word	No
4Dh	00B5h	V_{PP} Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5V
4Eh	00C5h	V_{PP} Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5V

Table 22. Security Code Area

Address	Data	Description
61h	XXXX	64 bit: unique device number
62h	XXXX	
63h	XXXX	
64h	XXXX	

APPENDIX C. BLOCK PROTECTION

Block protection can be used to prevent any operation from modifying the data stored in the memory. Once protected, Program and Erase operations within the protected group fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

To protect the Extended Block issue the Enter Extended Block command and then use either the Programmer or In-System technique. Once protected issue the Exit Extended Block command to return to read mode. The Extended Block protection is irreversible, once protected the protection cannot be undone.

Programmer Technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a group of blocks follow the flowchart in Figure 13, Programmer Equipment Group Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all groups can be unprotected at the same time. To unprotect the chip follow Figure 14, Programmer Equipment Chip Unprotect Flowchart. Table 23, Programmer Technique Bus Operations, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

In-System Technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the memory has been fitted to the system.

To protect a group of blocks follow the flowchart in Figure 15, In-System Equipment Group Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all the groups can be unprotected at the same time. To unprotect the chip follow Figure 16, In-System Equipment Chip Unprotect Flowchart.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 23. Programmer Technique Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A21	Data Inputs/Outputs DQ15-DQ0
Block (Group) Protect(1)	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-A21 Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others = X	X
Block (Group) Protection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A12-A21 Block Address Others = X	Pass = XX01h Retry = XX00h
Block (Group) Unprotection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A12-A21 Block Address Others = X	Retry = XX01h Pass = XX00h

Note: 1. Block Protection Groups are shown in Appendix A, Tables 16.

Figure 13. Programmer Equipment Group Protect Flowchart

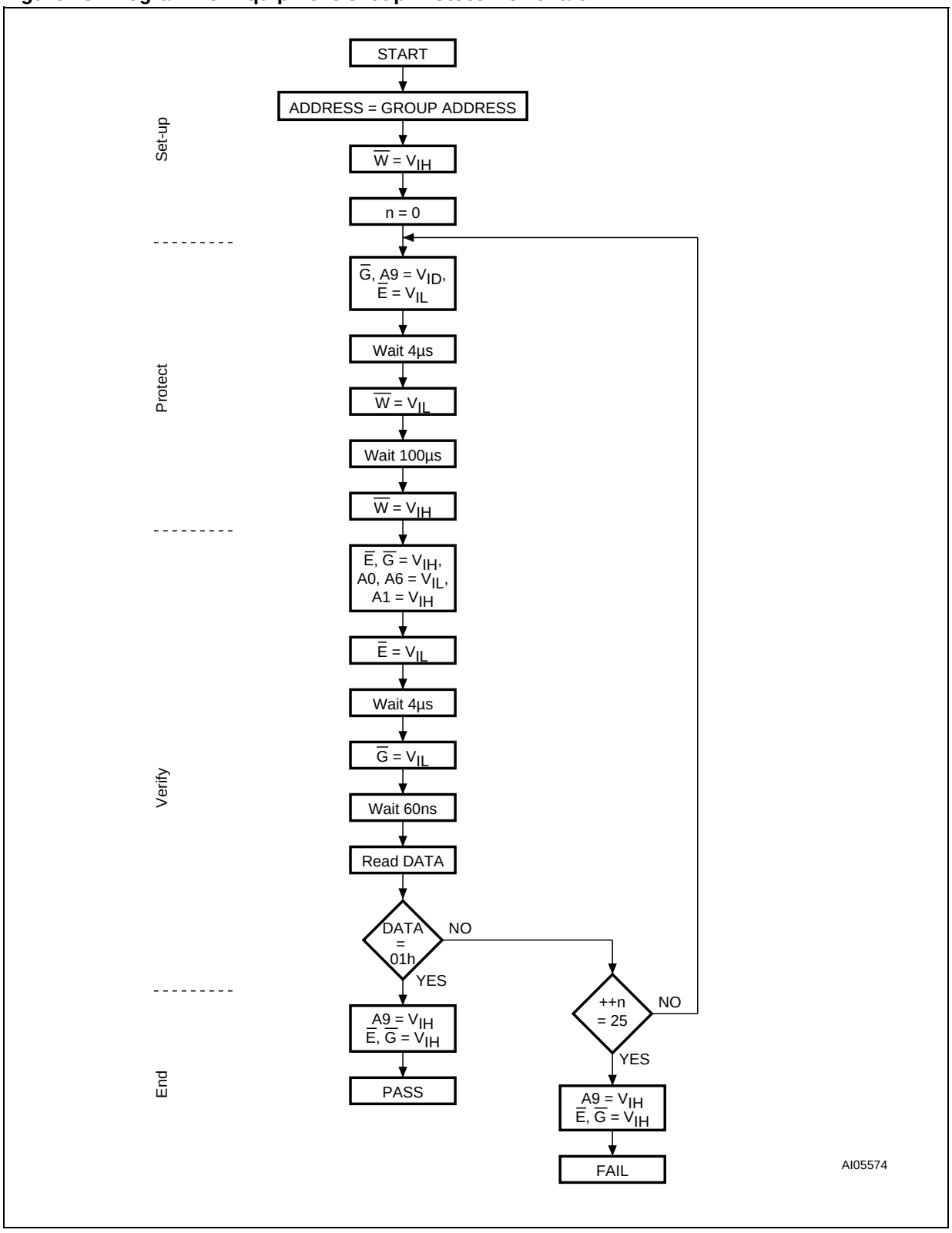


Figure 14. Programmer Equipment Chip Unprotect Flowchart

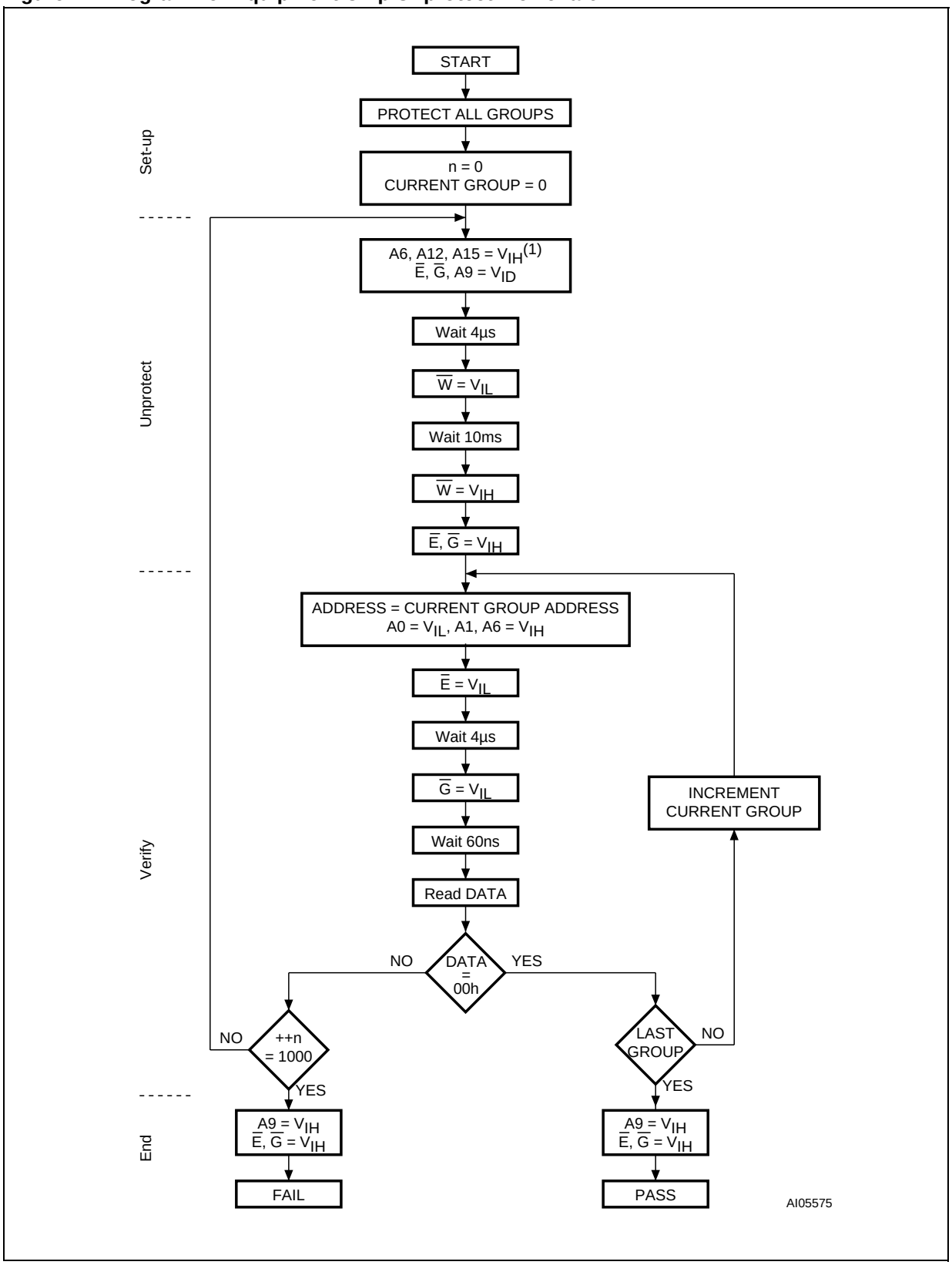


Figure 15. In-System Equipment Group Protect Flowchart

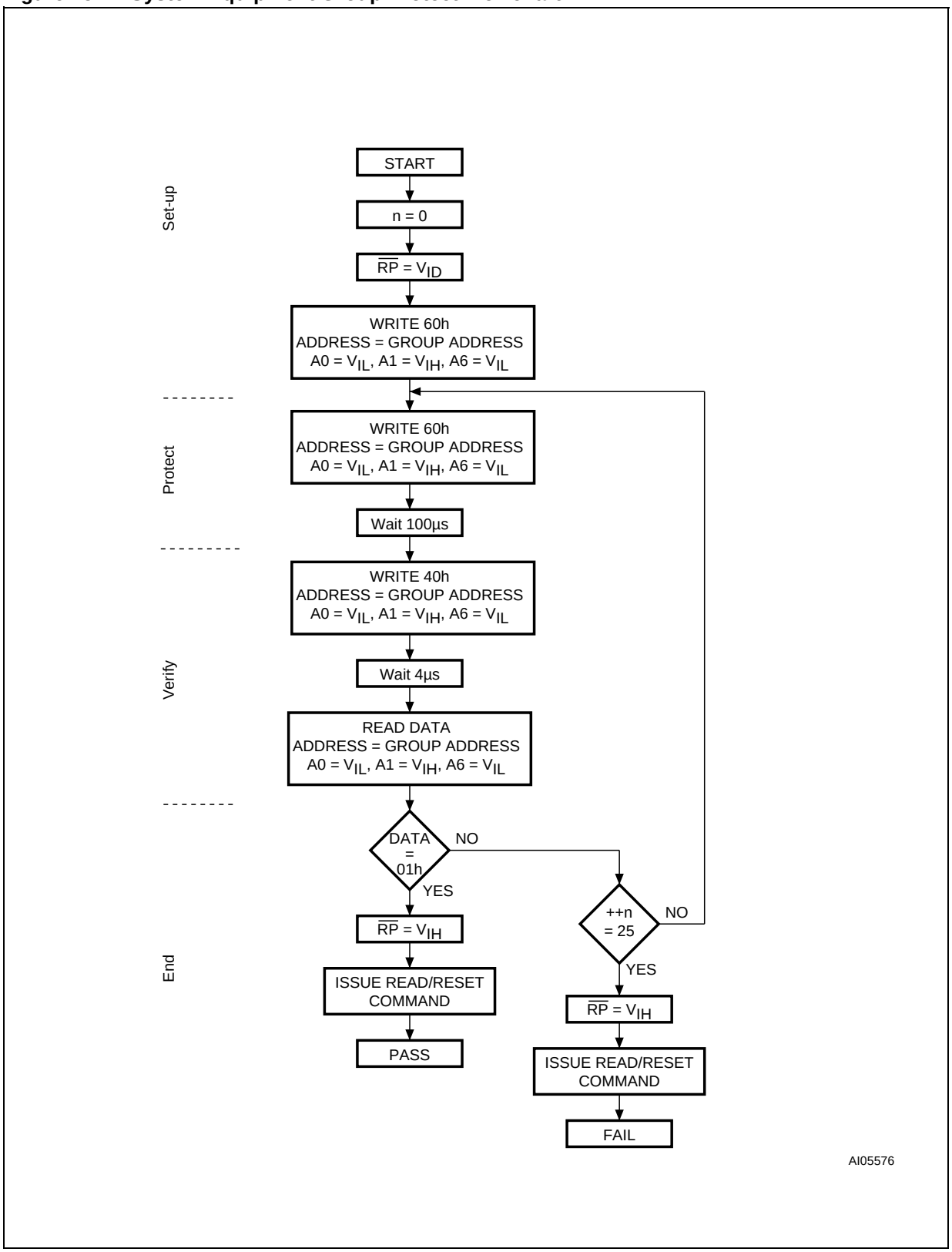
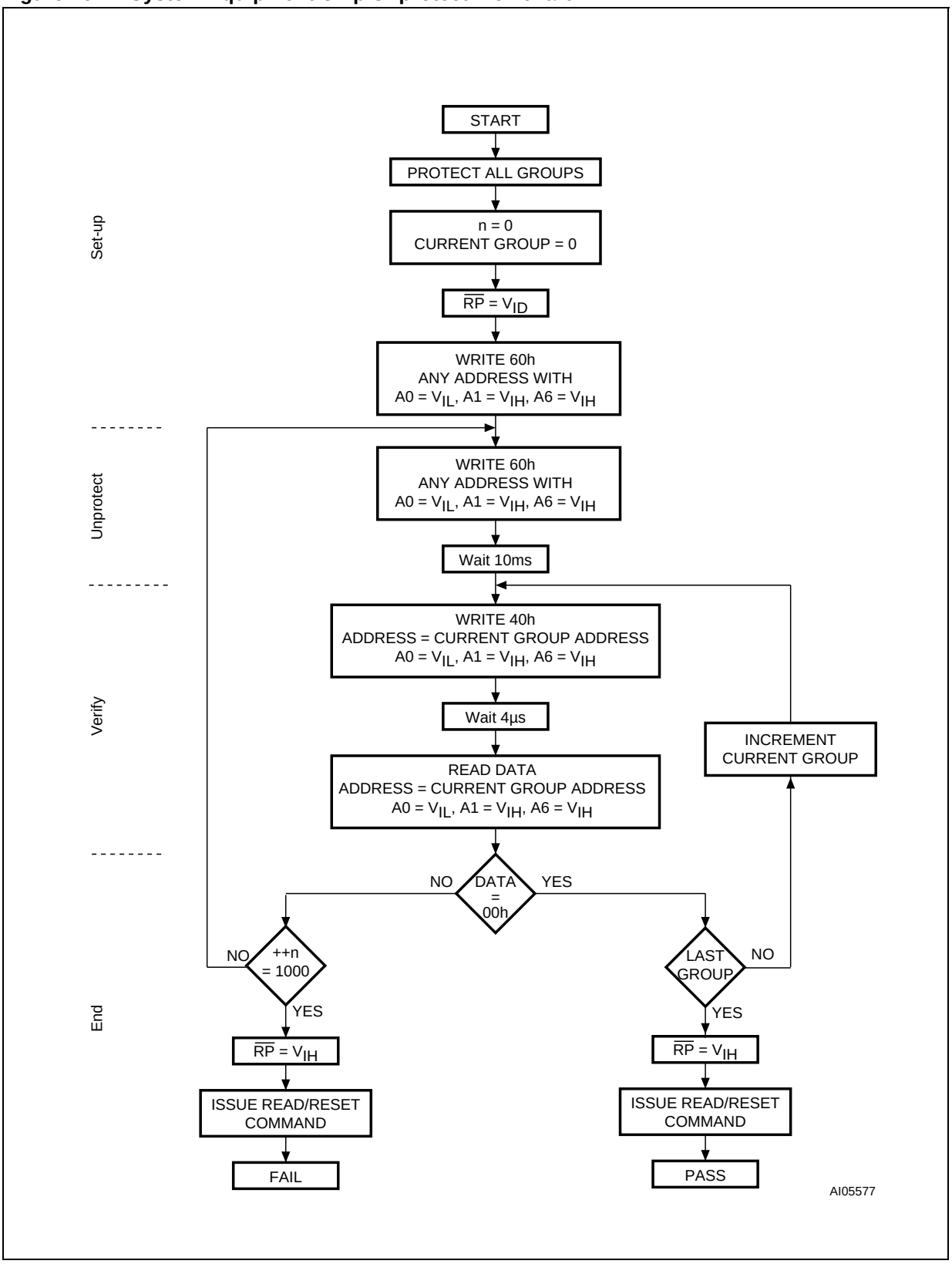


Figure 16. In-System Equipment Chip Unprotect Flowchart



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