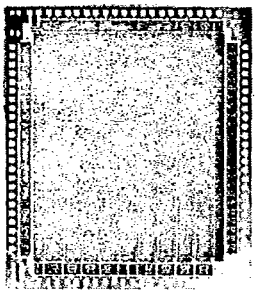
PA40000 Series

T-42-11-09

These data sheets are provided for technical guidance only. The final device performance may vary depending upon the final device design and configuration.



H-1922

PA40000 Series

CMOS Automated Gate Arrays

Features:
- *Low-power silicon-gate CMOS technology*
- *Supply voltage - 5 volts*
- *Typical gate delay from 2 to 20 ns*
- *Single-metal-mask programmable*
- *Implements user-defined logic*
- *Predefined macrocell library*
- *Supported by MIMIC simulation system*
- *Wide range of packaging capabilities*
- *Military temperature range*

The GE/RCA PA40000 series is a family of gate-array products manufactured in a high-performance silicon-gate complementary metal-oxide-semiconductor (CMOS) technology. The products gain their performance from a three (3) micron coplanar oxide-isolated LSI technology. The series contains arrays with gate counts from 640 to 1176 internal logic gates. The array pin counts range from 74 to 102 pins. The arrays are programmable through a single metallization interconnect mask. The arrays are compatible with other CMOS logic and are designed utilizing GE/RCA's extensive design automation technology.

8

SERIES OUTLINE

Device Number	Total Gates	Internal Gates*	Signal Pads†	I/O Buffers	Low-Impedance Buffers (Lo-Z)	Rows	Columns
PA40650	725	640	74	58	16	10	64
PA40850	953	840	86	70	16	10	84
PA41000	1133	1008	94	78	16	12	84
PA41200	1313	1176	102	86	16	14	84

*Utilization of internal gates is typically 80%.

†All devices have four (4) power-supply pins in addition to signal pads.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
(Voltages referenced to V_{SS} Terminal)

DC SUPPLY-VOLTAGE (V_{DD}) ..... -0.5 to +7 V
DC SUPPLY OPERATING VOLTAGE RANGE (V_{DD}) ..... 2 to 6 V
DC INPUT VOLTAGE RANGE, ALL INPUTS (V_{IN}) ..... -0.5 to V_{DD} +0.5 V
DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS (V_{OUT}) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±1 mA
POWER DISSIPATION PER PACKAGE (P_D):
For External Temperature Range -55 to +125°C
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
POWER DISSIPATION PER OUTPUT ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D (CERAMIC) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

PA40000 Series

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS +25°C Min.	LIMITS +25°C Typ.	LIMITS +25°C Max.	LIMITS -55/+125°C Min.	LIMITS -55/+125°C Max.	UNITS
Quiescent Device Current	I_{DD}	$V_{IN} = V_{DD}$ or V_{SS}	5	—	0.01	0.1	—	—	μA/gate
Low-Level Input Voltage	V_{IL}		5	—	—	1.5	—	1.5	V
High-Level Input Voltage	V_{IH}		5	3.5	—	—	3.5	—	V
Low-Level Output Voltage	V_{OL}	$I_{OUT} \leq 1\ \mu A$	5	—	—	0.05	—	0.05	V
High-Level Output Voltage	V_{OH}	$I_{OUT} \leq 1\ \mu A$	5	4.95	—	—	4.95	—	V
Output Low Drive (Sink) Current	I_{OL}								
Standard I/O Buffer		$V_O = 0.4$ V	5	—	1.8	—	0.84	—	mA
		$V_O = 2.5$ V	5	—	5.8	—	3.48	—	
Low-Impedance Buffer (Lo-Z)		$V_O = 0.4$ V	5	—	7.2	—	3.6	—	mA
		$V_O = 2.5$ V	5	—	24	—	14	—	
Output High Drive (Source) Current	I_{OH}								
Standard I/O Buffer		$V_O = 4.6$ V	5	—	1	—	0.48	—	mA
		$V_O = 2.5$ V	5	—	4.5	—	2.16	—	
Low-Impedance Buffer (Lo-Z)		$V_O = 4.6$ V	5	—	4.2	—	2	—	mA
		$V_O = 2.5$ V	5	—	18	—	8.8	—	
Input Leakage Current	I_N	$V_{IN} = V_{DD}$ or V_{SS}	5	—	$\pm 10^{-4}$	±0.1	—	±1	μA
3-State Output Leakage Current	I_{OUT}	$V_{IN} = V_{DD}$ or V_{SS}	5	—	$\pm 10^{-4}$	±0.5	—	±10	μA
Input Capacitance	C_{IN}			—	5	—	—	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS
5-Volt Operation

Number	Gate Description	Propagation Delay t_{PD} (ns) Typical 25°C Fanout 1	Typical 25°C Fanout 4	Typical 125°C Fanout 1	Typical 125°C Fanout 4
	Internal Gates				
1220	Two-Input NAND	2.2	3.6	4	6.8
1240	Four-Input NAND	4	6	7.3	10.9
2310	Exclusive OR	6.1	7.6	11.2	13.9
1410	S-R NAND Flip-Flop	4	6.2	7.3	11.4
8020	Inverting Input Buffer	1	1.5	1.8	2.7
	Peripheral Devices	Capacitive Load (pF) 15 pF	50 pF	Capacitive Load (pF) 15 pF	50 pF
8410	Low-Impedance Output Buffer	3	6	4.6	10.9
8120	Inverting Output Buffer	4.5	12	7.8	22
8110	Non-Inverting Output Buffer	7.5	21	15	41

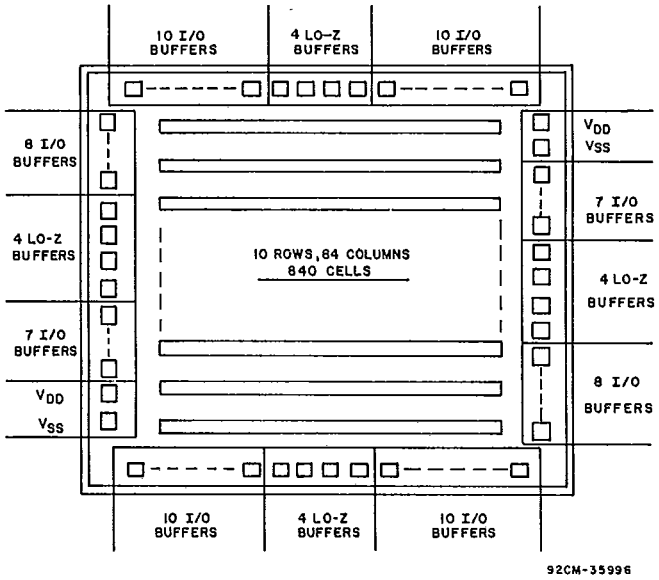


Fig. 1 - Basic layout of PA40850, 840 internal cells.
(Other devices in the family follow similar basic design.)

8

ARRAY DESCRIPTION

The automated gate array (GA) consists of two groups of cells. These include the internal cells and the peripheral cells. Each internal cell is an equivalent two-input gate function. Each equivalent gate would represent 2 n-channel and 2 p-channel transistors.

The heart of the GA is the repetitive internal cells that are combined to form primitive logic functions and then interconnected via a metallization pattern to produce a chip design of a logical application.

The peripheral cells are typically used as input/output circuitry. Peripheral cells include:

- **Input/output protection circuitry** designed to minimize the effect of static discharge through the I/O pins. This is accomplished by using protection diode and resistor networks to both V_{DD} and V_{SS}.
- **High-impedance (Hi-Z)** devices are used primarily as active pull-up or pull-down resistors on gate inputs. They can provide longer propagation delays when necessary. The impedance of these cells is typically 300 kilohms at 5 volts. It is also possible to use these devices in an inverter configuration if the peripheral cell is not being used as an I/O cell.
- **Low-impedance (Lo-Z) cells** are used in order to source and sink TTL levels of current or to drive off-chip capacitive loads at high speed. Low-impedance cells are positioned along the periphery of each array, with their own corresponding signal pads. These devices have very wide tunnels to provide low series impedance for implementing a variety of I/O functions.

The following cells are in the existing cell library:

Internal Cells

Library Code	Logic Function	Gates
1000	Power Cell (V_{DD}, V_{SS} Bus)	1
1100	Dual Inverter	1
1120	Two-Input NOR	2
1130	Three-Input NOR Plus Inv.	2
1140	Four-Input NOR	1
1220	Two-Input NAND	1
1230	Three-Input NAND Plus Inv.	2
1240	Four-Input NAND	2
1300	Non-Inverting Buffer	1
1320	Transmission Gate	1
1410	S-R NAND Flip-Flop	2
1420	S-R NOR Flip-Flop	2
1430	S1,S2-R1,R2 NAND Flip-Flop	3
1440	S1,S2-R1,R2 NAND Flip-Flop	3
1520	Buffer Inverter	1
1530	Double Buffer	2
1580	Tri-State Buffer Control	4
1620	Two-Input AND	2
1630	Three-Input AND	2

PA40000 Series

T-42-11-09

Internal Cells (Cont'd)

Library Code	Logic Function	Gates
1640	Four-Input AND	3
1720	Two-Input OR	2
1730	Three-Input OR	2
1740	Four-Input OR	3
1870	AND-OR Inv. Gate	2
1910	2-1 AND-NOR Gate Plus Inv.	2
1940	2-1 OR-NAND Plus Inv.	2
1970	OR-AND Inv. Gate	2
2030	MS-FF with reset and Hi Clk	7
2040	MS-FF with Lo set, reset and Hi Clk	8
2050	MS-FF with reset and Lo Clk	7
2060	MS-FF with Lo set, reset and Lo Clk	8
2070	MS-FF with Lo set and Lo Clk	7
2080	MS-FF with Lo set and Hi Clk	7
2310	ExOR	3
2340	ExNOR	3
2820	MS-FF with Hi Clk	6
2830	D-Latch with Hi Clk	3
2840	MS-FF with Lo Clk	6
2850	D-Latch with Lo Clk	3

Peripheral Cells

Library Code	Logic Function	Cells
8010	Non-Inv. Input Pad	Pad
8020	Inv. Input Pad	Pad
8030	Passive Input Pad	Pad
8040	Non-Inv. Input Pad w/Pull-Up	Pad
8050	Inv. Input Pad w/Pull-Up	Pad
8060	Passive Input Pad w/Pull-Up	Pad
8070	Non-Inv. Input Pad w/Pull-Down	Pad
8080	Inv. Input Pad w/Pull-Down	Pad
8090	Passive Input Pad w/Pull-Down	Pad
8100	Hi-Z Inv. (Internal Use)	Peripheral
8110	Non-Inv. Output Pad	Pad
8120	Inv. Output Pad	Pad
8130	Passive Output Pad	Pad
8140	Tri-State Output Pad	Pad
8150	Bidirectional Output Pad	Pad
8400	Lo-Z Inv. Left	Peripheral
8410	Lo-Z Inv. Left	Pad
8420	Lo-Z Bidirectional Left	Pad