
**256 × 8-bit static low-voltage RAM with
I²C-bus interface**

PCF8570**CONTENTS**

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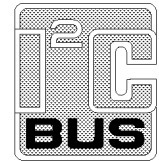
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1 FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 μ A
- Power-saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8 packages.

2 APPLICATIONS

- Telephony:
 - RAM expansion for stored numbers in repertory dialling (e.g. PCD33xxA applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention, such as battery or capacitor-backed.
- Radio, television and video cassette recorder:
 - channel presets
- General purpose:
 - RAM expansion for the microcontroller families PCD33xxA, PCF84CxxxA, P80CLxxx and most other microcontrollers.



3 GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM, organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|------------------------------------|--------------------------|------|------|---------|
| V _{DD} | supply voltage | | 2.5 | 6.0 | |
| I _{DD} | supply current (standby) | f _{SCL} = 0 Hz | – | 15 | μ A |
| I _{DDR} | supply current (power-saving mode) | T _{amb} = 25 °C | – | 400 | nA |
| T _{amb} | operating ambient temperature | | –40 | +85 | °C |
| T _{stg} | storage temperature | | –65 | +150 | °C |

5 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| PCF8570P | DIP8 | plastic dual in-line package; 8 leads (300 mil) | SOT97-1 |
| PCF8570T | SO8 | plastic small outline package; 8 leads; body width 7.5 mm | SOT176-1 |

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6 BLOCK DIAGRAM

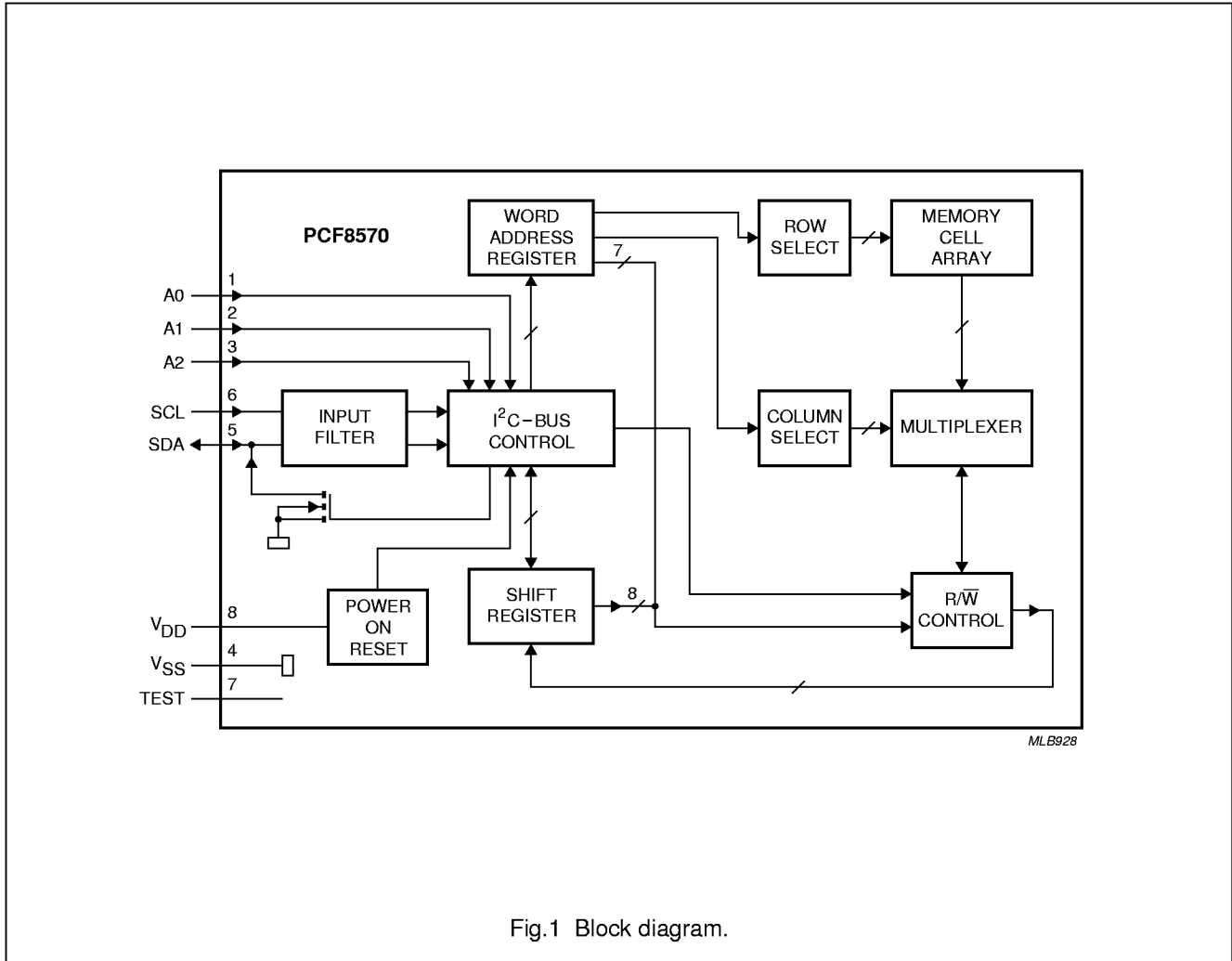


Fig.1 Block diagram.

7 PINNING

| SYMBOL | PIN | DESCRIPTION |
|-----------------|-----|---|
| A0 | 1 | hardware address input 0 |
| A1 | 2 | hardware address input 1 |
| A2 | 3 | hardware address input 2 |
| V _{SS} | 4 | negative supply |
| SDA | 5 | serial data input/output |
| SCL | 6 | serial clock input |
| TEST | 7 | Input for power-saving mode (see section "Power-saving mode"). Also used as a test output during manufacture. TEST should be tied to V _{SS} during normal operation. |
| V _{DD} | 8 | positive supply |

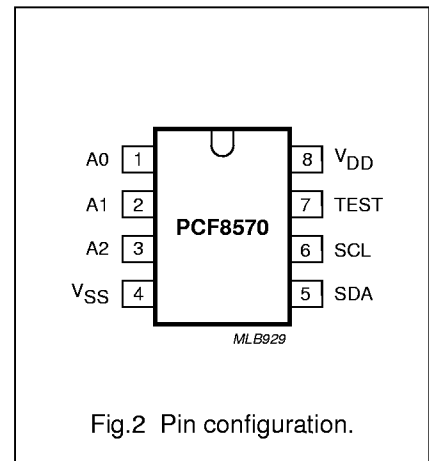


Fig.2 Pin configuration.

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8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

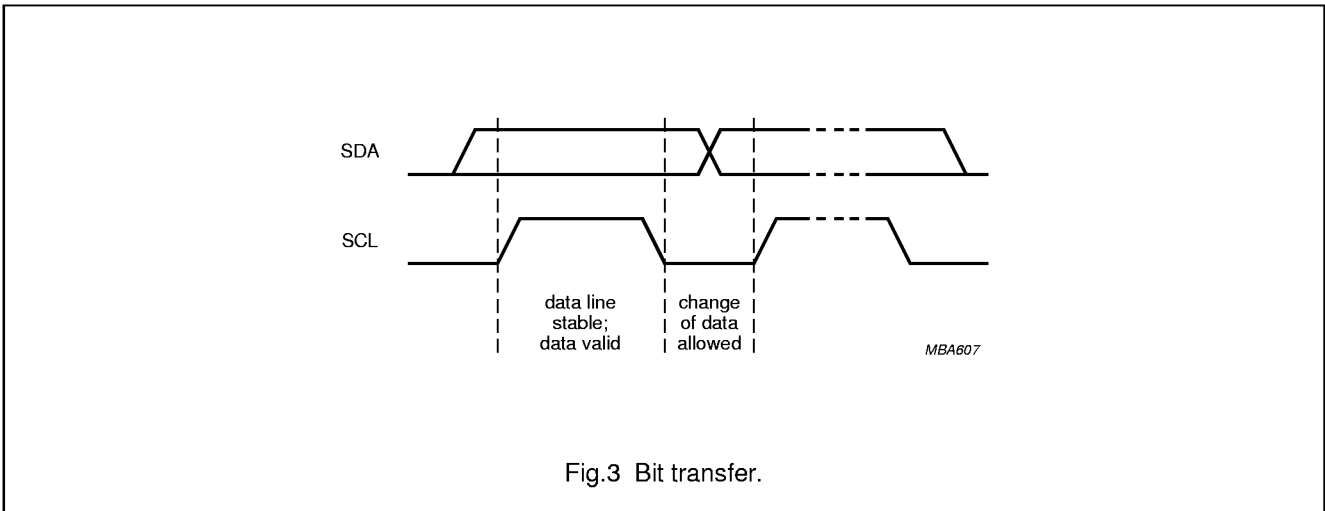


Fig.3 Bit transfer.

8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

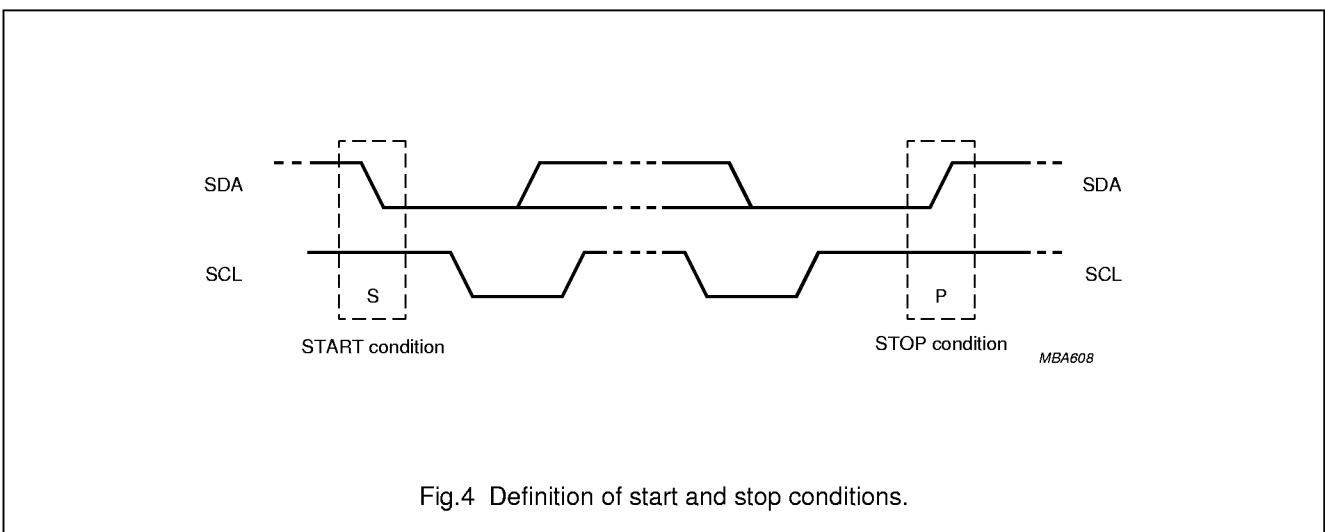


Fig.4 Definition of start and stop conditions.

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8.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

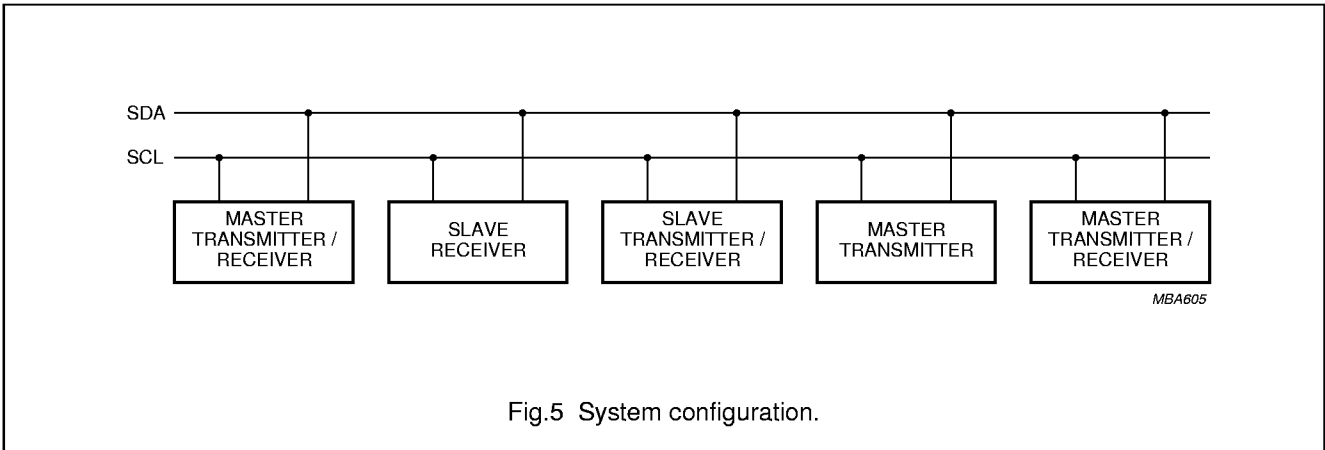


Fig.5 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

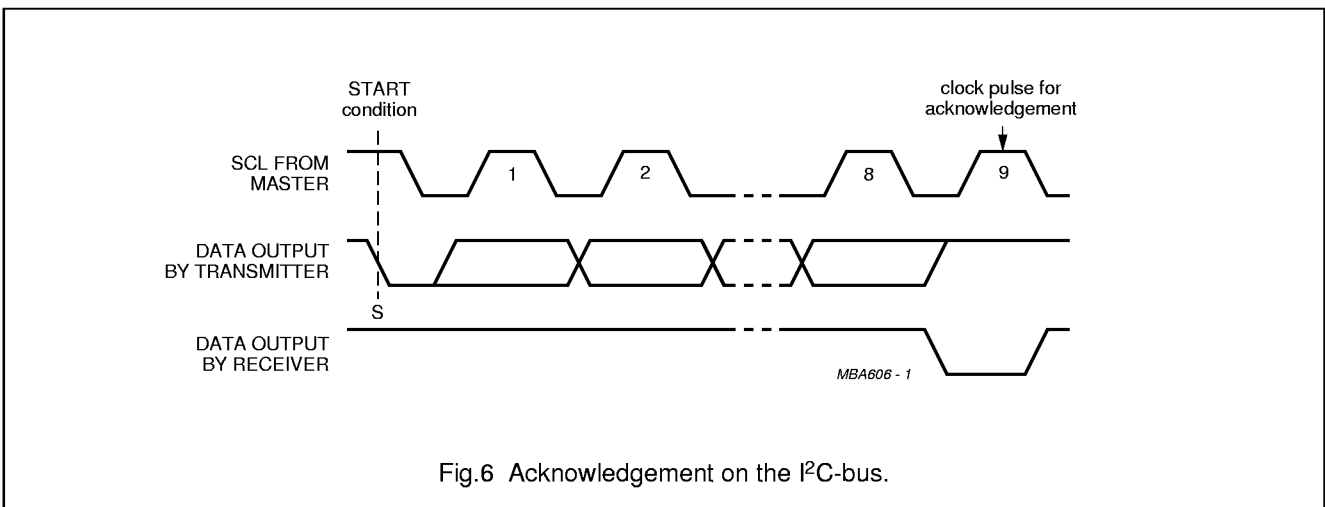


Fig.6 Acknowledgement on the I²C-bus.

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8.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8570 WRITE and READ cycles is shown in Figs 7, 8 and 9.

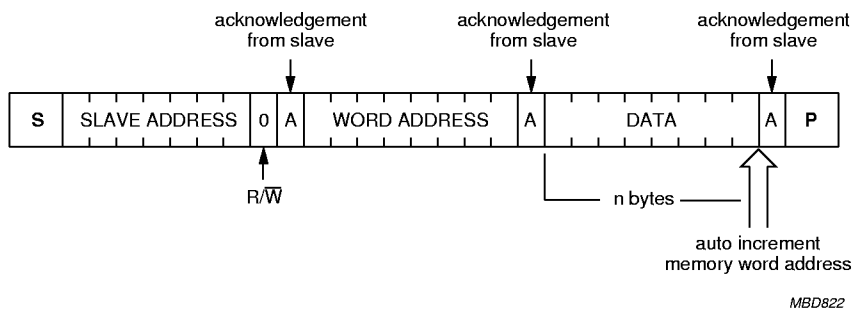


Fig.7 Master transmits to slave receiver (WRITE) mode.

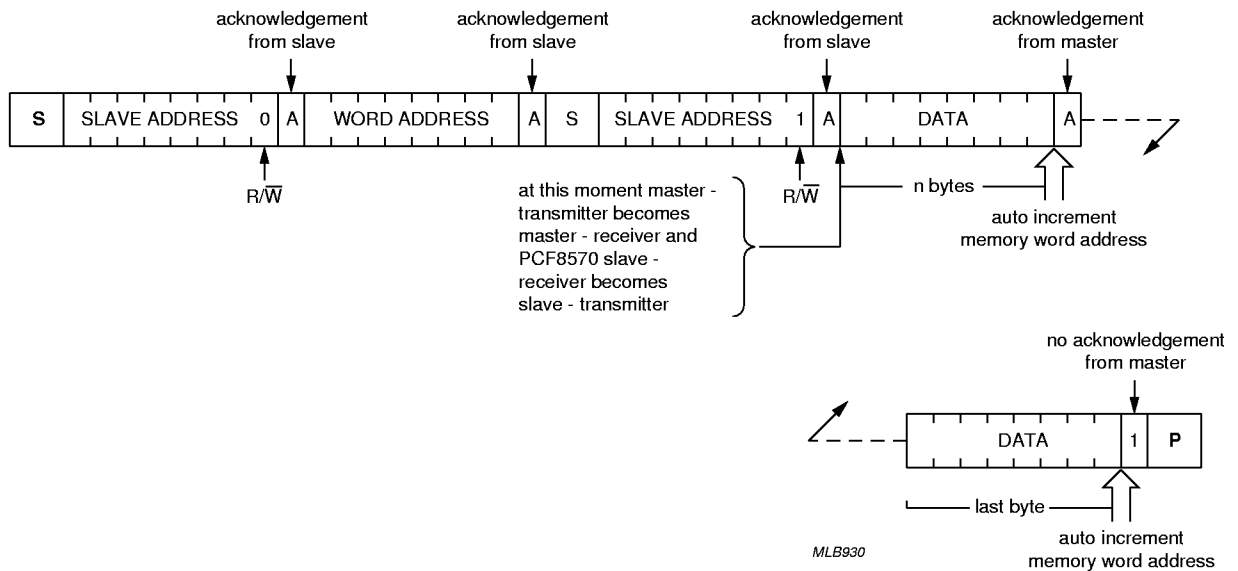


Fig.8 Master reads after setting word address (WRITE word address; READ data).

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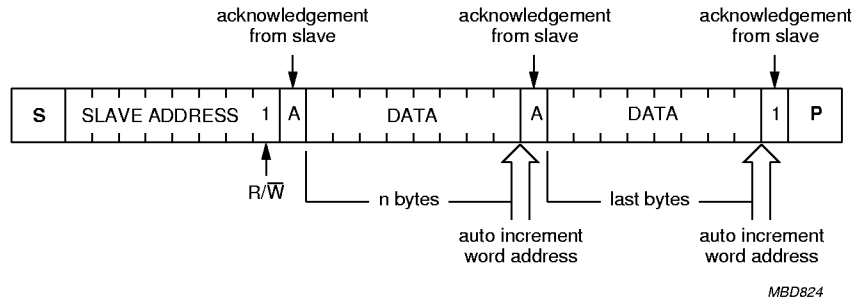


Fig.9 Master reads slave immediately after first byte (READ mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|------------------|-------------------------------------|------|-----------------------|------|
| V _{DD} | supply voltage (pin 8) | -0.8 | +8.0 | V |
| V _I | input voltage (any input) | -0.8 | V _{DD} + 0.8 | V |
| I _I | DC input current | - | ±10 | mA |
| I _O | DC output current | - | ±10 | mA |
| I _{DD} | positive supply current | - | ±50 | mA |
| I _{SS} | negative supply current | - | ±50 | mA |
| P _{tot} | total power dissipation per package | - | 300 | mW |
| P _O | power dissipation per output | - | 50 | mW |
| T _{amb} | operating ambient temperature | -40 | +85 | °C |
| T _{stg} | storage temperature | -65 | +150 | °C |

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under "Handling MOS Devices".

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11 DC CHARACTERISTICS

$V_{DD} = 2.5$ to 6.0 V; $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|-----------------------------------|--|-------------|------|----------------|------|
| Supply | | | | | | |
| V_{DD} | supply voltage | | 2.5 | – | 6.0 | V |
| I_{DD} | supply current standby mode | $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 0$ Hz; $T_{amb} = -25$ to $+70$ °C | – | – | 5 | μA |
| | operating mode | $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 100$ Hz | – | – | 200 | μA |
| V_{POR} | Power-on reset voltage | note 1 | 1.5 | 1.9 | 2.3 | V |
| Inputs, input/output SDA | | | | | | |
| V_{IL} | LOW level input voltage | note 2 | –0.8 | – | $0.3V_{DD}$ | V |
| V_{IH} | HIGH level input voltage | note 2 | $0.7V_{DD}$ | – | $V_{DD} + 0.8$ | V |
| I_{OL} | LOW level output current | $V_{OL} = 0.4$ V | 3 | – | – | mA |
| I_{LI} | input leakage current | $V_I = V_{DD}$ or V_{SS} | –1 | – | +1 | μA |
| Inputs A0, A1, A2 and TEST | | | | | | |
| I_{LI} | input leakage current | $V_I = V_{DD}$ or V_{SS} | –250 | – | +250 | nA |
| Inputs SCL and SDA | | | | | | |
| C_i | input capacitance | $V_I = V_{SS}$ | – | – | 7 | pF |
| Low V_{DD} data retention | | | | | | |
| V_{DDR} | supply voltage for data retention | | 1 | – | 6 | V |
| I_{DDR} | supply current | $V_{DDR} = 1$ V | – | – | 5 | μA |
| | | $V_{DDR} = 1$ V; $T_{amb} = -25$ to $+70$ °C | – | – | 2 | μA |
| Power-saving mode (see Figs 13 and 14) | | | | | | |
| I_{DDR} | supply current | TEST = V_{DD} ; $T_{amb} = 25$ °C | – | 50 | 400 | nA |
| t_{HD2} | recovery time | | – | 50 | – | μs |

Notes

- The Power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a Power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
- If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.

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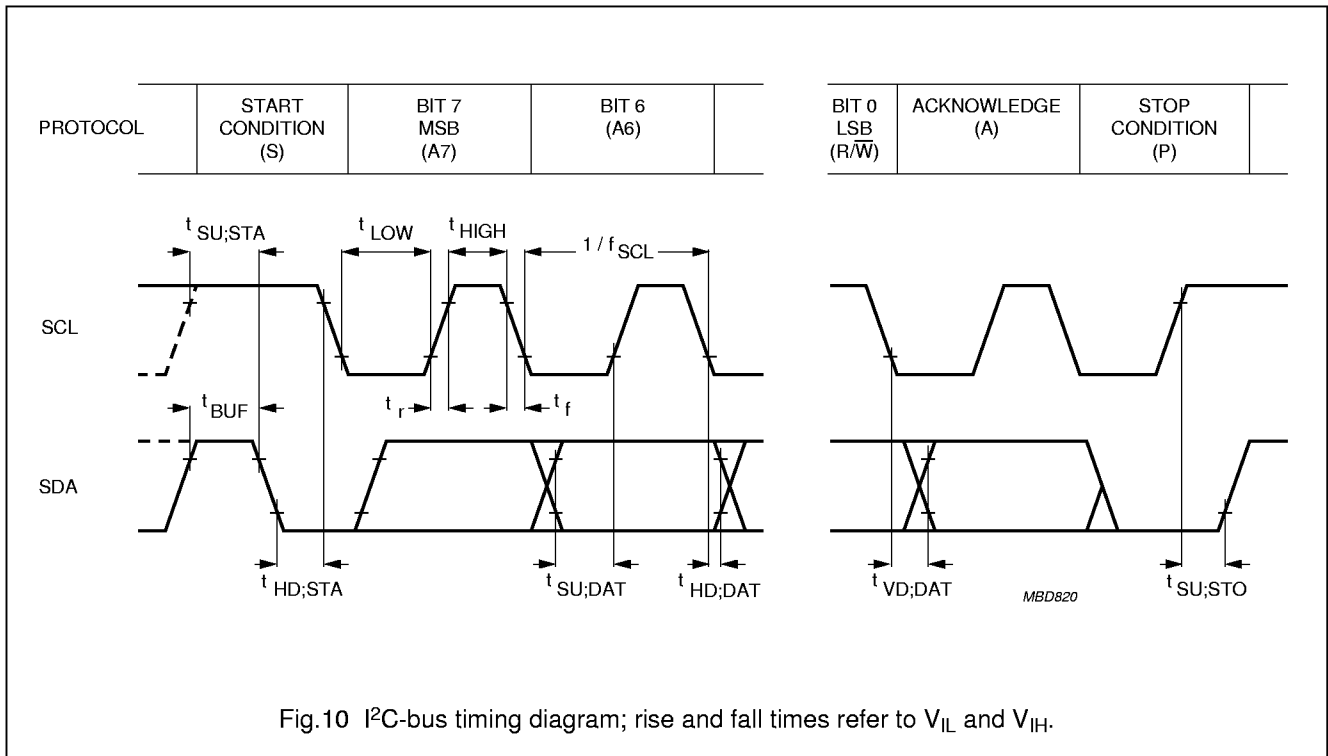
12 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|------------------------------|------|------|------|------|
| I²C-bus timing (see Fig.10; note 1) | | | | | |
| f _{SCL} | SCL clock frequency | – | – | 100 | kHz |
| t _{SP} | tolerable spike width on bus | – | – | 100 | ns |
| t _{BUF} | bus free time | 4.7 | – | – | μs |
| t _{SU;STA} | START condition set-up time | 4.7 | – | – | μs |
| t _{HD;STA} | START condition hold time | 4.0 | – | – | μs |
| t _{LOW} | SCL LOW time | 4.7 | – | – | μs |
| t _{HIGH} | SCL HIGH time | 4.0 | – | – | μs |
| t _r | SCL and SDA rise time | – | – | 1.0 | μs |
| t _f | SCL and SDA fall time | – | – | 0.3 | μs |
| t _{SU;DAT} | data set-up time | 250 | – | – | ns |
| t _{HD;DAT} | data hold time | 0 | – | – | ns |
| t _{VD;DAT} | SCL LOW-to-data out valid | – | – | 3.4 | μs |
| t _{SU;STO} | STOP condition set-up time | 4.0 | – | – | μs |

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure "The I²C-bus and how to use it". This brochure may be ordered using the code 9398 393 40011.

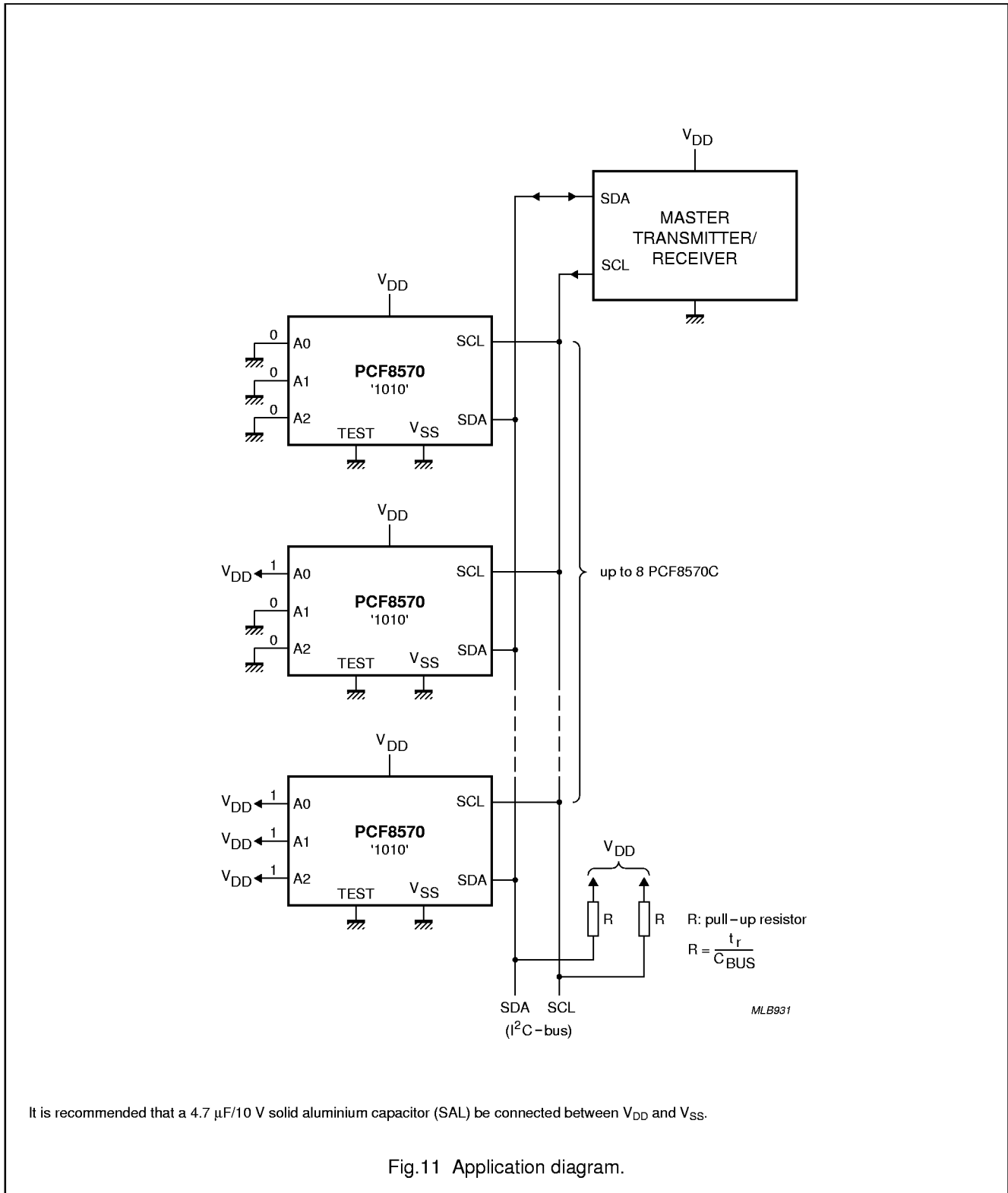


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13 APPLICATION INFORMATION

13.1 Application example



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13.2 Slave address

The PCF8570 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.12).

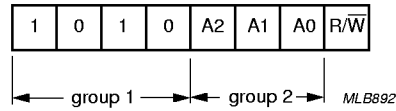
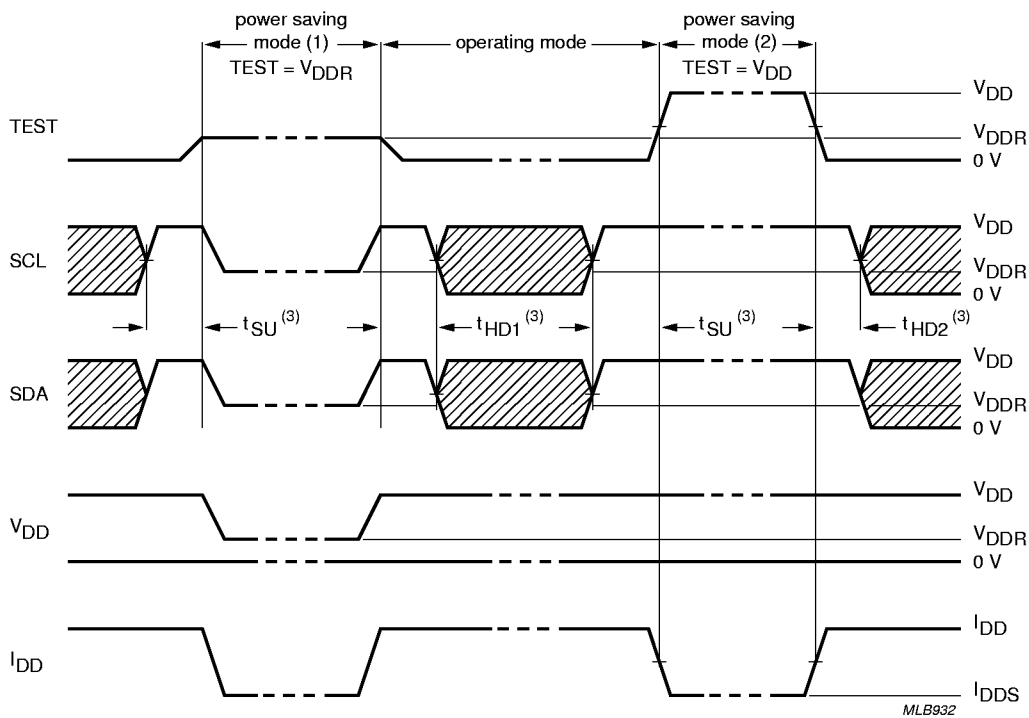


Fig.12 Slave address.

13.3 Power-saving mode

With the condition TEST = V_{DD} or V_{DDR} the PCF8570 goes into the power-saving mode and I²C-bus logic is reset.

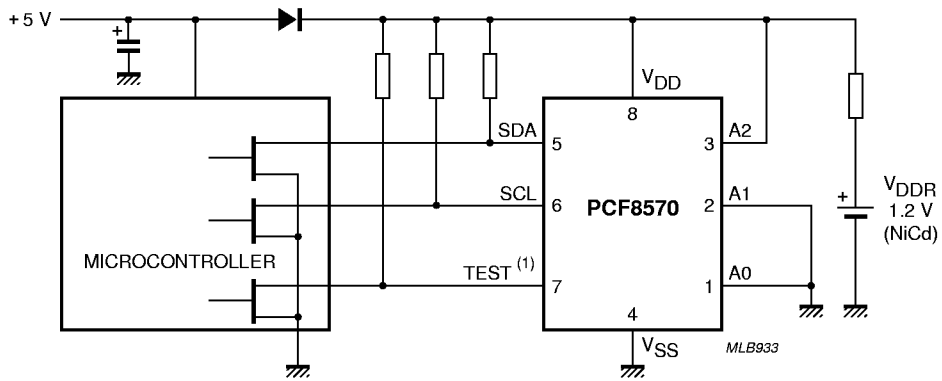


- (1) Power-saving mode without 5 V supply voltage.
- (2) Power-saving mode with 5 V supply voltage.
- (3) t_{SU} and t_{HD1} ≥ 4 μs and t_{HD2} ≥ 50 μs.

Fig.13 Timing for power-saving mode.

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It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

(1) In the operating mode TEST = 0 V; in the power-saving mode TEST = V_{DDR}.

Fig.14 Application example for power-saving mode.

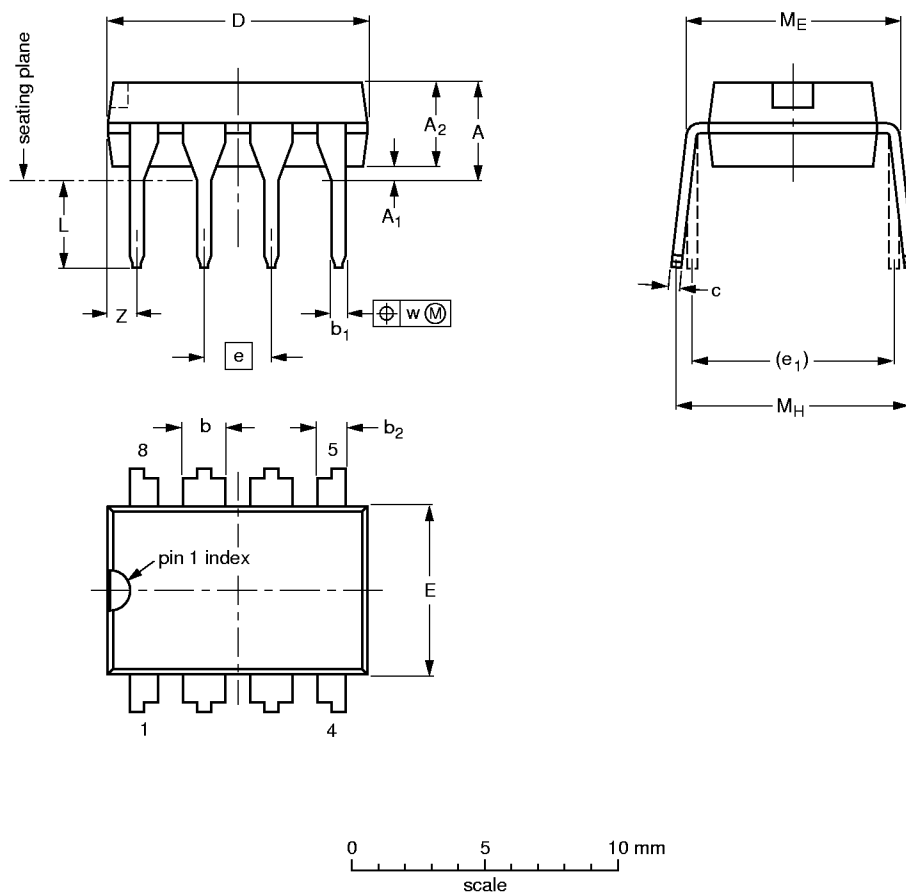
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14 PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.14 | 0.53 0.38 | 1.07 0.89 | 0.36 0.23 | 9.8 9.2 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.045 | 0.021 0.015 | 0.042 0.035 | 0.014 0.009 | 0.39 0.36 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.045 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

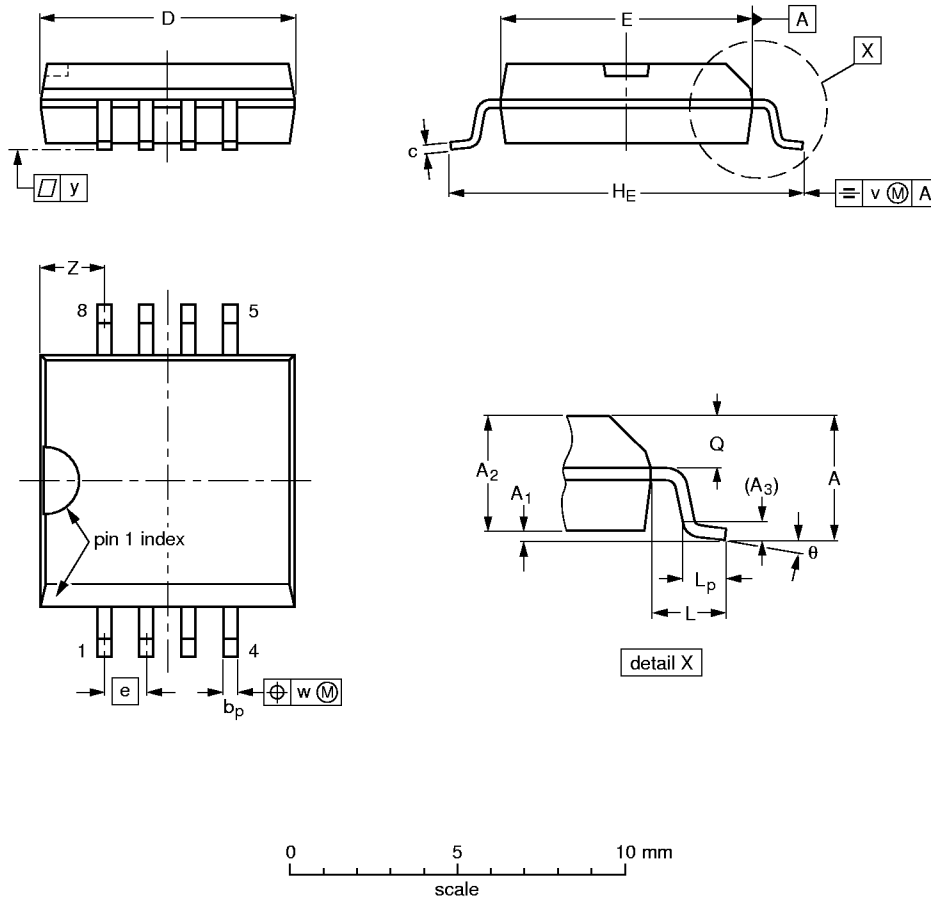
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT97-1 | 050G01 | MO-001AN | | | | 92-11-17 95-02-04 |

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S08: plastic small outline package; 8 leads; body width 7.5 mm

SOT176-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.3 0.1 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 7.65 7.45 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.45 | 1.1 0.45 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 2.0 1.8 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.30 0.29 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.057 | 0.043 0.018 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.079 0.071 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT176-1 | | | | | 95-02-25 97-05-22 |

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15 SOLDERING

15.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

15.2 Through-hole mount packages

15.2.1 SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 Surface mount packages

15.3.1 REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

15.3.2 WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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15.4 Suitability of IC packages for wave, reflow and dipping soldering methods

| MOUNTING | PACKAGE | SOLDERING METHOD | | |
|--------------------|---------------------------------|-----------------------------------|-----------------------|----------|
| | | WAVE | REFLOW ⁽¹⁾ | DIPPING |
| Through-hole mount | DBS, DIP, HDIP, SDIP, SIL | suitable ⁽²⁾ | – | suitable |
| Surface mount | BGA, SQFP | not suitable | suitable | – |
| | HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable ⁽³⁾ | suitable | – |
| | PLCC ⁽⁴⁾ , SO, SOJ | suitable | suitable | – |
| | LQFP, QFP, TQFP | not recommended ⁽⁴⁾⁽⁵⁾ | suitable | – |
| | SSOP, TSSOP, VSO | not recommended ⁽⁶⁾ | suitable | – |

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

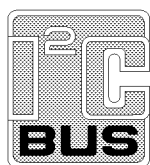
16 DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.