

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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SHEET	15	16	17	18	19	20														

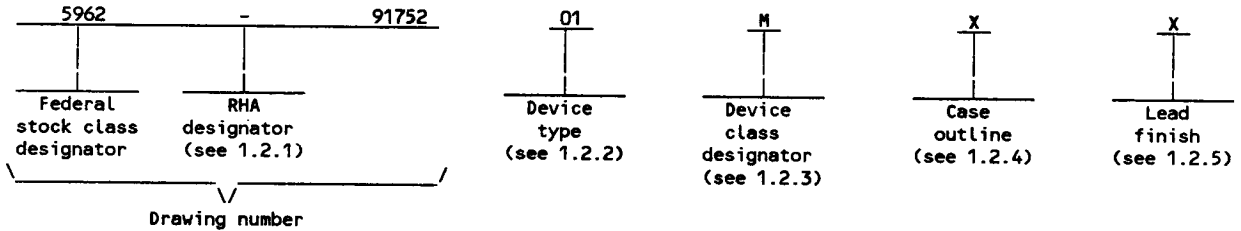
REV STATUS OF SHEETS	REV																			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Gary L. Gross	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444			
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY William J. Johnson			MICROCIRCUITS, MEMORY, DIGITAL, CMOS 512K X 8-BIT UVEPROM, MONOLITHIC SILICON	
	APPROVED BY Michael A. Frye				
	DRAWING APPROVAL DATE 93-01-18	SIZE A	CAGE CODE 67268		5962-91752
	REVISION LEVEL	SHEET	1		OF

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) Levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>Access time</u>
01		(512K x 8) UVEPROM	250 ns
02		(512K x 8) UVEPROM	200 ns
03		(512K x 8) UVEPROM	170 ns
04		(512K x 8) UVEPROM	150 ns
05		(512K x 8) UVEPROM	120 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

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1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDIP2-T32 or GDIP1-T32	32	Dual-in-line package <u>2/</u>
Y	CQCC1-N32	32	Rectangular leadless chip carrier <u>2/</u>

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 3/

Storage temperature range	-65°C to +150°C
All input or output voltage with respect to ground	-0.6 V dc to V_{CC} +0.5 V dc
Voltage on A9 with respect to ground	-0.6 V dc to +13.0 V dc
V_{PP} supply voltage range with respect to ground during programming	-0.6 V dc to +13.5 V dc
V_{CC} supply voltage range with respect to ground	-0.6 V dc to +7.0 V dc
Maximum power dissipation (P_D)	330 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal Resistance, junction-to-case (θ_{JC}):	
Case X and Y	See MIL-STD-1835
Junction temperature (T_J)	+150°C <u>4/</u>
Endurance	50 cycles/byte, minimum
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent <u>5/</u>
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2/ Lid shall be transparent to permit ultraviolet light erasure.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ When a Qualified Manufacturer's List (QML) source exists, a value shall be provided.

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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

- MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of the documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

- JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Application for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

- ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

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2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required, in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Processing EPROMs. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.5.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.5.3 Erase of EPROMs. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.5 herein.

3.5.4 Verification of erasure of programmability of EPROMs. When specified, devices shall be verified as either programmed to the specified pattern (see 4.6) or erased (see 4.5). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.6.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input load current	I _{LI}	V _{IN} = 0 V to 5.5 V	1, 2, 3	ALL	-10	+10	μA
Output leakage current	I _{LO}	V _{OUT} = 0 V to 5.5 V	1, 2, 3	ALL	-10	+10	μA
V _{pp} load current head	I _{pp1}	V _{pp} = 5.5 V	1, 2, 3	ALL		100	μA
V _{CC} active current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0 mA, V _{CC} = V _{pp} = 5.5 V, f = 1/t _{AVQV}	1, 2, 3	ALL		60	mA
V _{CC} standby current (TTL)	I _{CC2}	$\overline{CE} = V_{IH}$, V _{CC} = 5.5 V	1, 2, 3	ALL		1	mA
V _{CC} super standby current (CMOS)	I _{CC3}	$\overline{CE} = V_{CC} \pm 0.3$ V, V _{CC} = 5.5 V	1, 2, 3	ALL		100	μA
Input low voltage	V _{IL}		1, 2, 3	ALL	-0.1 1/	0.8	V
Input high voltage	V _{IH}		1, 2, 3	ALL	2.0	V _{CC} +0.5 V 1/	V
Output low voltage	V _{OL}	I _{OL} = 2.1 mA, V _{IL} = 0.8 V, V _{IH} = 2.0 V	1, 2, 3	ALL		0.45	V
Output high voltage	V _{OH}	I _{OH} = -400 μA, V _{IL} = 0.8 V, V _{IH} = 2.0 V	1, 2, 3	ALL	2.4		V
Input capacitance 1/ 2/	C _{IN}	T _A = +25°C, f = 1 MHz, V _{IN} = 0 V, see 4.4.1e	4	ALL		12	pF
Output capacitance 1/ 2/	C _{OUT}	T _A = +25°C, f = 1 MHz, V _{OUT} = 0 V, see 4.4.1e	4	ALL		15	pF
Functional tests		See 4.4.1c	7, 8	ALL			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _c ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to output delay	t _{AVQV}	$\overline{CE} = \overline{OE} = V_{IL}$, see figures 3 and 4 as applicable	9, 10, 11	01 02 03 04 05		250 200 170 150 120	ns
\overline{CE} to output delay	t _{ELQV}	$\overline{OE} = V_{IL}$, see figures 3 and 4 as applicable	9, 10, 11	01 02 03 04 05		250 200 170 150 120	ns
\overline{OE} to output delay	t _{OLQV}	$\overline{CE} = V_{IL}$, see figures 3 and 4 as applicable	9, 10, 11	01 02 03 04 05		100 75 65 65 50	ns
\overline{CE} or \overline{OE} high to output float	t _{EHQZ} t _{OHQZ} <u>3/</u>	\overline{CE} or $\overline{OE} = V_{IL}$, see figures 3 and 4 as applicable	9, 10, 11	01 02 03 04 05		60 60 50 50 50	ns
Output hold from addresses, \overline{CE} or \overline{OE} which- ever occurred first	t _{AXQX} <u>3/</u>	see figures 3 and 4 as applicable	9, 10, 11	ALL	0		ns

- 1/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
 2/ All pins not being tested shall be grounded.
 3/ May not be tested, but shall be guaranteed to the limits specified in table I.

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Device types	ALL
Case outlines	X and Y
Terminal number	Terminal symbol
1	V _{PP}
2	A ₁₆
3	A ₁₅
4	A ₁₂
5	A ₇
6	A ₆
7	A ₅
8	A ₄
9	A ₃
10	A ₂
11	A ₁
12	A ₀
13	I/O ₀
14	I/O ₁
15	I/O ₂
16	GND
17	I/O ₃
18	I/O ₄
19	I/O ₅
20	I/O ₆
21	I/O ₇
22	$\overline{CE}/(\overline{E})$
23	A ₁₀
24	$\overline{OE}/(\overline{G})$
25	A ₁₁
26	A ₉
27	A ₈
28	A ₁₃
29	A ₁₄
30	A ₁₇
31	A ₁₈
32	V _{CC}

FIGURE 1. Terminal connections.

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Mode	Pins						
	\overline{CE}	\overline{OE}	A ₀	A ₉	V _{pp}	Outputs	
Read	V _{IL}	V _{IL}	X	X	V _{CC}	D _{OUT}	
Standby (TTL)	V _{IH}	X	X	X	V _{CC}	Hi-Z	
Standby (CMOS)	V _{CC} ±0.3 V	X	X	X	V _{CC}	Hi-Z	
Output disable	V _{IL}	V _{IH}	X	X	V _{CC}	Hi-Z	
Program	V _{IL}	V _{IH}	X	X	V _{pp}	D _{IN}	
Program verify	V _{IH}	V _{IL}	X	X	V _{pp}	D _{OUT}	
Program inhibit	V _{IH}	V _{IH}	X	X	V _{pp}	Hi-Z	
Auto select (see notes 1 and 3)	Manufacturer code	V _{IL}	V _{IL}	V _{IL}	V _H	V _{CC}	
	Device	V _{IL}	V _{IL}	V _{IH}	V _H	V _{CC}	

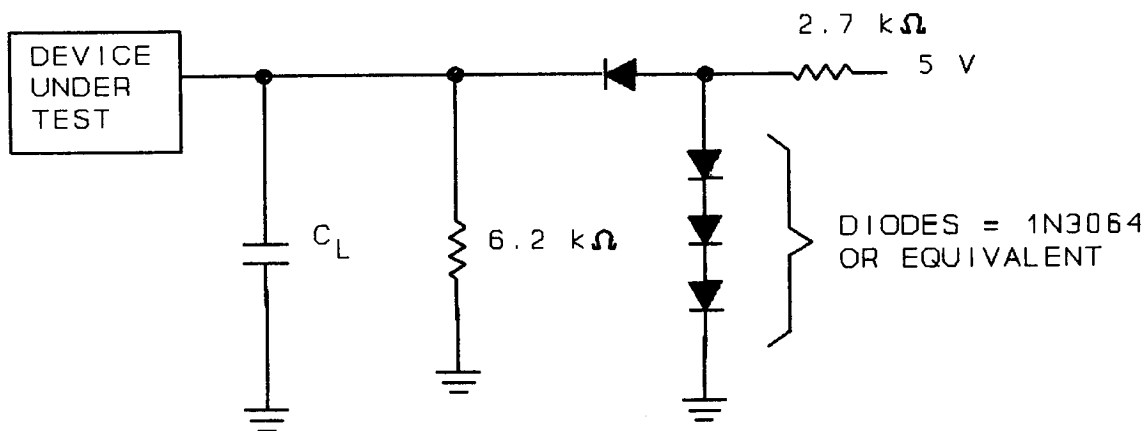
NOTES:

1. V_H = HIGH voltage +12.0 ±0.5 V.
2. X = either V_{IH} or V_{IL}.
3. A₁ - A₈ = A₁₀ - A₁₈ = V_{IL}.
4. V_{pp} = see 4.6.

FIGURE 2. Truth table.

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$C_L = 100\text{ pF}$ INCLUDING JIG CAPACITANCE

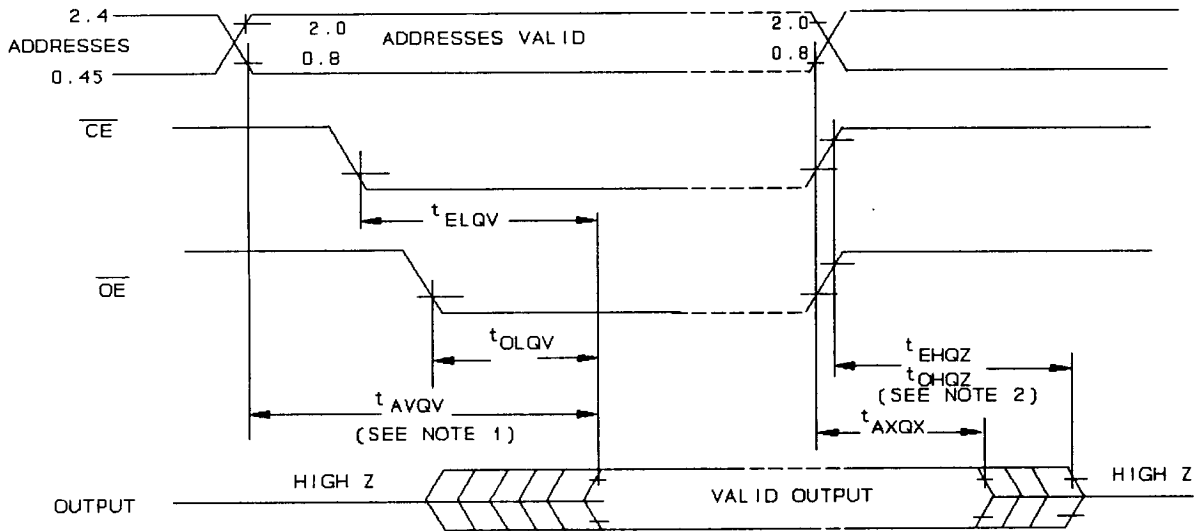
Note:

1. Alternate equivalent switching time test circuit may be used.

FIGURE 3. Switching time test circuit.

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NOTES:

1. \overline{OE} may be delayed up to $t_{ELQV} - t_{OLQV}$ after the falling edge of \overline{CE} without impact on t_{ELQV} .
2. t_{EHQZ} or t_{OHQZ} is specified from \overline{OE} or \overline{CE} , whichever occurs first.
3. Timing measurements are made at 2.0 V for a Logic "1" and 0.8 V for a Logic "0".

FIGURE 4. Read cycle waveforms.

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3.7 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.10 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.12 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendors reliability monitors, this reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 20 program/erase cycles on 25 devices with the following conditions:

- (1) All devices selected for testing shall be programmed per 3.2.3.1 herein (see 4.6).
- (2) Verify pattern (see 3.5.4).
- (3) Erase (see 3.5.4).
- (4) Verify pattern erasure (see 3.5.4).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

- a. Delete the sequence specified as 3.1.9 - 3.1.13 (preburn-in electrical parameters through interim postburn-in electrical parameters of method 5004) and substitute lines 1 through 6 of table IIA herein.
- b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot (see 4.2.3 herein).

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c. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to $V_{CC} \pm 0.5$ V. $R1 = 220$ ohms to 47 kohms. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) $V_{CC} = 4.5$ V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1c herein).

d. Interim and final electrical test parameters shall be as specified in table IIA herein.

e. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

f. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test.

Method A. (Steps 1 through 4 may be performed at wafer level.)

- (1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.5.4).
- (2) Unbiased bake for 24 hours at +175°C.
- (3) Test at $T_C = +25^\circ\text{C}$ (minimum), including a margin test at $V_m = +6$ V and loose timing (i.e., $t_{AVQV} = 1 \mu\text{s}$).
- (4) Erase.
- (5) Program at +25°C with checkerboard pattern (see 3.5.4).
- (6) Test at $T_C = +25^\circ\text{C}$ (minimum), including a margin test at $V_m = +6$ V and loose timing (i.e., $t_{AVQV} = 1 \mu\text{s}$).
- (7) Burn-in (see 4.2.1c).
- (8) Test at $T_C = +25^\circ\text{C}$ (minimum), including a margin test at $V_m = +6$ V and loose timing (i.e., $t_{AVQV} = 1 \mu\text{s}$).
- (9) Test at $T_C = +125^\circ\text{C}$ (minimum), including a margin test at $V_m = +6$ V and loose timing (i.e., $t_{AVQV} = 1 \mu\text{s}$).
- (10) Test at $T_C = -55^\circ\text{C}$ (minimum), including a margin test at $V_m = +6$ V and loose timing (i.e., $t_{AVQV} = 1 \mu\text{s}$).
- (11) Erase (see 3.5.3). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
- (12) Verify erasure at +25°C (see 3.5.4).

Method B. I. Wafer margin test method:

- (1) Program at +25° C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.5.4).
- (2) Measure V_{CC} maximum and store die signature row.
- (3) Unbiased bake for two hours (minimum) at 250° C.
- (4) Test at 25° C. Measure V_{CC} maximum and compare to V_{CC} maximum stored in die. Any die with a delta greater than 0.66 V constitutes a failure and that die is removed from the lot.
- (5) Erase (see 3.5.3). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
- (6) Verify erasure at +25°C (see 3.5.4).

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II. Back end margin test method:

- (1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.5.4).
- (2) Unbiased bake for 72 hours at +165°C.
- (3) Test at $T_C = +25^\circ\text{C}$ (minimum), including a margin test at $V_m = +6\text{ V}$ and loose timing (i.e., $t_{AVQV} = 1\ \mu\text{s}$).
- (4) Erase.
- (5) Program at +25°C with checkerboard pattern or equivalent (see 3.5.4).
- (6) Test at $T_C = +25^\circ\text{C}$ (minimum).
- (7) Burn-in (see 4.2.1c).
- (8) Test at $T_C = +25^\circ\text{C}$ and perform PDA calculation (see 4.2.3).
- (9) Test at $T_C = +125^\circ\text{C}$ (minimum).
- (10) Test at $T_C = -55^\circ\text{C}$ (minimum).
- (11) Erase (see 3.5.3). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
- (12) Verify erasure at +25°C (see 3.5.4).

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

- a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.
- b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.
- c. Static burn-in I and II failures shall be cumulative for determining PDA.
- d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.
- e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7*,Δ 8/		1*,7*,Δ 8/
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7*,Δ 8/		1*,7*,Δ 8/
6	Final electrical parameters	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11
7	Group A test requirements	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11
8	Group B end-point electrical parameters			1,2,3,7,8A,8B,9,10,11,Δ		
9	Group C end-point electrical parameters	2,3,7,8A,8B or 2,8A,10	1,2,3,7,8A,8B,Δ		1,2,3,7,8A,8B,Δ	1,2,3,7,8A,8B,9,10,11,Δ
10	Group D end-point electrical parameters	2,3,8A,8B or 2,8A,10	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

- 1/ Blank spaces indicates tests are not applicable.
- 2/ Any or all subgroups may be combined when using high-speed tests.
- 3/ Subgroups 7 and 8 functional tests shall verify the truth table.
- 4/ * indicates PDA applies to subgroup 1 and 7.
- 5/ ** see 4.4.1e.
- 6/ Δ indicates delta limit (see table IIC) shall be required when specified, and the delta values shall be computed with reference to the previous interim electrical parameters (lines 1 and 3).
- 7/ See 4.4.1d.
- 8/ The device manufacturer may at this option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

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TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

TABLE IIC. Delta Limits at +25°C.

Test ^{1/}	Device types ALL
I _{CC3} standby	±10% of specified value in table I
I _{LI}	±10% of specified value in table I
I _{LO}	±10% of specified value in table I

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.3.1.1 Qualification extension for device class B or S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q or V. Qualification inspection for device classes Q or V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B or S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, or S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q or V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein, except where option 2 of MIL-I-38535 permits in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. O/V (latch-up over-voltage) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-EC for class M devices. For classes B and S, the procedures and circuits shall be submitted to the qualifying activity. For classes Q or V, the procedures and circuits shall be submitted to DESC-EC and will be under the control of the device manufacturer's TRB. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. JEDEC Standard No. 17 may be used as a guideline when performing O/V testing.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except device submitted for groups B, C, and D testing).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

- a. For device class S steady-state life tests shall be conducted using test condition D and the circuit described in 4.2.1c herein, or equivalent as approved by the qualifying activity.
- b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.
- c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted to groups C and D).

4.4.3 Group C inspection. End-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC.

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4.4.3.1 Additional criteria for device classes M and B.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

- (1) The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).
- (2) Test condition D or E. For device class M the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- (3) $T_A = +125^\circ\text{C}$, minimum.
- (4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternative shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005. After completion of all testing, the devices shall be erased and verified.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.6 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be a minimum of 15 Ws/cm^2 . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a $12000 \mu\text{W/cm}^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at $12000 \mu\text{W/cm}^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC. The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

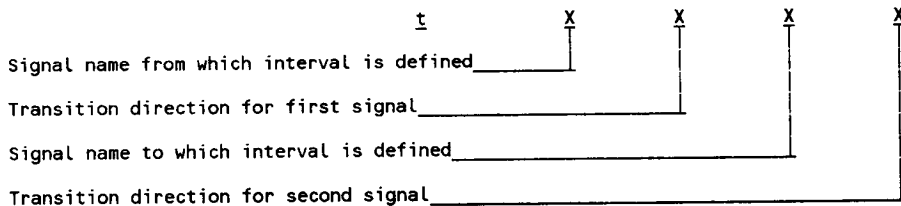
6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

- C_{IN} C_{OUT} Input and bidirectional output, terminal-to-GND capacitance.
- GND Ground zero voltage potential.
- I_{CC} Supply current.
- I_{LI} Input load current.
- T_C Case temperature.
- T_A Ambient temperature.
- V_{CC} Positive supply voltage.
- O/V Latch-up over-voltage.
- O/I Latch-up over-current.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document Listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-EC.

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