MOTOROLA
Semiconductor Products Sector

Order Number: MPC7410PCPNS/D
Rev. 0, 10/2000

Motorola Part Numbers Affected:
XPC7410RX400PC
XPC7410RX450PC
XPC7410RX500PC
XPC7410RX550PC
XPC7410RX600PC

PowerPC™

MPC7410 Part Number Specification for the RX*xxx*PC Series

This document describes part number specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (order #: MPC7410EC/D).

Specifications provided in this Part Number Specification supersede those in the *MPC7410 Hardware Specifications* Rev 0.3 (dated 3/2001) for these part numbers only; specifications not addressed herein are unchanged. This document is frequently updated. Therefore, contact your Motorola sales office for the latest version.

Part numbers addressed in this document are listed in Table 1. For more detailed ordering information see Table 1.

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Table 1. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T_J (°C)	
XPC7410RX400PC	400 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency
XPC7410RX450PC	450 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
XPC7410RX500PC	500 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency
XPC7410RX550PC	550 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 550Mhz frequency
XPC7410RX600PC	600 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 600Mhz frequency

Note: The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

Note: Grayed-out 600Mhz data are extrapolated values.

Errata

This section summarizes design defects or errors (errata) that are known to exist for these parts. There may be additional errata that are not known or are not yet documented here which may cause the part to deviate from the functional description provided in the MPC7410 RISC Microprocessor User’s Manual (order # MPC7410UM/AD Rev 0). The MPC7410 RISC Microprocessor User’s Manual will be available in 4Q00. Contact your local Motorola sales office for later and/or more detailed description of the errata.

The known errata as of the date of this document are summarized below

Table 2. Errata

#	Problem	Description	Impact	Work-Around
1	Cache inhibited instruction fetches that hit in L2 Direct Mapped SRAM space may cause processor hang	Cache inhibited instruction fetches that hit in L2 Direct Mapped SRAM space when the instruction buffers are full may cause processor to not make forward progress	Systems using L2 Direct Mapped SRAM and mapping part of this space as Cache Inhibited	1. Set L2RDIS (bit 13) of MSSCR1, or 2. Do not map instructions in the L2 Direct Mapped memory space as cache inhibited.
2	Incorrect condition code on mismatched LWARX/STWCX pair	A STWCX instruction may be performed without setting the condition code if the store hits in the L2 and the LWARX instruction that set the reservation is to another coherency granule.	Any code which uses mismatched LWARX/STWCX address pairs	1. Avoid mismatched LWARX/STWCX address pairs, or 2. Turn off the L2
3	TLBSYNC may hang in the presence of a DST	The MPC7400 may not make forward progress if a DST has caused an MMU tablewalk, that MMU tablewalk was marked by a TLBIE instruction, and a TLBSYNC instruction is pipelined the cycle after the MMU tablewal accesses the dL1 cache.	Any system which has an active DST engine while executing a TLBSYNC instruction in a privileged context	Insert a DSSALL instruction before a TLBSYNC instruction
4	Queueing six transactions to secondary bus may hang the system	Queueing six transactions from a single MAX processor could use all Data Transaction Queue resources and hang the system if forward progress cannot be made by allowing MAX to complete at least one outstanding transaction.	Any system which allows 6 outstanding transactions from a single processor and which has a secondary bus with characteristics as detailed in full description.	1. Limit the number of outstanding transactions from a secondary bus to 5 in system logic, or 2. Mark the memory space on the secondary bus as guarded and avoid DST(ST)(T) and LMW instructions.
5	Consecutive interrupts may be non-recoverable	Consecutive Performance Monitor, Decrementer, or Thermal Management Interrupts may become non-recoverable.	Any system which enables a combination of Performance Monitor, Decrementer, or Thermal Management Interrupts at the same time.	Avoid enabling any combination of Performance Monitor, Decrementer, or Thermal Management Interrupts at the same time.
6	Disabling L2 cache may hang processor	The MPC7410 may hang if the L2 cache is disabled during an outstanding instruction fetch.	Any system which executes code to disable the L2 cache.	1. Mark the code that disables the L2 cache as Cache Inhibited, or 2. Preload the code that disables the L2 cache into the instruction cache before execution.

General

There are no changes to the features of the MPC7410 described in the MPC7410 Hardware Specifications (MPC7410EC/D).

1.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0V±50mV	V
PLL supply voltage		AVdd	2.0V±50mV	V
L2 DLL supply voltage		L2AVdd	2.0V±50mV	V
Processor bus supply voltage	BVSEL = $\overline{\text{HRESET}}$	OVdd	2.5V±125mV	V
	BVSEL = GND	OVdd	1.8V±90mV	V
L2 bus supply voltage	L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.5V±125mV	V
	L2VSEL = GND	L2OVdd	1.8V±90mV	V
Input voltage	Processor bus	V_{in}	GND to OVdd	V
	L2 Bus	V_{in}	GND to L2OVdd	V
	JTAG Signals	V_{in}	GND to OVdd	V
Die-junction temperature		T_j	0-65	°C
Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.				

Table 7 provides the power consumption for the MPC7410 part at the frequencies described herein.

Table 4. Power Consumption for MPC7410

	Processor (CPU) Frequency	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz	600Mhz		
Full-On Mode					
Typical	6	7	8	W	1, 3,
Maximum	12	14	16	W	1, 2, 4
Doze Mode					
Maximum	4	5	6	W	1, 2
Nap Mode					
Maximum	2.0	2.25	2.5	W	1, 2
Sleep Mode					
Maximum	2.0	2.25	2.5	W	1, 2

Table 4. Power Consumption for MPC7410 (Continued)

	Processor (CPU) Frequency	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz	600Mhz		
Sleep Mode—PLL and DLL Disabled					
Typical	0.5	0.5	0.5	W	1, 3
Maximum	2.0	2.0	2.0	W	1, 2

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at Vdd = 2.2V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.15V, OVdd = L2OVdd = 2.5V in a system while running a codec application that is AltiVec intensive.
4. These values include the use of Altivec. Without Altivec operation, estimate a 25% decrease.

1.4.2.1 Clock AC Specifications

Table 8 provides the additional clock AC timing specifications described in this Part Number Specification. Refer to the MPC7410 Hardware Specification for the remaining frequencies.

Table 5. Clock AC Timing Specifications

At recommended operating conditions (See Table 3.)

Characteristic	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		600 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	300	400	300	450	300	500	300	550	300	600	MHz	
VCO frequency	f_{VCO}	600	800	600	900	600	1000	600	1100	600	1200	MHz	
SYSCLK frequency	f_{SYSCLK}	33	100	33	100	33	100	33	100	33	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	7.5	30	7.5	30	ns	
SYSCLK rise and fall time	t_{KR} & t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns	2
		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OVdd/2	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	40	60	%	4
SYSCLK jitter		—	±150	—	±150	—	±150	—	±150	—	±150	ps	5
Internal PLL relock time		—	100	—	100	—	100	—	100	—	100	µs	6
Notes:See General hardware specification.													

1.4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7410 part described in this Part Number Specification.

Table 1. Processor Bus AC Timing Specifications[1]

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 100MHz

Parameter	Symbol	400, 450, 500, 550, 600 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	2,3,4,5
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	t_{AVKH}	1.4	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSVKH}	1.4	—		—
Data/Data Parity	t_{DVKH}	1.4	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARVKH}	1.4	—		—
All Other Inputs	t_{IVKH}	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	t_{AXKH}	0	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSXKH}	0	—		—
Data/Data Parity	t_{DXKH}	0	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARXKH}	0	—		—
All Other Inputs	t_{IXKH}	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	t_{KHAV}	—	3.0		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSV}	—	3.0		—
Data	t_{KHDV}	—	3.5		7
Data Parity	t_{KHDPV}	—	3.5		7
ARTRY/SHD0/SHD1	t_{KHARV}	—	2.3		—
All Other Outputs	t_{KHOV}	—	3.0		9
Output Hold Times:				ns	13
Address/Transfer Attribute	t_{KHAX}	0.75	—		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSX}	0.75	—		—
Data/Data Parity	t_{KHDX}	0.6	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{KHARX}	0.75	—		—
All Other Outputs	t_{KHOX}	0.75	—		9
SYSCLK to Output Enable	t_{KHOE}	0.5	—	ns	14
SYSCLK to Output High Impedance (all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$/AMON(0), $\overline{\text{ARTRY}}$/$\overline{\text{SHD}}$, $\overline{\text{DBB}}$/DMON(0))	t_{KHOZ}	—	3.5	ns	15

Table 1. Processor Bus AC Timing Specifications[1] (Continued)

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 100MHz

Parameter	Symbol	400, 450, 500, 550, 600 Mhz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{TS}$, $\overline{ABB/AMON(0)}$, $\overline{DBB/DMON(0)}$ High Impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	4,15, 16,17
Maximum Delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ Precharge	t_{KHARP}	—	1	t_{sysclk}	4,17
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ High Impedance After Precharge	t_{KHARPZ}	—	2	t_{sysclk}	4,17

Notes:
See General hardware specification.

1.4.2.3 L2 Clock AC Specifications

Table 1 provides the L2CLK Output AC Timing Specifications for the MPC7410 part described in this Part Number Specification

Table 1. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3.)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		600 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	150	200	150	225	150	250	150	275	150	300	MHz	1
L2CLK cycle time	t_{L2CLK}	5	6.67	4.4	6.67	4	6.67	3.6	6.67	3.3	6.67	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	640	—	640	—	L2CLK	4
DLL capture window			±200		±200		±200		±200		±200	ns	5
Notes: See General hardware specification.													

1.4.2.4 L2 Bus AC Specifications

Table 1 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this Part Number Specification.

Table 1. L2 Bus Interface AC Timing Specifications

At Vdd=AVdd=L2AVdd= 2.05V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 2.5V±0.125V and L2OVdd =1.8V±0.090V

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		600 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} & t_{L2CF}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns	1
Setup Times: Data and parity	t_{DVL2CH}	1.5	—	1.375	—	1.250	—	1.125	—	1.0	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOV}	- - - -	2.5 TBD TBD TBD	- - - -	2.375 TBD TBD TBD	- - - -	2.25 TBD TBD TBD	- - - -	2.05 TBD TBD TBD	- - - -	2.0 TBD TBD TBD	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOX}	0.6 TBD TBD TBD	- - - -	0.55 TBD TBD TBD	- - - -	0.5 TBD TBD TBD	- - - -	0.45 TBD TBD TBD	- - - -	0.4 TBD TBD TBD	- - - -	ns	3
L2SYNC_IN to high impedance All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOZ}	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	ns	
Notes: See General Hardware Specification													

1.10 Ordering Information

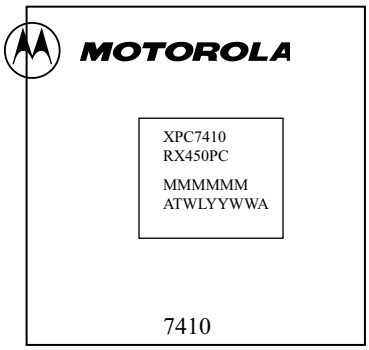
Table 1 provides the ordering information for the MPC7410 part described in this Part Number Specification.

Table 1. Ordering Information for the MPC7410 Microprocessor

Package Type	Device Rev	Process	Mask Code	CPU Frequency (MHz)	Motorola Part Number
360 CBGA	1.2	HIP 6	82K65D	400MHz	XPC7410RX400PC
				450MHz	XPC7410RX450PC
				500MHz	XPC7410RX500PC
				550MHz	XPC7410RX550PC
				600MHz	XPC7410RX600PC

1.10.1 Part Marking

Parts are marked as the example shown in Figure 1.Figure 1.



BGA

Notes:

MMMMMM is the 6-digit mask number

ATWLYYWWA is the traceability code

CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure 1. Motorola Part Marking for BGA Device

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