

# 19 Output Differential Buffer for PCIe Gen2 and QPI

9DB1904B

## Description

The **9DB1904** is electrically compatible to the Intel DB1900GS Differential Buffer Specification. This buffer provides 19 output clocks for PCI-Express Gen2 or Intel QPI 6.4GT/s applications. A differential clock from a CK410B+ main clock generator, such as the ICS932S421 drives the **9DB1904**. The **9DB1904** can provide outputs up to 400MHz in Bypass Mode.

## Recommended Application

19 Output Differential Buffer for PCIe Gen2 and QPI

## Key Specifications

- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 150ps across all outputs

## Features/Benefits

- Power up default is all outputs in 1:1 mode/No SMBus programming
- Spread spectrum compatible/EMI reductions
- Supports output frequencies up to 400 MHz in bypass mode/flexible fanout buffer
- 8 Selectable SMBus addresses/no SMBus segmentation required
- SMBus address determines PLL or Bypass mode/pin savings
- Dedicated VDDA and CKPWRGD\_PD# pins/easy board design

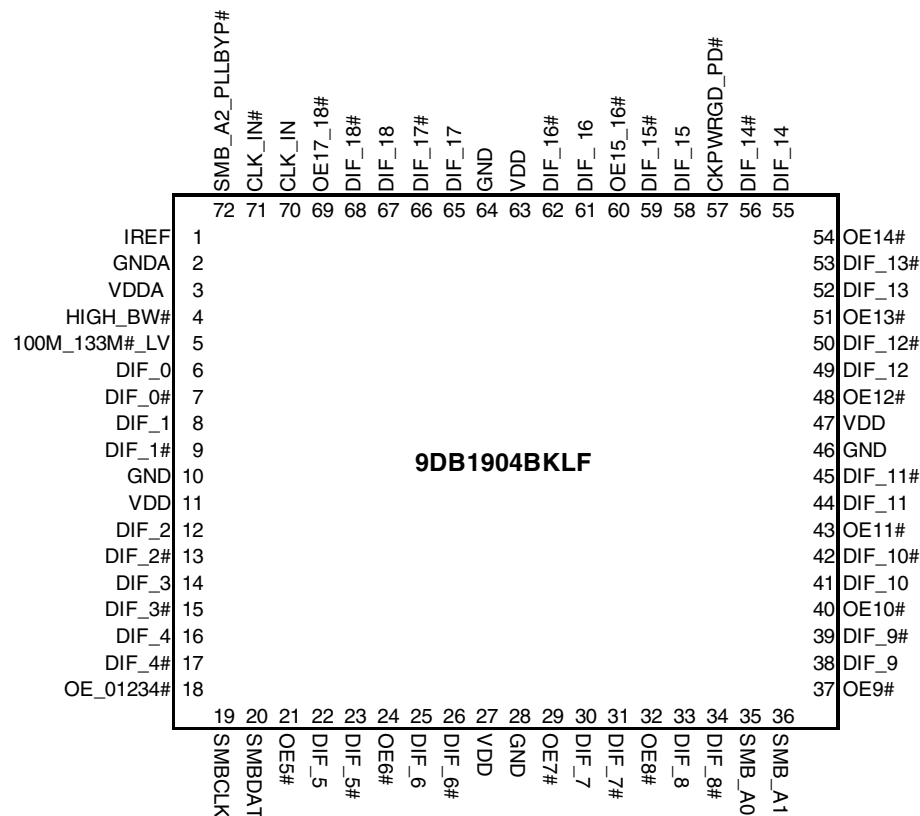
## Functionality at Power Up (PLL Mode)

| 100M_133M# | CLK_IN MHz | DIF_(18:0) MHz |
|------------|------------|----------------|
| 1          | 100MHz     | CLK_IN         |
| 0          | 133MHz     | CLK_IN         |

## Power Down Functionality

| INPUTS      |                | OUTPUTS  | PLL State |
|-------------|----------------|----------|-----------|
| CKPWRGD_PD# | CLK_IN/CLK IN# | DIF/DIF# |           |
| 1           | Running        | Running  | ON        |
| 0           | X              | Hi-Z     | OFF       |

## Pin Configuration



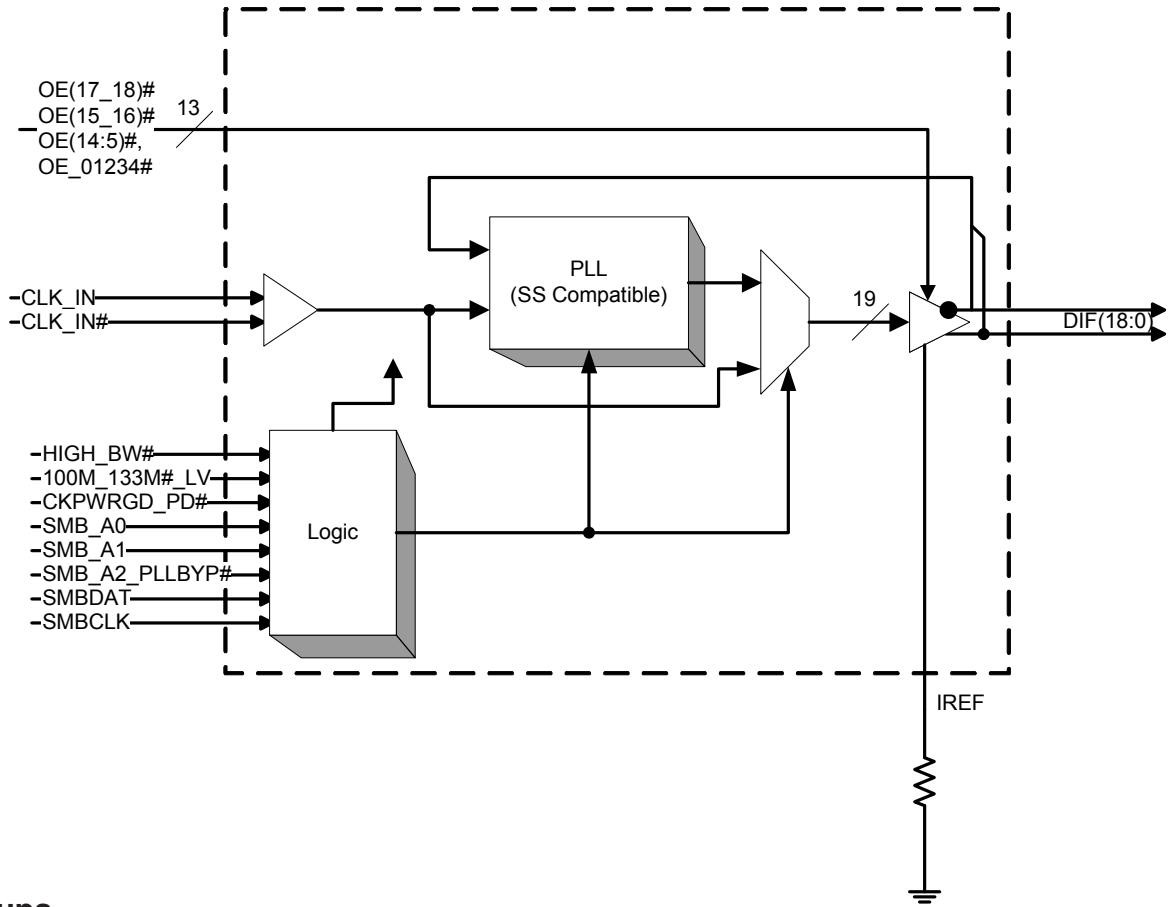
## Pin Description

| PIN # | PIN NAME      | PIN TYPE | DESCRIPTION   |
|-------|---------------|----------|---|
| 1     | IREF          | OUT      | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 2     | GNDA          | PWR      | Ground pin for the PLL core.  |
| 3     | VDDA          | PWR      | 3.3V power for the PLL core.  |
| 4     | HIGH_BW#      | IN       | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low   |
| 5     | 100M_133M#_LV | IN       | Low Threshold Input to select operating frequency.<br>See Functionality Table for Definition  |
| 6     | DIF_0         | OUT      | 0.7V differential true clock output   |
| 7     | DIF_0#        | OUT      | 0.7V differential Complementary clock output  |
| 8     | DIF_1         | OUT      | 0.7V differential true clock output   |
| 9     | DIF_1#        | OUT      | 0.7V differential Complementary clock output  |
| 10    | GND           | PWR      | Ground pin.   |
| 11    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 12    | DIF_2         | OUT      | 0.7V differential true clock output   |
| 13    | DIF_2#        | OUT      | 0.7V differential Complementary clock output  |
| 14    | DIF_3         | OUT      | 0.7V differential true clock output   |
| 15    | DIF_3#        | OUT      | 0.7V differential Complementary clock output  |
| 16    | DIF_4         | OUT      | 0.7V differential true clock output   |
| 17    | DIF_4#        | OUT      | 0.7V differential Complementary clock output  |
| 18    | OE_01234#     | IN       | Active low input for enabling DIF pairs 0, 1, 2, 3 and 4.<br>1 =disable outputs, 0 = enable outputs   |
| 19    | SMBCLK        | IN       | Clock pin of SMBUS circuitry, 5V tolerant   |
| 20    | SMBDAT        | I/O      | Data pin of SMBUS circuitry, 5V tolerant  |
| 21    | OE5#          | IN       | Active low input for enabling DIF pair 5.<br>1 =disable outputs, 0 = enable outputs   |
| 22    | DIF_5         | OUT      | 0.7V differential true clock output   |
| 23    | DIF_5#        | OUT      | 0.7V differential Complementary clock output  |
| 24    | OE6#          | IN       | Active low input for enabling DIF pair 6.<br>1 =disable outputs, 0 = enable outputs   |
| 25    | DIF_6         | OUT      | 0.7V differential true clock output   |
| 26    | DIF_6#        | OUT      | 0.7V differential Complementary clock output  |
| 27    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 28    | GND           | PWR      | Ground pin.   |
| 29    | OE7#          | IN       | Active low input for enabling DIF pair 7.<br>1 =disable outputs, 0 = enable outputs   |
| 30    | DIF_7         | OUT      | 0.7V differential true clock output   |
| 31    | DIF_7#        | OUT      | 0.7V differential Complementary clock output  |
| 32    | OE8#          | IN       | Active low input for enabling DIF pair 8.<br>1 =disable outputs, 0 = enable outputs   |
| 33    | DIF_8         | OUT      | 0.7V differential true clock output   |
| 34    | DIF_8#        | OUT      | 0.7V differential Complementary clock output  |
| 35    | SMB_A0        | IN       | SMBus address bit 0 (LSB)   |
| 36    | SMB_A1        | IN       | SMBus address bit 1   |

## Pin Description (continued)

| PIN # | PIN NAME       | PIN TYPE | DESCRIPTION   |
|-------|----------------|----------|---|
| 37    | OE9#           | IN       | Active low input for enabling DIF pair 9.<br>1 =disable outputs, 0 = enable outputs   |
| 38    | DIF_9          | OUT      | 0.7V differential true clock output   |
| 39    | DIF_9#         | OUT      | 0.7V differential Complementary clock output  |
| 40    | OE10#          | IN       | Active low input for enabling DIF pair 10.<br>1 =disable outputs, 0 = enable outputs  |
| 41    | DIF_10         | OUT      | 0.7V differential true clock output   |
| 42    | DIF_10#        | OUT      | 0.7V differential Complementary clock output  |
| 43    | OE11#          | IN       | Active low input for enabling DIF pair 11.<br>1 =disable outputs, 0 = enable outputs  |
| 44    | DIF_11         | OUT      | 0.7V differential true clock output   |
| 45    | DIF_11#        | OUT      | 0.7V differential Complementary clock output  |
| 46    | GND            | PWR      | Ground pin.   |
| 47    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 48    | OE12#          | IN       | Active low input for enabling DIF pair 12.<br>1 =disable outputs, 0 = enable outputs  |
| 49    | DIF_12         | OUT      | 0.7V differential true clock output   |
| 50    | DIF_12#        | OUT      | 0.7V differential Complementary clock output  |
| 51    | OE13#          | IN       | Active low input for enabling DIF pair 13.<br>1 =disable outputs, 0 = enable outputs  |
| 52    | DIF_13         | OUT      | 0.7V differential true clock output   |
| 53    | DIF_13#        | OUT      | 0.7V differential Complementary clock output  |
| 54    | OE14#          | IN       | Active low input for enabling DIF pair 14.<br>1 =disable outputs, 0 = enable outputs  |
| 55    | DIF_14         | OUT      | 0.7V differential true clock output   |
| 56    | DIF_14#        | OUT      | 0.7V differential Complementary clock output  |
| 57    | CKPWRGD_PD#    | IN       | 3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.   |
| 58    | DIF_15         | OUT      | 0.7V differential true clock output   |
| 59    | DIF_15#        | OUT      | 0.7V differential Complementary clock output  |
| 60    | OE15_16#       | IN       | Active low input for enabling DIF pairs 15 and 16.<br>1 =disable outputs, 0 = enable outputs  |
| 61    | DIF_16         | OUT      | 0.7V differential true clock output   |
| 62    | DIF_16#        | OUT      | 0.7V differential Complementary clock output  |
| 63    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 64    | GND            | PWR      | Ground pin.   |
| 65    | DIF_17         | OUT      | 0.7V differential true clock output   |
| 66    | DIF_17#        | OUT      | 0.7V differential Complementary clock output  |
| 67    | DIF_18         | OUT      | 0.7V differential true clock output   |
| 68    | DIF_18#        | OUT      | 0.7V differential Complementary clock output  |
| 69    | OE17_18#       | IN       | Active low input for enabling DIF pairs 17 and 18.<br>1 =disable outputs, 0 = enable outputs  |
| 70    | CLK_IN         | IN       | True Input for differential reference clock.  |
| 71    | CLK_IN#        | IN       | Complementary Input for differential reference clock.   |
| 72    | SMB_A2_PLLBYP# | IN       | SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating.<br>0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used) |

### Functional Block Diagram



### Power Groups

| Pin Number  |             | Description |
|-------------|-------------|-------------|
| VDD         | GND         |             |
| 3           | 2           | PLL, Analog |
| 11,27,47,63 | 10,28,46,64 | DIF clocks  |

### 9DB1904 Frequency Selects for PLL Mode

| Byte 9, bit 2<br>100M_133M#_LV | Byte9, bit 1<br>FSB | Byte 9, bit 0<br>FSA | CLK_IN MHz | DIF Outputs MHz | Notes |
|--------------------------------|---------------------|----------------------|------------|-----------------|-------|
| 1                              | 0                   | 1                    | 100.00     | 100.00          | 1     |
| 0                              | 0                   | 1                    | 133.33     | 133.33          | 2     |

#### Notes:FS\_A\_410 = 1

1. Powerup Default for 100M\_133M# = 1
2. Powerup Default for 100M\_133M# = 0

**Electrical Characteristics - Absolute Maximum Ratings**

| PARAMETER                 | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage  | VDDA               |                            |         |     | 4.6                   | V     | 1,2   |
| 3.3V Logic Supply Voltage | VDD                |                            |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage         | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage        | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage        | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature       | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature      | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

**Electrical Characteristics - Clock Input Parameters**

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER                          | SYMBOL             | CONDITIONS  | MIN                   | TYP | MAX  | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN        | V <sub>IHDIF</sub> | Differential inputs<br>(single-ended measurement)         | 600                   | 800 | 1150 | mV    | 1     |
| Input Low Voltage - DIF_IN         | V <sub>ILDIF</sub> | Differential inputs<br>(single-ended measurement)         | V <sub>SS</sub> - 300 | 0   | 300  | mV    | 1     |
| Input Common Mode Voltage - DIF_IN | V <sub>COM</sub>   | Common Mode Input Voltage                                 | 300                   |     | 1000 | mV    | 1     |
| Input Amplitude - DIF_IN           | V <sub>SWING</sub> | Peak to Peak value  | 300                   |     | 1450 | mV    | 1     |
| Input Slew Rate - DIF_IN           | dv/dt              | Measured differentially                                   | 0.4                   |     | 8    | V/ns  | 1,2   |
| Input Leakage Current              | I <sub>IN</sub>    | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND | -5                    |     | 5    | uA    | 1     |
| Input Duty Cycle                   | d <sub>tin</sub>   | Measurement from differential waveform                    | 45                    |     | 55   | %     | 1, 3  |
| Input Jitter - Cycle to Cycle      | J <sub>DIFIN</sub> | Differential Measurement                                  | 0                     |     | 125  | ps    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through +/-75mV window centered around differential zero

<sup>3</sup>Input duty cycle will directly impact output duty cycle in bypass mode. It has no impact in PLL mode.

**Electrical Characteristics - Current Consumption**

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER                | SYMBOL                | CONDITIONS                       | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|----------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I <sub>DD3.3OP</sub>  | VDD, All outputs active @100MHz  |     | 425 | 450 | mA    | 1     |
|                          | I <sub>DD3.3AOP</sub> | VDDA, All outputs active @100MHz |     | 35  | 45  | mA    | 1     |
| Powerdown Current        | I <sub>DD3.3PD</sub>  | VDD                              |     | 20  | 25  | mA    | 1     |
|                          | I <sub>DD3.3APD</sub> | VDDA                             |     | 12  | 15  | mA    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. Zo = 100Ω

**Electrical Characteristics - Input/Supply/Common Parameters**TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER                        | SYMBOL                | CONDITIONS  | MIN                   | TYP    | MAX                   | UNITS  | NOTES |
|----------------------------------|-----------------------|---|-----------------------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature    | T <sub>COM</sub>      | Commercial range  | 0                     |        | 70                    | °C     | 1     |
| Input High Voltage               | V <sub>IH</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | 2                     |        | V <sub>DD</sub> + 0.3 | V      | 1     |
| Input Low Voltage                | V <sub>IL</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | GND - 0.3             |        | 0.8                   | V      | 1     |
| Low Threshold Input-High Voltage | V <sub>IH_FS</sub>    | 3.3 V +/-5%, Applies to 100M_133M#_LV pin   | 0.7                   |        | V <sub>DD</sub> + 0.3 | V      | 1     |
| Low Threshold Input-Low Voltage  | V <sub>IL_FS</sub>    | 3.3 V +/-5%, Applies to 100M_133M#_LV pin   | V <sub>SS</sub> - 0.3 |        | 0.35                  | V      | 1     |
| Input Current                    | I <sub>IN</sub>       | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5                    |        | 5                     | uA     | 1     |
|                                  | I <sub>INP</sub>      | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200                  |        | 200                   | uA     | 1     |
| Input Frequency                  | F <sub>ibyp</sub>     | V <sub>DD</sub> = 3.3 V, Bypass mode  | 33                    |        | 400                   | MHz    | 2     |
|                                  | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 100MHz PLL mode  | 90                    | 100.00 | 110                   | MHz    | 2     |
|                                  | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 133.33MHz PLL mode   | 120                   | 133.33 | 147                   | MHz    | 2     |
| Pin Inductance                   | L <sub>pin</sub>      |   |                       |        | 7                     | nH     | 1     |
| Capacitance                      | C <sub>IN</sub>       | Logic Inputs, except DIF_IN   | 1.5                   |        | 5                     | pF     | 1     |
|                                  | C <sub>INDIF_IN</sub> | DIF_IN differential clock inputs  | 1.5                   |        | 2.7                   | pF     | 1,4   |
|                                  | C <sub>OUT</sub>      | Output pin capacitance  |                       |        | 6                     | pF     | 1     |
| Clk Stabilization                | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |                       |        | 1.8                   | ms     | 1,2   |
| Input SS Modulation Frequency    | f <sub>MODIN</sub>    | Allowable Frequency (Triangular Modulation)   | 30                    |        | 33                    | kHz    | 1     |
| OE# Latency                      | t <sub>LATOE#</sub>   | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 4                     |        | 12                    | clocks | 1,3   |
| Tdrive_PD#                       | t <sub>DRVPD</sub>    | DIF output enable after PD# de-assertion  |                       |        | 300                   | us     | 1,3   |
| Tfall                            | t <sub>F</sub>        | Fall time of control inputs   |                       |        | 5                     | ns     | 1,2   |
| Trise                            | t <sub>R</sub>        | Rise time of control inputs   |                       |        | 5                     | ns     | 1,2   |
| SMBus Input Low Voltage          | V <sub>ILSMB</sub>    |   |                       |        | 0.8                   | V      | 1     |
| SMBus Input High Voltage         | V <sub>IHSMB</sub>    |   | 2.1                   |        | V <sub>DD</sub> SMB   | V      | 1     |
| SMBus Output Low Voltage         | V <sub>OLSMB</sub>    | @ I <sub>PULLUP</sub>   |                       |        | 0.4                   | V      | 1     |
| SMBus Sink Current               | I <sub>PULLUP</sub>   | @ V <sub>OL</sub>   | 4                     |        |                       | mA     | 1     |
| Nominal Bus Voltage              | V <sub>DD</sub> SMB   | 3V to 5V +/- 10%  | 2.7                   |        | 5.5                   | V      | 1     |
| SCLK/SDATA Rise Time             | t <sub>RSMB</sub>     | (Max VIL - 0.15) to (Min VIH + 0.15)  |                       |        | 1000                  | ns     | 1     |
| SCLK/SDATA Fall Time             | t <sub>FSMB</sub>     | (Min VIH + 0.15) to (Max VIL - 0.15)  |                       |        | 300                   | ns     | 1     |
| SMBus Operating Frequency        | f <sub>MAXSMB</sub>   | Maximum SMBus operating frequency   |                       |        | 100                   | kHz    | 1,5   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.<sup>3</sup>Time from deassertion until outputs are >200 mV<sup>4</sup>DIF\_IN input<sup>5</sup>The differential input clock must be running for the SMBus to be active

## Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER              | SYMBOL     | CONDITIONS  | MIN  | TYP  | MAX  | UNITS | NOTES   |
|------------------------|------------|---|------|------|------|-------|---------|
| Slew rate              | Trf        | Scope averaging on  | 1    | 2    | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | ΔTrf       | Slew rate matching, Scope averaging on  |      | 12.6 | 20   | %     | 1, 2, 4 |
| Voltage High           | VHigh      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  | 797  | 850  | mV    | 1       |
| Voltage Low            | VLow       |   | -150 | 39   | 150  |       | 1       |
| Max Voltage            | Vmax       | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      | 857  | 1150 | mV    | 1       |
| Min Voltage            | Vmin       |   | -300 | 7    |      |       | 1       |
| Vswing                 | Vswing     | Scope averaging off   | 300  | 1510 |      | mV    | 1, 2    |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off   | 250  | 378  | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | Δ-Vcross   | Scope averaging off   |      | 57   | 140  | mV    | 1, 6    |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. I<sub>REF</sub> = VDD/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA.

I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω (100Ω differential impedance).

<sup>2</sup> Measured from differential waveform

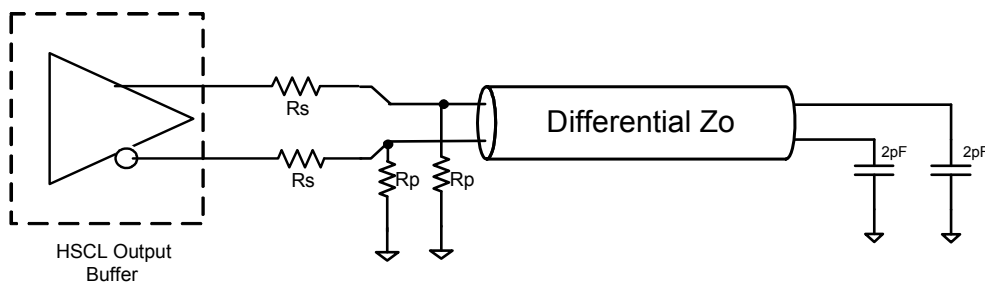
<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of V<sub>cross\_min</sub>/max (V<sub>cross</sub> absolute) allowed. The intent is to limit Vcross induced modulation by setting V<sub>cross\_delta</sub> to be smaller than V<sub>cross</sub> absolute.

### 9DBxxx Differential Test Loads



**Differential Output Termination Table**

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|------------|----------|--------|--------|
| 100        | 475      | 33     | 50     |
| 85         | 412      | 27     | 43.2   |

### Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T<sub>COM</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER              | SYMBOL               | CONDITIONS   | MIN  | TYP               | MAX               | UNITS | NOTES            |
|------------------------|----------------------|--|------|-------------------|-------------------|-------|------------------|
| PLL Bandwidth          | BW                   | -3dB point in High BW Mode   | 2    | 3                 | 4                 | MHz   | 1                |
|                        |                      | -3dB point in Low BW Mode  | 0.7  | 1                 | 1.4               | MHz   | 1                |
| PLL Jitter Peaking     | t <sub>JPEAK</sub>   | Peak Pass band Gain  |      | 1.4               | 2                 | dB    | 1                |
| Duty Cycle             | t <sub>DC</sub>      | Measured differentially, PLL Mode  | 45   | 49.5              | 55                | %     | 1,2              |
| Duty Cycle Distortion  | t <sub>DCD</sub>     | Measured differentially, Bypass Mode<br>@100MHz  | -2   | 1                 | 2                 | %     | 1,2,5            |
| Skew, Input to Output  | t <sub>pdBYP</sub>   | Bypass Mode, nominal value @ 25°C, 3.3V,<br>V <sub>T</sub> = 50%   | 2500 | 3700              | 4500              | ps    | 1,2,4            |
|                        | t <sub>pdPLL</sub>   | PLL Mode, nominal value @ 25°C, 3.3V,<br>V <sub>T</sub> = 50%  | 100  | 300               | 500               | ps    | 1,2,3            |
| DIF_IN, DIF [x:0]      | Δt <sub>pd_BYP</sub> | Input-to-Output Skew Variation in Bypass mode<br>(over specified voltage / temperature operating ranges) |      | 1500 <sup>1</sup> | 1600 <sup>1</sup> | ps    | 1,2,4,6,7,8,9,13 |
| DIF_IN, DIF [x:0]      | Δt <sub>pd_PLL</sub> | Input-to-Output Skew Variation in PLL mode<br>(over specified voltage / temperature operating ranges)    |      | 1250 <sup>1</sup> | 1350 <sup>1</sup> | ps    | 1,2,3,6,7,8,9,13 |
| DIF[X:0]               | t <sub>JPH</sub>     | Differential Phase Jitter (RMS Value)  |      | 2                 | 10                | ps    | 1,7,10           |
| DIF[X:0]               | t <sub>SSERROR</sub> | Differential Spread Spectrum Tracking Error<br>(peak to peak)  |      | 40                | 80                | ps    | 1,7,12           |
| Skew, Output to Output | t <sub>sk3</sub>     | V <sub>T</sub> = 50%   |      | 100               | 150               | ps    | 1                |
| Jitter, Cycle to cycle | t <sub>jyc-cyc</sub> | PLL mode   |      | 40                | 50                | ps    | 1,2              |
|                        |                      | Additive Jitter in Bypass Mode   |      | 25                | 50                | ps    | 1,2              |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. C<sub>LOAD</sub> = 2pF

<sup>2</sup>Measured from differential cross-point to differential cross-point

<sup>3</sup>PLL mode Input-to-Output skew is measured at the first output edge following the corresponding input.

<sup>4</sup>All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

<sup>5</sup>Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>6</sup>V<sub>T</sub> = 50% of V<sub>out</sub>

<sup>7</sup>This parameter is deterministic for a given device

<sup>8</sup>Measured with scope averaging on to find mean value.

<sup>9</sup>Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.

<sup>10</sup>This parameter is measured at the outputs of two separate 9DB1904 devices driven by a single main clock. The 9DB1904's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22MHz and 11-33MHz.

<sup>11</sup>t is the period of the input clock

<sup>12</sup>Differential spread spectrum tracking error is the difference in spread spectrum tracking between two 9DB1904 devices. This parameter is measured at the outputs of two separate 9DB1904 devices driven by a single main clock in Spread Spectrum mode. The 9DB1904's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33KHz modulation frequency, linear profile.

<sup>13</sup>This parameter is an absolute value. It is not a double-sided figure.



**Electrical Characteristics - Phase Jitter Parameters**TA = T<sub>COM</sub>; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER                             | SYMBOL                  | CONDITIONS   | MIN | TYP  | MAX | UNITS    | Notes |
|---------------------------------------|-------------------------|--|-----|------|-----|----------|-------|
| Phase Jitter, PLL Mode                | t <sub>jphPCleG1</sub>  | PCIe Gen 1   |     | 35   | 86  | ps (p-p) | 1,2,3 |
|                                       | t <sub>jphPCleG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |     | 1.2  | 3   | ps (rms) | 1,2   |
|                                       |                         | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |     | 2.5  | 3.1 | ps (rms) | 1,2   |
|                                       | t <sub>jphQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |     | 0.30 | 0.5 | ps (rms) | 1,5   |
| Additive Phase Jitter,<br>Bypass mode | t <sub>jphPCleG1</sub>  | PCIe Gen 1   |     | 3    | 10  | ps (p-p) | 1,2,3 |
|                                       | t <sub>jphPCleG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |     | 0.01 | 0.3 | ps (rms) | 1,2,6 |
|                                       |                         | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |     | 0.8  | 1.3 | ps (rms) | 1,2,6 |
|                                       | t <sub>jphQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |     | 0.12 | 0.3 | ps (rms) | 1,5,6 |

<sup>1</sup> Applies to all outputs.<sup>2</sup> See <http://www.pcisig.com> for complete specs<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.<sup>4</sup> Subject to final radification by PCI SIG.<sup>5</sup> Calculated from Intel-supplied Clock Jitter Tool v 1.6.3<sup>6</sup> For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)<sup>2</sup> = (total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>**Clock Periods - Differential Outputs with Spread Spectrum Disabled**

| SSC OFF | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|         |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|         |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF     | 100.00           | 9.94900                |                             | 9.99900                     | 10.00000             | 10.00100                    |                             | 10.05100               | ns    | 1,2   |
|         | 133.33           | 7.44925                |                             | 7.49925                     | 7.50000              | 7.50075                     |                             | 7.55075                | ns    | 1,2   |

**Clock Periods - Differential Outputs with Spread Spectrum Enabled**

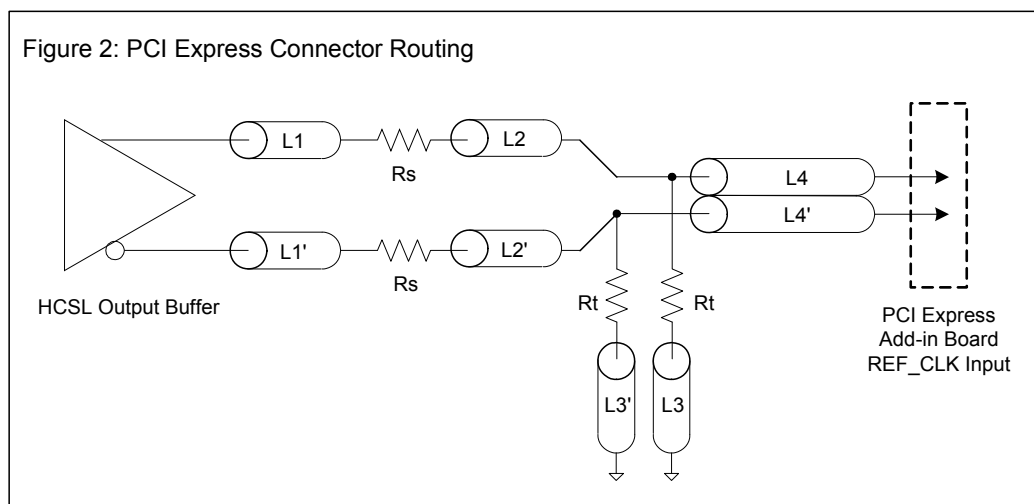
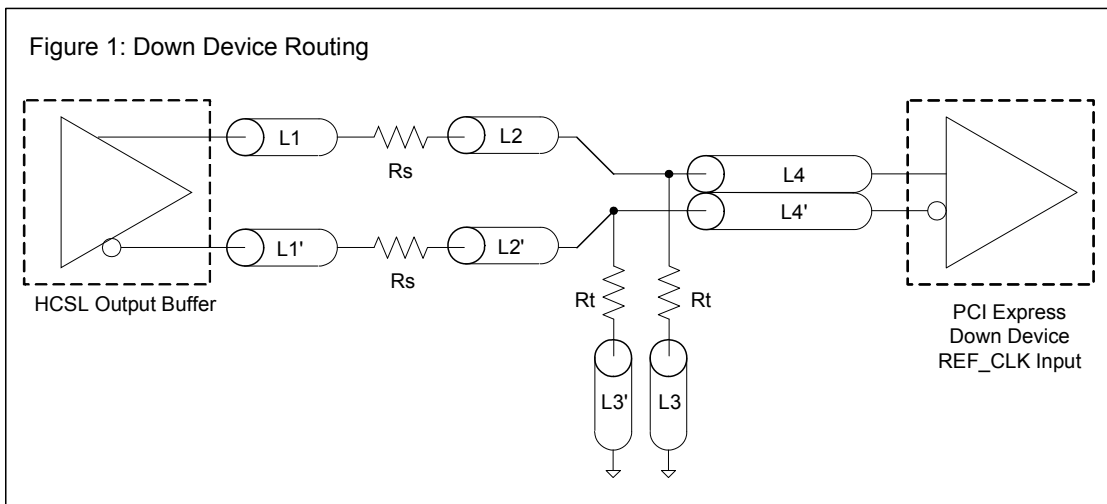
| SSC ON | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|        |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|        |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF    | 99.75            | 9.94906                | 9.99906                     | 10.02406                    | 10.02506             | 10.02607                    | 10.05107                    | 10.10107               | ns    | 1,2   |
|        | 133.00           | 7.44930                | 7.49930                     | 7.51805                     | 7.51880              | 7.51955                     | 7.53830                     | 7.58830                | ns    | 1,2   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The 9DB1904 itself does not contribute to ppm error.

| DIF Reference Clock                             |                    |      |        |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace     | 0.5 max            | inch | 1      |
| L2 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| L3 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| $R_s$   | 33                 | ohm  | 1      |
| $R_t$   | 49.9               | ohm  | 1      |

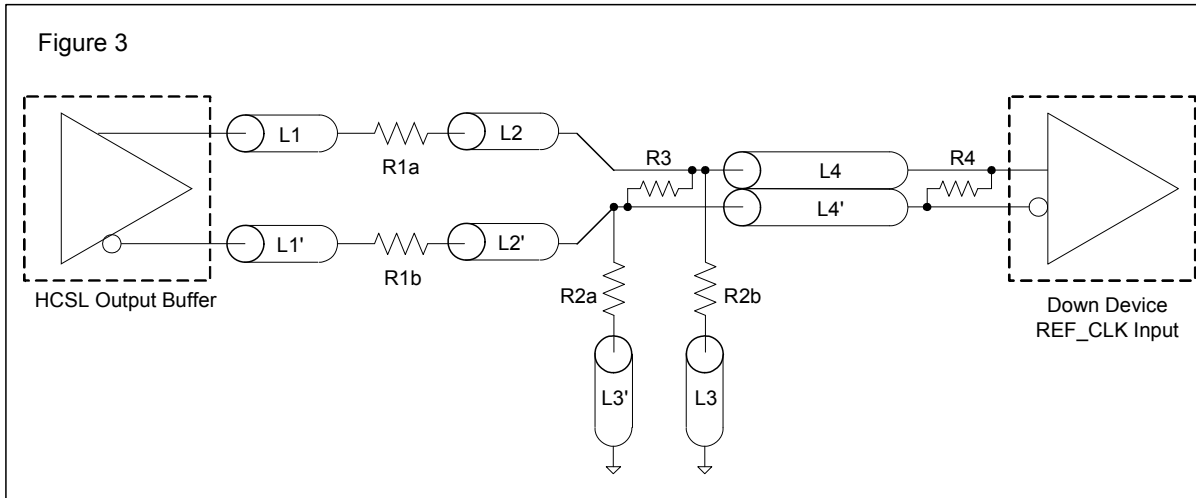
| Down Device Differential Routing                                 |                     |      |   |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max     | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace  | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector                    |                       |      |   |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max        | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace  | 0.225 min to 12.6 max | inch | 2 |

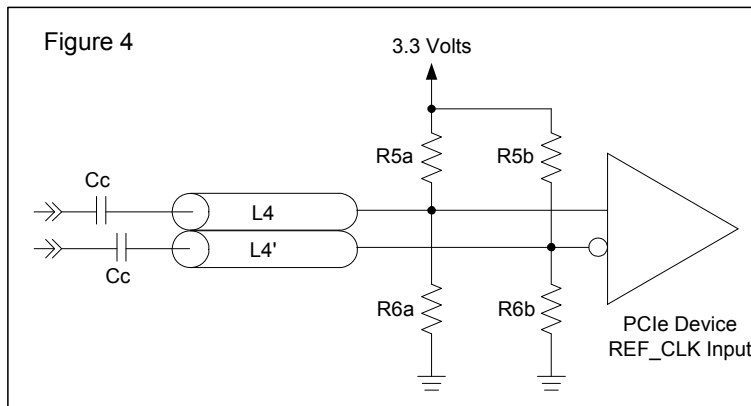


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) |       |      |    |      |      |     |                                |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff   | Vp-p  | Vcm  | R1 | R2   | R3   | R4  | Note                           |
| 0.45v   | 0.22v | 1.08 | 33 | 150  | 100  | 100 |                                |
| 0.58  | 0.28  | 0.6  | 33 | 78.7 | 137  | 100 |                                |
| 0.80  | 0.40  | 0.6  | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60  | 0.3   | 1.2  | 33 | 174  | 140  | 100 | Standard LVDS                  |

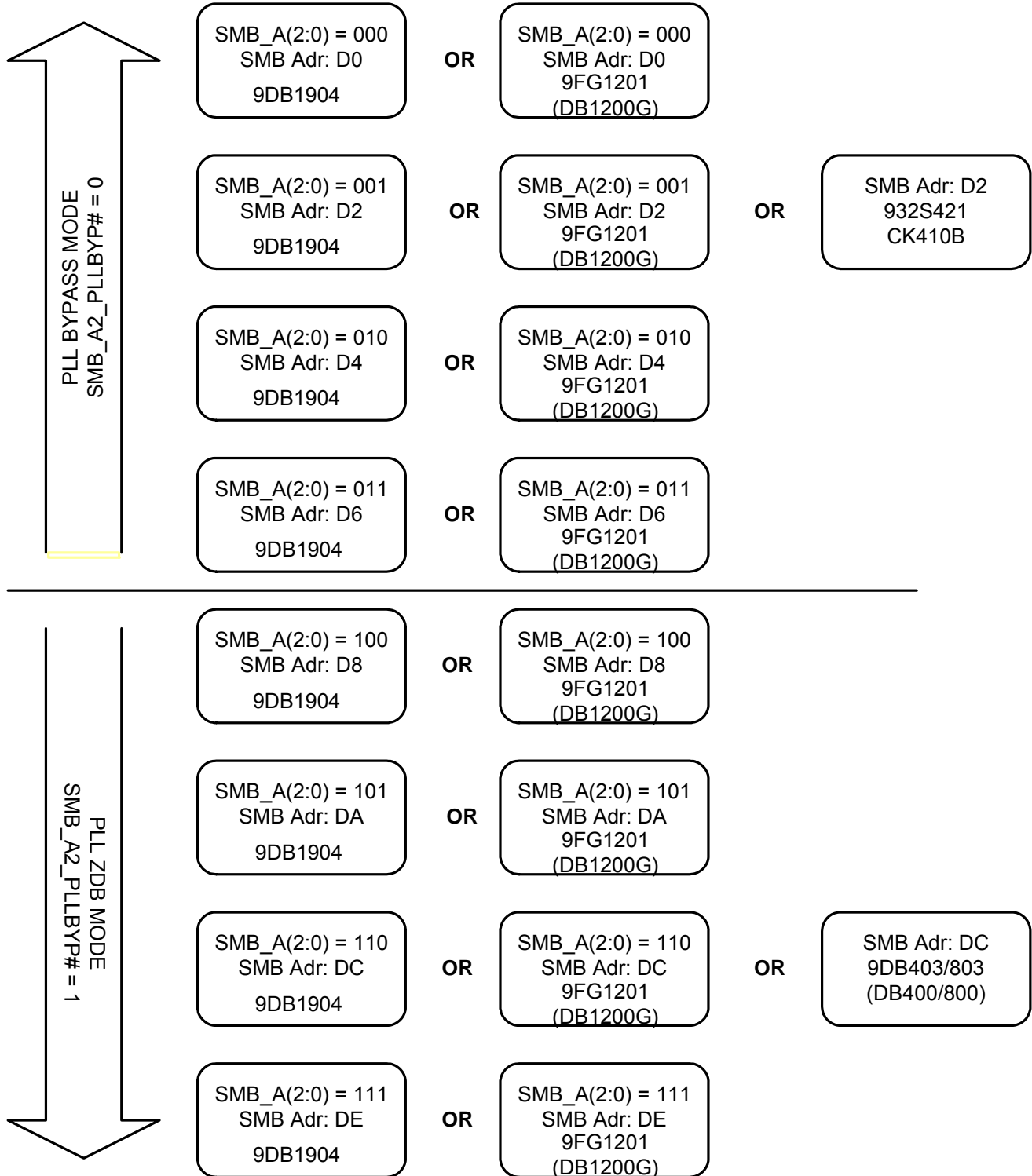
R1a = R1b = R1  
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) |             |      |
|---|-------------|------|
| Component   | Value       | Note |
| R5a, R5b  | 8.2K 5%     |      |
| R6a, R6b  | 1K 5%       |      |
| Cc  | 0.1 $\mu$ F |      |
| Vcm   | 0.350 volts |      |



**9DB1904 SMBus Address Mapping  
when using CK410/CK410B, 9FG1200, and  
9DB403/803**



## General SMBus serial interface information for the 9DB1904B

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $D4_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $D4_{(h)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $D5_{(h)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if  $X_{(h)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address $D4_{(h)}$ *  |           |                      |
| WR                          | WRite     |                      |
|                             |           | ACK                  |
| Beginning Byte = N          |           |                      |
|                             |           | ACK                  |
| Data Byte Count = X         |           |                      |
|                             |           | ACK                  |
| Beginning Byte N            | X Byte    |                      |
| ◊                           |           | ACK                  |
| ◊                           |           | ◊                    |
| ◊                           |           | ◊                    |
| ◊                           |           | ◊                    |
| Byte N + X - 1              |           |                      |
|                             |           | ACK                  |
| P                           | stoP bit  |                      |

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address $D4_{(h)}$ * |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address $D5_{(h)}$ * |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count = X  |
| ACK                        |                 |                      |
|                            |                 | Beginning Byte N     |
| ACK                        |                 |                      |
|                            |                 | ◊                    |
|                            |                 | ◊                    |
|                            |                 | ◊                    |
|                            |                 | ◊                    |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

SMBusTable: Reserved Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 6  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 5  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 4  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 3  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 2  | -     |      | Reserved         | R    |   |   | 0   |
| Bit 1  | -     |      | Reserved         | R    |   |   | 1   |
| Bit 0  | -     |      | Reserved         | R    |   |   | 1   |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name  | Control Function | Type | 0    | 1      | PWD |
|--------|-------|-------|------------------|------|------|--------|-----|
| Bit 7  |       | DIF_7 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 6  |       | DIF_6 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 5  |       | DIF_5 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 4  |       | DIF_4 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 3  |       | DIF_3 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 2  |       | DIF_2 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 1  |       | DIF_1 | Output Control   | RW   | Hi-Z | Enable | 1   |
| Bit 0  |       | DIF_0 | Output Control   | RW   | Hi-Z | Enable | 1   |

SMBusTable: Output and PLL BW Control Register

| Byte 2 | Pin #    | Name   | Control Function        | Type | 0       | 1      | PWD |
|--------|----------|--------|-------------------------|------|---------|--------|-----|
| Bit 7  | see note |        | PLL_BW# adjust          | RW   | High BW | Low BW | 1   |
| Bit 6  | see note |        | BYPASS# test mode / PLL | RW   | Bypass  | PLL    | 1   |
| Bit 5  |          | DIF_13 | Output Control          | RW   | Hi-Z    | Enable | 1   |
| Bit 4  |          | DIF_12 | Output Control          | RW   | Hi-Z    | Enable | 1   |
| Bit 3  |          | DIF_11 | Output Control          | RW   | Hi-Z    | Enable | 1   |
| Bit 2  |          | DIF_10 | Output Control          | RW   | Hi-Z    | Enable | 1   |
| Bit 1  |          | DIF_9  | Output Control          | RW   | Hi-Z    | Enable | 1   |
| Bit 0  |          | DIF_8  | Output Control          | RW   | Hi-Z    | Enable | 1   |

Note: Bit 7 is wired OR to the HIGH\_BW# input, any 0 selects High BW

Note: Bit 6 is wired OR to the SMB\_A2\_PLLBYP# input, any 0 selects Fanout Bypass mode

SMBusTable: Output Enable Readback Register

| Byte 3 | Pin # | Name | Control Function             | Type | 0        | 1 | PWD |
|--------|-------|------|------------------------------|------|----------|---|-----|
| Bit 7  |       |      | Readback - OE9# Input        | R    | Readback |   | X   |
| Bit 6  |       |      | Readback - OE8# Input        | R    | Readback |   | X   |
| Bit 5  |       |      | Readback - OE7# Input        | R    | Readback |   | X   |
| Bit 4  |       |      | Readback - OE6# Input        | R    | Readback |   | X   |
| Bit 3  |       |      | Readback - OE5# Input        | R    | Readback |   | X   |
| Bit 2  |       |      | Readback - OE_01234# Input   | R    | Readback |   | X   |
| Bit 1  | 8     |      | Readback - HIGH_BW# In       | R    | Readback |   | X   |
| Bit 0  | 72    |      | Readback - SMB_A2_PLLBYP# In | R    | Readback |   | X   |

**SMBusTable: Output Enable Readback Register**

| Byte 4 | Pin # | Name                      | Control Function | Type | 0        | 1 | PWD |
|--------|-------|---------------------------|------------------|------|----------|---|-----|
| Bit 7  | 69    | Readback - OE17_18# Input |                  | R    | Readback |   | X   |
| Bit 6  | 60    | Readback - OE15_16# Input |                  | R    | Readback |   | X   |
| Bit 5  |       | Reserved                  |                  |      |          |   | 0   |
| Bit 4  | 54    | Readback - OE14# Input    |                  | R    | Readback |   | X   |
| Bit 3  | 51    | Readback - OE13# Input    |                  | R    | Readback |   | X   |
| Bit 2  | 48    | Readback - OE12# Input    |                  | R    | Readback |   | X   |
| Bit 1  | 43    | Readback - OE11# Input    |                  | R    | Readback |   | X   |
| Bit 0  | 40    | Readback - OE10# Input    |                  | R    | Readback |   | X   |

**SMBusTable: Vendor & Revision ID Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0   |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0   |
| Bit 5  | -     | RID1 |                  | R    | - | - | 0   |
| Bit 4  | -     | RID0 |                  | R    | - | - | 1   |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0   |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0   |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0   |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1   |

**SMBusTable: DEVICE ID (194 Decimal or C2 Hex)**

| Byte 6 | Pin # | Name              | Control Function | Type | 0        | 1 | PWD |
|--------|-------|-------------------|------------------|------|----------|---|-----|
| Bit 7  | -     | Device ID 7 (MSB) |                  | RW   | Reserved |   | 1   |
| Bit 6  | -     | Device ID 6       |                  | RW   | Reserved |   | 1   |
| Bit 5  | -     | Device ID 5       |                  | RW   | Reserved |   | 0   |
| Bit 4  | -     | Device ID 4       |                  | RW   | Reserved |   | 0   |
| Bit 3  | -     | Device ID 3       |                  | RW   | Reserved |   | 0   |
| Bit 2  | -     | Device ID 2       |                  | RW   | Reserved |   | 0   |
| Bit 1  | -     | Device ID 1       |                  | RW   | Reserved |   | 1   |
| Bit 0  | -     | Device ID 0       |                  | RW   | Reserved |   | 0   |

**SMBusTable: Byte Count Register**

| Byte 7 | Pin # | Name | Control Function  | Type | 0 | 1 | PWD |
|--------|-------|------|---|------|---|---|-----|
| Bit 7  | -     | BC7  | Writing to this register configures how many bytes will be read back. | RW   | - | - | 0   |
| Bit 6  | -     | BC6  |   | RW   | - | - | 0   |
| Bit 5  | -     | BC5  |   | RW   | - | - | 0   |
| Bit 4  | -     | BC4  |   | RW   | - | - | 0   |
| Bit 3  | -     | BC3  |   | RW   | - | - | 0   |
| Bit 2  | -     | BC2  |   | RW   | - | - | 1   |
| Bit 1  | -     | BC1  |   | RW   | - | - | 1   |
| Bit 0  | -     | BC0  |   | RW   | - | - | 1   |

SMBusTable: Control Pin Readback Register

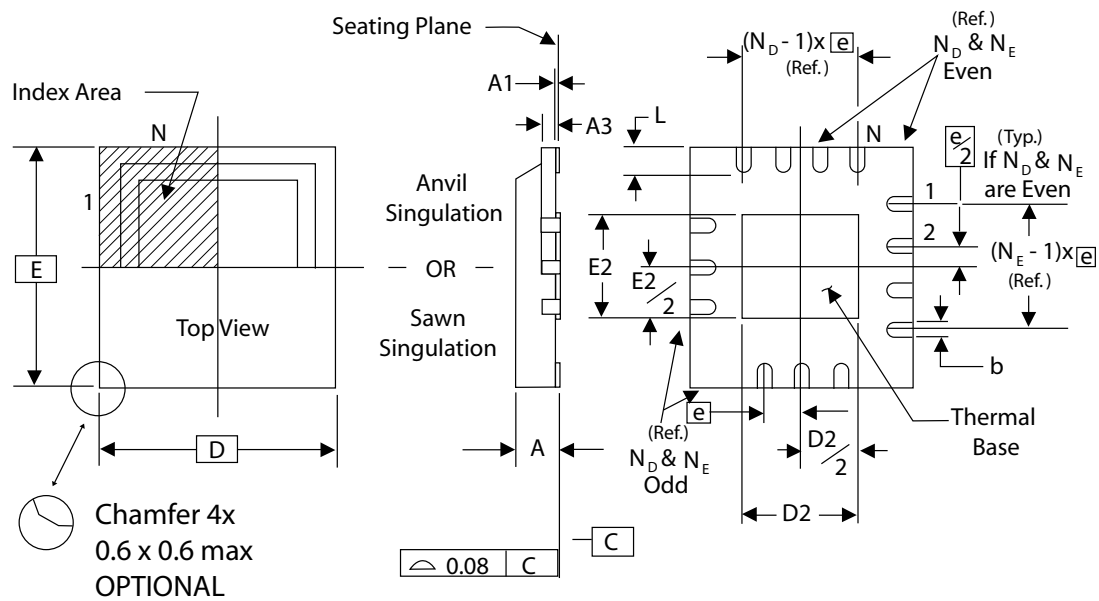
| Byte 8 | Pin # | Name                    | Control Function | Type | 0        | 1      | PWD   |
|--------|-------|-------------------------|------------------|------|----------|--------|-------|
| Bit 7  | 5     | Readback -100M_133M#_LV |                  | R    | Readback |        | Latch |
| Bit 6  |       | RESERVED                |                  |      |          |        | X     |
| Bit 5  |       | RESERVED                |                  |      |          |        | X     |
| Bit 4  |       | DIF_18                  | Output Control   | RW   | Hi-Z     | Enable | 1     |
| Bit 3  |       | DIF_17                  | Output Control   | RW   | Hi-Z     | Enable | 1     |
| Bit 2  |       | DIF_16                  | Output Control   | RW   | Hi-Z     | Enable | 1     |
| Bit 1  |       | DIF_15                  | Output Control   | RW   | Hi-Z     | Enable | 1     |
| Bit 0  |       | DIF_14                  | Output Control   | RW   | Hi-Z     | Enable | 1     |

SMBusTable: PLL Operating Set Point Register

| Byte 9 | Pin # | Name                        | Control Function | Type | 0   | 1 | PWD   |
|--------|-------|-----------------------------|------------------|------|---|---|-------|
| Bit 7  |       | RESERVED                    |                  |      |   |   | 0     |
| Bit 6  |       | RESERVED                    |                  |      |   |   | 0     |
| Bit 5  |       | RESERVED                    |                  |      |   |   | 0     |
| Bit 4  |       | RESERVED                    |                  |      |   |   | 0     |
| Bit 3  |       | RESERVED                    |                  |      |   |   | 0     |
| Bit 2  | -     | Frequency Select 100M_133M# |                  | RW   | See ICS9DB1904 1:1<br>PLL Programming Table |   | Latch |
| Bit 1  | -     | Frequency Select B          |                  | RW   |   |   | 0     |
| Bit 0  | -     | Frequency Select A          |                  | RW   |   |   | 1     |



**9DB1904B**  
**19 Output Differential Buffer for PCIe Gen2 and QPI**



**THERMALLY ENHANCED, VERY THIN, FINE PITCH**  
**QUAD FLAT / NO LEAD PLASTIC PACKAGE**

| SYMBOL | MIN.           | MAX. |
|--------|----------------|------|
| A      | 0.8            | 1.0  |
| A1     | 0              | 0.05 |
| A3     | 0.25 Reference |      |
| b      | 0.18           | 0.3  |
| e      | 0.50 BASIC     |      |

**DIMENSIONS**

| SYMBOL         | ICS 72L TOLERANCE |
|----------------|-------------------|
| N              | 72                |
| N <sub>D</sub> | 18                |
| N <sub>E</sub> | 18                |
| D x E BASIC    | 10.00 x 10.00     |
| D2 MIN. / MAX. | 5.75 / 6.15       |
| E2 MIN. / MAX. | 5.75 / 6.15       |
| L MIN. / MAX.  | 0.30 / 0.50       |

**Ordering Information**

| Part / Order Number | Shipping Packaging | Package    | Temperature |
|---------------------|--------------------|------------|-------------|
| 9DB1904BKLF         | Tubes              | 72-pin MLF | 0 to +70° C |
| 9DB1904BKLFT        | Tape and Reel      | 72-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.  
 "B" is the device revision designator (will not correlate with the datasheet revision).

## Revision History

| Rev. | Issue Date | Description   | Page #  |
|------|------------|---|---------|
| 0.1  | 7/1/2009   | Initial release   | -       |
| 0.2  | 7/8/2009   | Updated revision ID in Byte 5   | 13      |
| A    | 9/21/2010  | Updated electrical characteristics tables.<br>Added Test loads and terminations<br>Corrected minor typo's, move to release. | Various |
| B    | 9/23/2010  | 1. Updated electrical char tables<br>2. Updated test loads and termination figures<br>3. Added Period PPM tables            | Various |
| C    | 4/19/2011  | 1. Updated electrical tabels with Typ. Values<br>2. Updated Differential Clock Period PPM tables                            | Various |
|      |            |   |         |

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