LG Semicon Co.,Ltd.

GM71C4800C
GM71CS4800CL

524,288WORDS x 8 BIT
CMOS DYNAMIC RAM

Description

The GM71C4800C/CL is the new generation dynamic RAM organized 524,288 x 8 bit. GM71C4800C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4800C/CL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C4800C/CL to be packaged in standard 400 mil 28pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V+/-10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

* 524,288 Words x 8 Bit Organization
* Fast Page Mode Capability
* Single Power Supply (5V+/-10%)
* Fast Access Time & Cycle Time

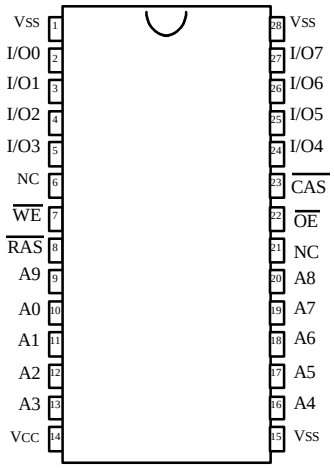
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C(S)4800C/CL-60	60	18	110	40
GM71C(S)4800C/CL-70	70	20	130	45

* Low Power
  Active : 715/660 mW(MAX)
  Standby : 5.5mW (CMOS level : MAX)
  1.1mW (L-series)
* $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
* All inputs and outputs TTL Compatible
* 1024 Refresh Cycles/16§Â
* 1024 Refresh Cycles/128§Â (L-series)
* Battery Back Up Operation (L-series)
* Self-Refresh Operation (GM71C4800C/CL)

Pin Configuration

28 SOJ



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A9	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O7	Data-In/Out	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C4800CJ-60 GM71C4800CJ-70	60ns 70§À	400 Mil 28 Pin Plastic SOJ
GM71CS4800CLJ-60 GM71CS4800CLJ-70	60ns 70§À	400 Mil 28Pin Plastic SOJ

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	C
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions* (T_A = 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

*Note: All voltage reffered to Vss

Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	I/O0-I/O7	I/O8-I/O15	Operation
	H	H	H	High-Z	High-Z	Standby
L	H	H	H	High-Z	High-Z	Refresh
L	L	H	L	D_{OUT}	High-Z	Lower Byte Read
	H	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	H	H	High-Z	High-Z	
H to L	L	-	-	High-Z	High-Z	CBR Refresh or Self Refresh
H to L	H	-	-	High-Z	High-Z	
H to L	L	-	-	High-Z	High-Z	

DC Electrical Characteristics (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min)	60§À	-	130	mA	1, 2
		70§À	-	120		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current (t_{RC} = t_{RC} min)	60§À	-	130	mA	2
		70§À	-	120		
I_{CC4}	Fast Page mode current Average Power Supply Current (t_{PC} = t_{PC} min)	60§À	-	130	mA	1, 3
		70§À	-	120		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$>=V_{CC}-0.2V, D_{OUT}=High-Z)		-	1	mA	4
			-	200	uA	4,5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60§À	-	130	mA	
		70§À	-	120		
I_{CC7}	Battery Back Up Current (Standby with CBR Refresh) (t_{RC}=125¥ìs, t_{RAS}<=1¥ìs, $\overline{WE}$, $\overline{OE}$=V_{IH}, $\overline{CAS}$ =V_{IL}, D_{OUT}=High-Z)		-	300	uA	4, 5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{CAS}$<=0.2V, D_{OUT} = High-Z)	GM71C4800C	-	1	mA	6
		GM71CS4800CL	-	200	uA	
$I_{I(L)}$	Input Leakage Current Any Input (0V<=V_{IN}<=6.5V)		-10	10	uA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<=V_{OUT}<=6.5V)		-10	10	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.
4. V_{IH}>=V_{CC}-0.2V, 0<=V_{IL}<=0.2V, Address can be changed once or less while $\overline{RAS}$=V_{IL}.
5. L-Series.
6. Self-refresh series. (GM71C(S)4800C/CL)

Capacitance (V_{CC} = 5V+/-10%, T_A = 25C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	§Ü	1
C_{I2}	Input Capacitance (Clocks)	-	7	§Ü	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	§Ü	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$= V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V+/-10%, T_A = 0 ~ 70C, Notes 1, 14, 15, 17, 18)

Test Conditions

Input rise and fall times : 5ns
Input level : V_{IL} = 0V , V_{IH} = 3.0V
Input timing reference level : 0.8V, 2.4V
Output timing reference level : 0.8V, 2.4V
Output load : 2TTL gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	130		-	§À	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	§À	
t_{CP}	$\overline{CAS}$ Percharge Time	10		10	-	§À	22
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	§À	
t_{CAS}	$\overline{CAS}$ Pulse Width	15		20	10,000	§À	
t_{ASR}	Row Address Set-up Time	0	-	0	-	§À	
t_{RAH}	Row Address Hold Time	10	-	10	-	§À	
t_{ASC}	Column Address Set-up Time	0	-	0	-	§À	19
t_{CAH}	Column Address Hold Time	15		15	-	§À	19
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	§À	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	§À	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	§À	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	§À	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	§À	20
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	15	-	20	-	§À	24
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	§À	25
t_{DZC}	$\overline{CAS}$ Setup Time from D_{IN}	0	-	0	-	§À	25
t_T	TransitionTime (Rise and Fall)	3	50	3	50	§À	7
t_{REF}	Refresh Period	-	16	-	16	§Â	
	Refresh Period (L-Series)	-	128	-	128	§Â	

Read Cycle

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	§À	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	§À	3, 4, 13
t_{AA}	Access Time from Address	-	30	-	35	§À	3, 5, 13
t_{OAC}	Access Time from $\overline{OE}$	-	15	-	20	§À	3
t_{RCS}	Read Command Setup Time	0	-	0	-	§À	19
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	§À	16, 19
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	§À	16
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	§À	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	-	35	-	§À	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	§À	
t_{OH}	Output Data Hold Time	5	-	5	-	§À	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	5	-	5	-	§À	
t_{OFF}	Output Buffer Turn-off Time	0	15	0	20	§À	6
t_{OEZ}	Output Buffer Turn-off Time from $\overline{OE}$	0	15	0	20	§À	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	-	20	-	§À	24

Write Cycle

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	§À	10, 19
t_{WCH}	Write Command Hold Time	15	-	15	-	§À	19
t_{WP}	Write Command Pulse Width	10	-	10	-	§À	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	§À	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	§À	21
t_{DS}	Data-in Setup Time	0	-	0	-	§À	11, 21
t_{DH}	Data-in Hold Time	15	-	15	-	§À	11, 21

Read- Modify-Write Cycle

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	150	-	180	-	§À	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	-	95	-	§À	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	-	45	-	§À	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	§À	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	-	20	-	§À	

Refresh Cycle

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	§À	19
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	§À	20
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	§À	19
t_{WRP}	WE Setup time(CBR refresh cycle)	10	-	10	-	§À	

Fast Page Mode Cycle

Symbol	Parameter	GM71C(S)4800 C/CL- 6 0		GM71C(S)4800 C/CL- 7 0		Unit	Note
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	§À	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	§À	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	§À	3, 13, 20
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	§À	
t_{CPW}	Fast Page ModeRead-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	55	-	65	-	§À	10,20
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	§À	

Self-Refresh Mode

Symbol	Parameter	GM71C(S)4800 C/CL-60		GM71C(S)4800 C/CL-70		Unit	Note
		Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width (Self-Refresh)	100	-	100	-	ns	
t_{RPS}	$\overline{RAS}$ Precharge Time (Self-Refresh)	110	-	130	-	§À	
t_{CHS}	$\overline{CAS}$ Hold Time (Self-Refresh)	-50	-	-50	-	§À	21

Notes:

1. AC Measurements assume t_T = 5§À.
2. Assumes that $t_{RCD} <= t_{RCD}$(max) and $t_{RAD} <= t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100§Ü.
4. Assumes that $t_{RCD} >= t_{RCD}$(max) and $t_{RAD} <= t_{RAD}$(max).
5. Assumes that $t_{RCD} <= t_{RCD}$(max) and $t_{RAD} >= t_{RAD}$(max).
6. t_{OFF}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only ; if $t_{WCS} >= t_{WCS}$(min), the cycle is an early write cycle and thedata out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} >= t_{RWD}$(min), $t_{CWD} >= t_{CWD}$(min), $t_{AWD} >= t_{AWD}$(min) and $t_{CPW} >= t_{CPW}$(min), the cycle is a read modify write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to WE leading edge in a delayed write or a read modify write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100¥ìs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eitht $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.

15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either T_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. The supply voltage with all Vcc pins must be on the same level.

    The supply voltage with all Vcc pins must be on the same level.
18. Do not enable D_{OUT} buffer when using delayed write timing.
19. If you use distributed CBR refresh mode with 15.6¥is interval in normal read/write cycle, CBR refresh should be executed within 15.6¥is immediately affter exiting from and before entering into self refresh mode.
20. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6us interval should be executed within 16ms immediately after exiting from and before entering into self refresh mode.
21. Repetitive self refresh mode without refreshing all memory is not allowed. once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

Package Dimensions

Unit: Inches (mm)

SOJ