

Version: 3.0

TECHNICAL SPECIFICATION

MODEL NO.: PW035XS4

Customer's Confirmation	
Customer	
Ву	PW035XS4
Бу	
	☐PVI's Confirmation
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Date: March 28, 2008

This technical specification is subject to change without notice.





Revision History

Rev.	Issued Date	Revised Contents
1.0	Apr.30, 2007	NEW
2.0	Nov.12, 2007	Modify
		Page 27: 14. Delete carton and change packing
3.0	March 28,2008	Change outline



TECHNICAL SPECIFICATION

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1. Application

This technical specification applies to 3.5" color TFT-LCD module, PW035XS4.

The applications of the panel are car TV, portable DVD, DV,GPS, multimedia applications and other AV systems..

2. Features

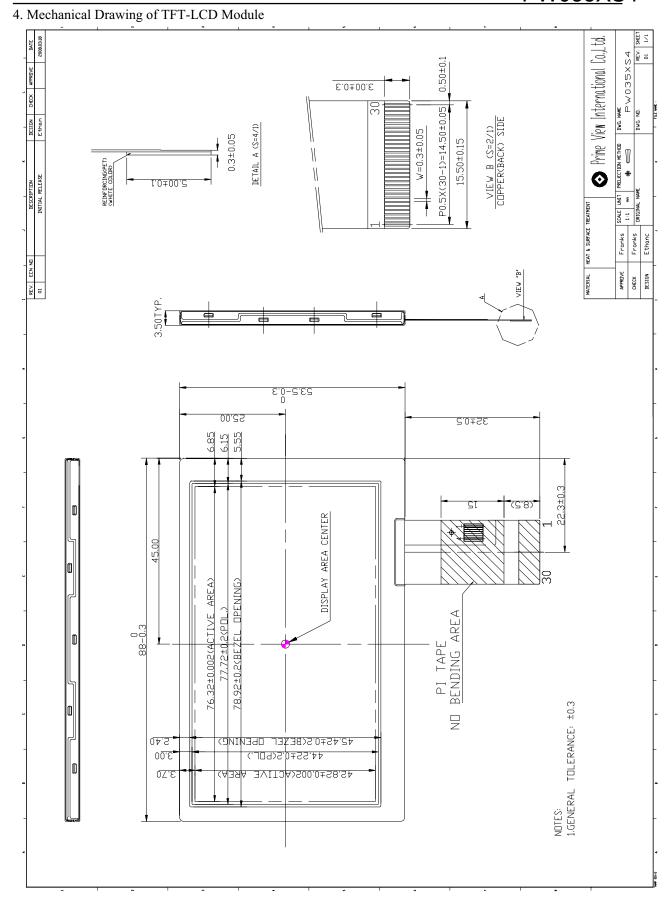
- . Amorphous silicon TFT-LCD panel with LED Backlight unit.
- . Compatible with NTSC & PAL system
- . Pixel in stripe configuration
- . Slim and compact
- . Image Reversion: Up/Down and Left/Right
- . Support multi display mode (If you use this mode ,you must use PVI-1004D's timing controller (made by PVI))
- . Wide viewing angle

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5 (16:9 diagonal)	inch
Display Format	320x(RGB)x234	dot
Active Area	76.32(H)x42.82(V)	mm
Pixel Pitch	0.2385(H)×0.1829 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	$88.0(W) \times 53.5(H) \times 3.5(D)(typ.)$	mm
Weight	34±5	g
Back-light	6-LED	
Surface Treatment	Anti – Glare	
Display model	Normally white	
Gray scale inversion direction	12 o'clock [Note 10- 1]	



PW035XS4





5. Input / Output Terminals

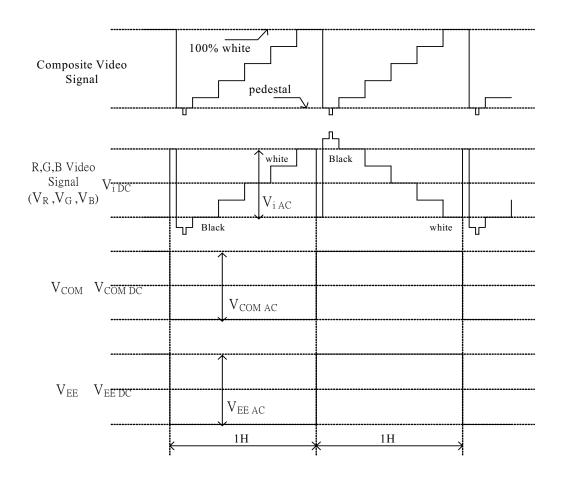
TFT-LCD Module Connector

FPC Down Connect, 30Pins, Pitch: 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GLED1	I	Ground for LED backlight	
2	VLED1	I	Supply voltage of LED backlight	Note 5-7
3	GLED2	I	Ground for LED backlight	
4	VLED2	I	Supply voltage of LED backlight	Note 5-7
5	GND	-	Ground for logic circuit	
6	V _{cc}	I	Supply voltage of logic control circuit for gate driver	Note 5-2
7	V _{EE}	I	Negative power for gate driver	Note 5-3
8	V_{GH}	I	Positive power for gate driver	Note 5-4
9	STVD	I/O	Vertical start pulse	N. 1. 5.0
10	STVU	I/O	Vertical start pulse	Note 5-8
11	CKV	I	Shift clock for gate driver	
12	U/D	I	Up / Down control for gate driver	Note 5-8
13	OE3	I	Output enable for gate driver	
14	OE2	I	Output enable for gate driver	
15	OE1	I	Output enable for gate driver	
16	V_{COM}	- 1	Common electrode voltage	Note 5-1
17	STHL	I/O	Start pulse for source driver	Note 5-8
18	V_{SS2}	-	Ground for analog circuit	
19	V_R	I	Video Input R	
20	V_{G}	I	Video Input G	
21	V_B	I	Video Input B	
22	V_{SS1}	-	Ground for digital circuit	
23	V_{DD2}	ı	Supply power of analog circuit	Note 5-5
24	CPH1	ı	Sampling and shift clock for source driver	
25	CPH2 I Sampling		Sampling and shift clock for source driver	Note 5-9
26	CPH3		Sampling and shift clock for source driver	
27	V_{DD1}	I	Supply power for digital circuit	Note 5-6
28	R/L	I	Left / Right control for source driver	Note 5-8
29	OEH	I	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-8

Note5-1: $V_{COM}(Typ.) = 6.0 V_{PP}$.

Phase of the video signal input and V_{COM} The relation between these values could refer to 8-1 Operating condition



Liquid crystal transmission of the video signal input , V_{COM} and timing

	V_{COM}		
	H Level	L Level	
Video Signal Input Maximum	Black	White	
Video Signal Input Minimum	White	Black	

White: maximum transmission / Black: minimum transmission

Note 5-2 : $V_{CC}TYP. = +3.3V$

Note 5-3 : V_{EE} TYP.=-12V

Note 5-4 : V_{GH} TYP.=+17V

Note 5-5: V_{DD2} TYP.=+5V



Note 5-6 : V_{DD1} TYP.=+3.3V

Note 5-7: I_{LED1}, I_{LED2} TYP.=20 mA

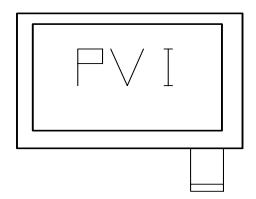
Note 5-8: STHL, STHR and R/L mode

R/L	STHL	STHR	Remark
$High(V_{DD1})$	Output	Input	Left to Right
Low(0 Volt.)	Input	Output	Right to Left

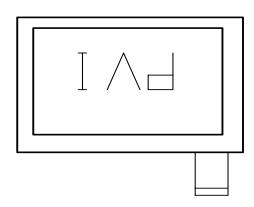
STVD,STVU and U/D mode

U/D	STVD	STVU	Remark	
High(V _{CC})	High(V _{CC}) Input		Down to Up	
Low(0 Volt.)	Output	Input	Up to Down	

U/D(PIN 12)=Low R/L(PIN 28)=High



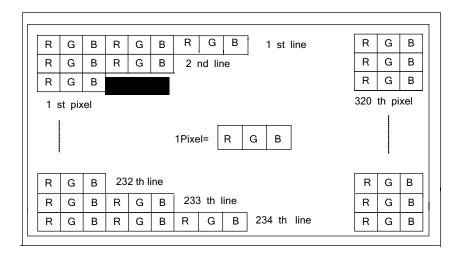
U/D(PIN 12)=High R/L(PIN 28)=Low



Note 5 –9 : The CPH1 reference Fig.8-1 Sampling clock timing CPH2 and CPH3 connect GND.



6. Pixel Arrangement





7. Absolute Maximum Ratings:

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V, Ta = 25 °C

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD2}	-0.3	+5.8	V	
		V_{DD1}	-0.3	+7.0	V	
		V _{cc}	-0.3	+6.0	V	
		V _{GH} -V _{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+25.0	V	
	L Level	V _{EE}	-16	+0.3	V	

8. Electrical Characteristics

8-1) Operating Condition for TFT-LCD panel

Ta=25°C

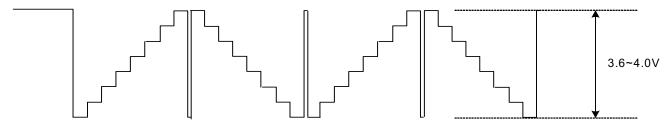
		l		I		I	Ta-23 (
Parameter		Symbol	MIN.	Тур.	MAX.	Unit	Remark
	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
Supply Voltage For Source Driver	Logic	V _{DD1}	+3.0	+3.3	+3.6	V	Depend on T/C
		- 001	+4.5	+5.0	+5.5		Signal voltage
	V	GH	+15	+17	+19	V	
	VE	E DC	-13	-12	-10.5	V	DC Component of V _{EE}
Supply Voltage For Gate Driver	VE	E AC	-	+6.0	-	V _{P-P}	AC Component of V_{EE}
	Logic	V _{CC}	+3.0	+3.3	+3.6	V	Depend on T/C
			+4.5	+5.0	+5.5]	Signal voltage
Analog Signal input Level	Vi	AC	-	+3.6	+4.0	V	Note 8-2
(V_R, V_G, V_B)	Vi	DC	-	2.5	-	V	
Digital input voltage	H level	V _{IH}	0.7 VDD1	-	V _{DD1}	V	
Digital iliput voltage	L level	V _{IL}	-0.3	-	0.3 V _{DD1}	V	
Digital output voltage	H level	V _{OH}	0.7 V _{DD1}	-	V _{DD1}	V	
Digital output voltage	L level	V _{OL}	-0.3	-	0.3 V _{DD1}	V	
V_{COM}		V _{COM AC}	-	+6.0	-	V _{P-P}	AC Component of V _{COM}
		V _{COM DC}	-	1.5	-	٧	DC Component of V _{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{\text{COM DC}}$ level shall be adjustable , and the adjustable level range is $1.5V\pm1V$, every module's $V_{\text{COM DC}}$ level shall be carefully adjusted to show a best image performance.



PW035XS4

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



8-2) Recommended driving condition for LED backlight

Ta = 25 °C

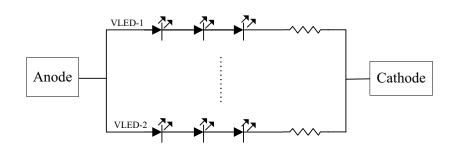
Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	VLED1			(10.8)	V	Note 8-3
	VLED2	-	-			11016-0-0
	ILED1		20			
Supply current of LED backlight	ILED2	-	20	-	mA	Note 8-4
Backlight Power Consumption	PLED	-	-	432	mW	Note 8-3/Note 8-5

Note 8-3: I_{LED}= 20mA,constant current

Note 8-4: The LED driving condition is defined for each LED module. (3 LED Serial)

Input current = 20mA * 2

Note 8-5 : $P_{\text{LED}} = V_{\text{LED1}} * I_{\text{LED1}} + V_{\text{LED2}} * I_{\text{LED2}}$.



8-7) Power Consumption

Ta = 25 °C

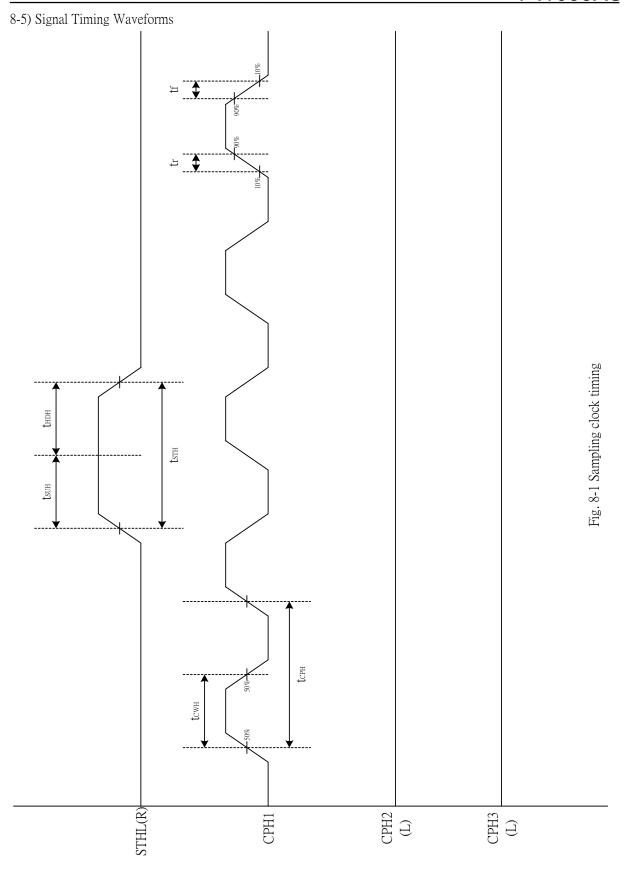
Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I _{GH}	$V_{GH} = +17V$	0.1	0.3	mA	
Supply current for Gate Driver (Low level)	I _{EE}	$V_{EE} = -12V$	0.1	0.3	mA	V_{EE} center voltage
Supply current for Source Driver(Digital)	I _{DD1}	$V_{DD1} = +3.3V$	0.8	1.6	mA	
Supply current for Source Driver(Analog)	I _{DD2}	V _{DD2} =+5V	0.35	7.0	mA	
Supply current for Gate Driver (Digital)	I _{CC}	$V_{CC} = +3.3V$	0.1	0.3	mA	
LCD Panel Power Consumption	-	-	23.4	50	mW	
Backlight Power Consumption	PLED	-	396	432	mW	
Total Power Consumption	-	-	420	482	mW	

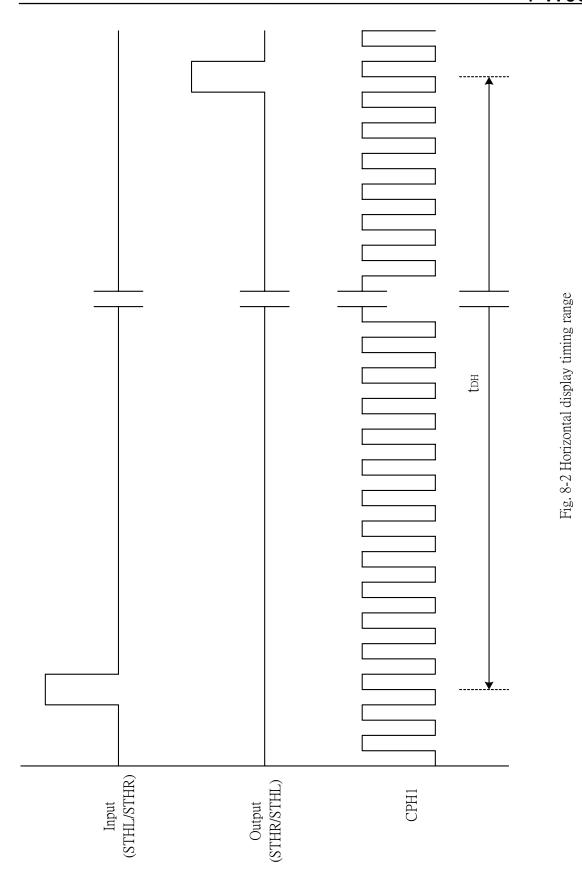


8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Тур.	Max.	Unit	Remark
Rising time	$t_{\rm r}$	-	-	10	ns	
Falling time	$t_{\rm f}$	-	-	10	ns	
High and low level pulse width	t_{CPH}	147	156	166	ns	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	$t_{ m SUH}$	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_{H}	61.5	63.5	65.5	μ s	STHR,STHL
OEH pulse width	t _{OEH}	-	1.6	-	μ s	OEH
Sample and hold disable time	$t_{\rm DIS1}$	-	4.4	-	μ s	
OEV pulse width	t _{OEV}	-	12	-	μ s	OEV
CKV pulse width	t_{CKV}	-	32	-	μ s	CKV
Clean enable time	$t_{\rm DIS2}$	-	6	-	μ s	
Horizontal display timing range	t_{DH}	-	320	-	t_{CPH}	
STV setup time	$t_{ m SUV}$	400	-	-	ns	
STV hold time	$t_{ m HDV}$	400	-	-	ns	STVU,STVD
STV pulse width	t_{STV}	-	-	1	t_{H}	STVU,STVD
Horizontal lines per field	$t_{ m V}$	256	262	268	t_{H}	
Vertical display start	$t_{ m SV}$		3	-	$t_{\rm H}$	
Vertical display timing range	$t_{ m DV}$		234	-	$t_{\rm H}$	
VCOM rising time	t _{rCOM}		-	5	μ s	
VCOM falling time	t_{fCOM}		-	5	μ s	
VCOM delay time	t _{DCOM}		-	3	μ s	
RGB delay time	t _{DRGB}		-	1	μ s	

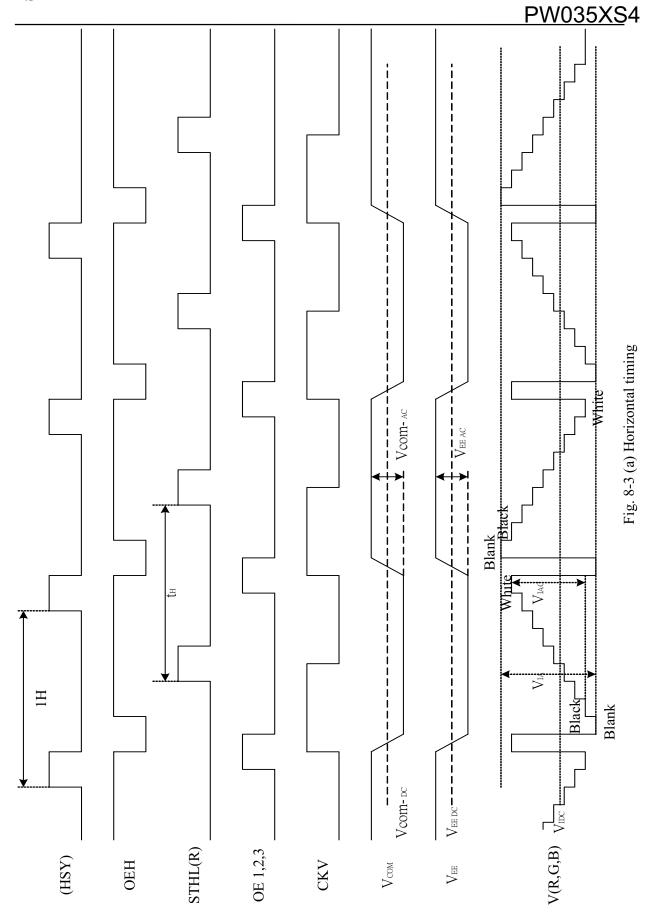


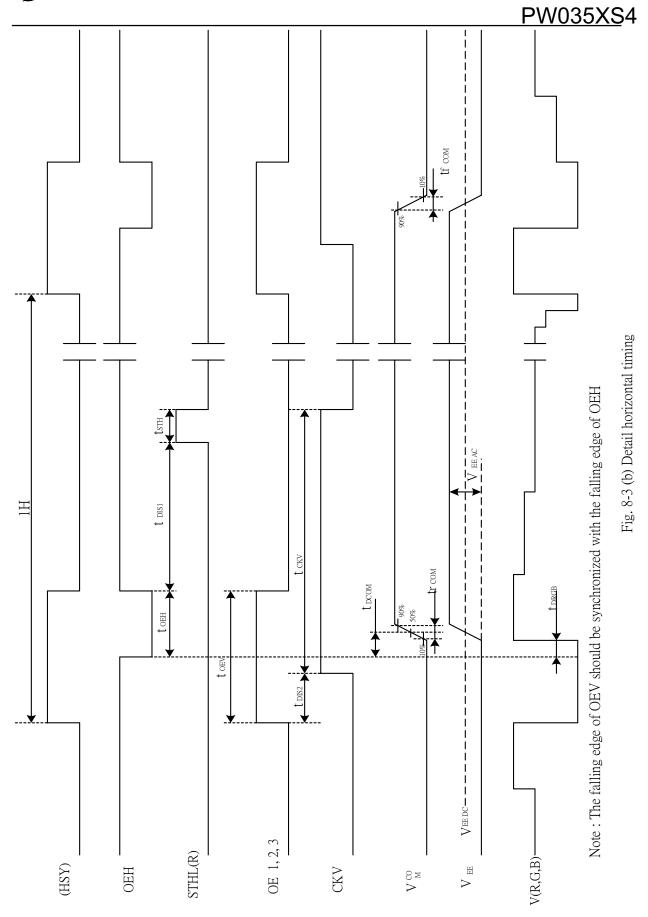




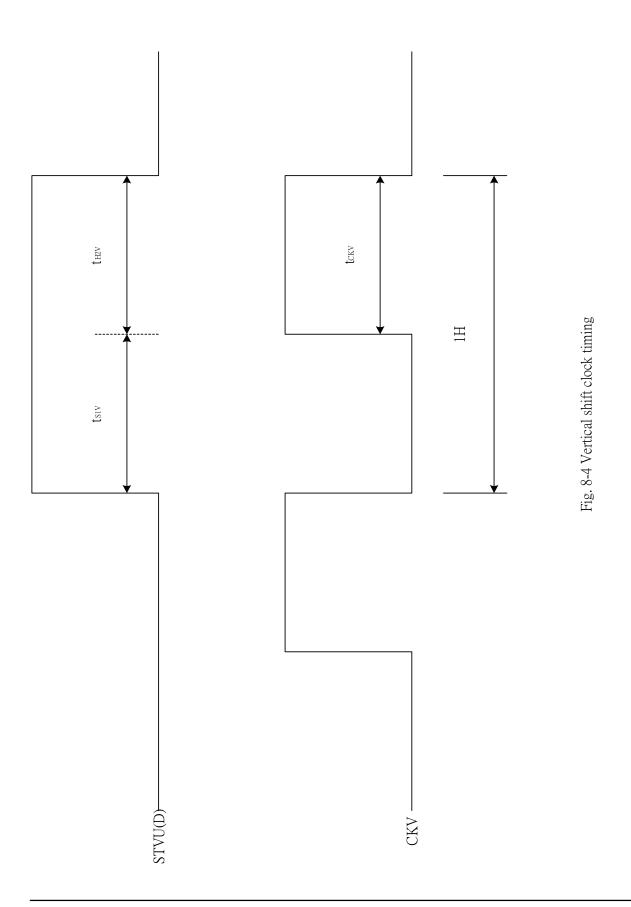
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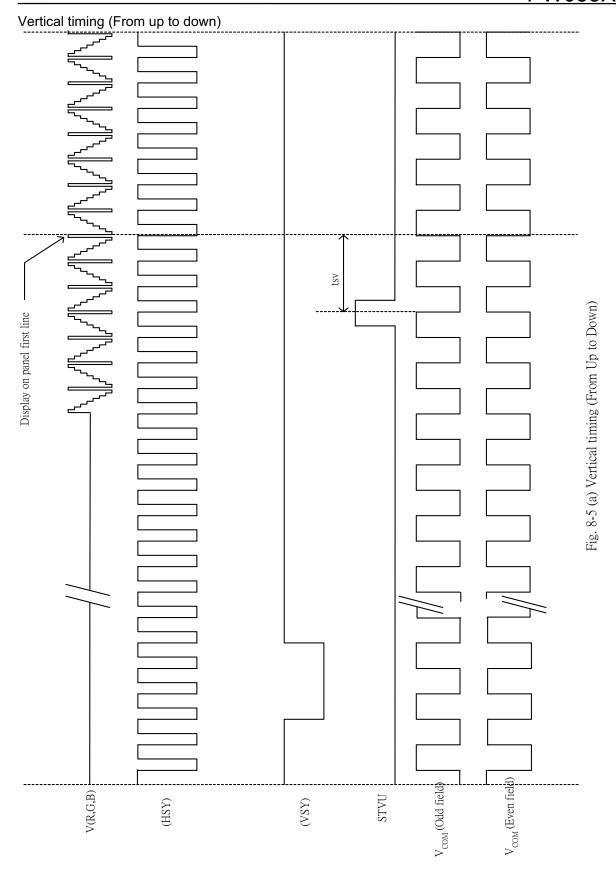




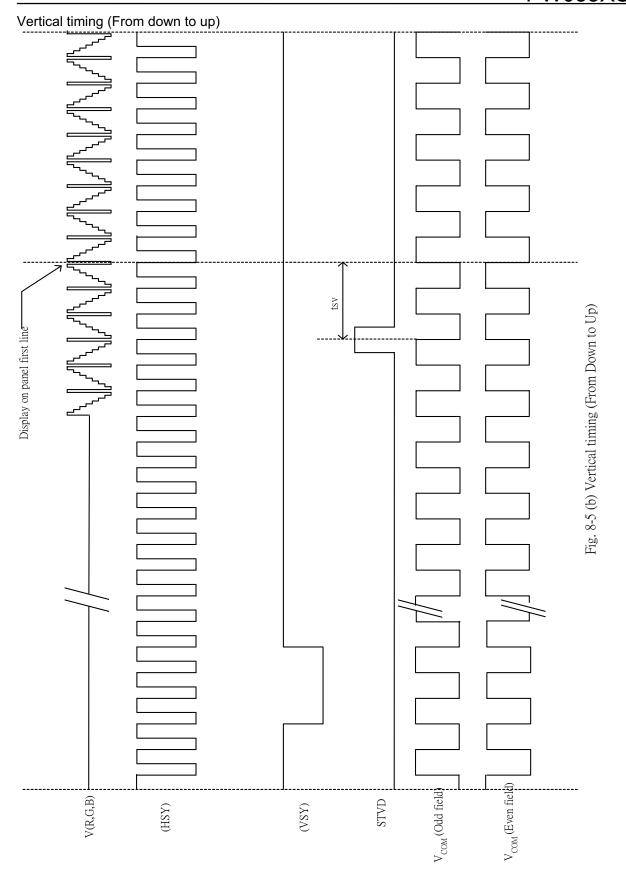
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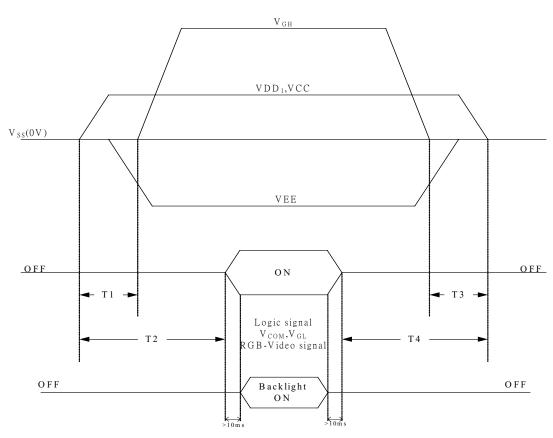






9. Power On Sequence

The Power on Sequence only effect by V_{CC} , V_{SS} , V_{DD} , V_{EE} and V_{GH} , the others do not care.



- 1) 10ms≦T1<T2
- 2) $0ms < T3 \le T4 \le 10ms$



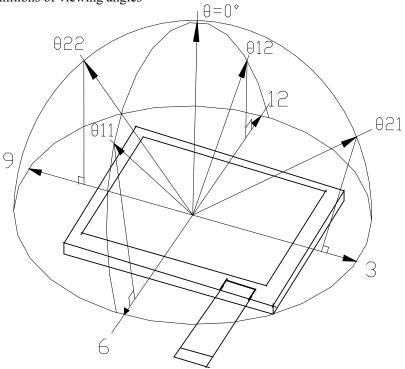
10. Optical Characteristics

10-1) Specification:

 $Ta = 25^{\circ}C$

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing	Horizontal	θ 21, θ 22		55	60		deg	
Angle	Vertical	θ 11	CR≧10	35	40		deg	Note 10-1
		θ 12		45	50		deg	
Contrast Ratio		CR	At optimized	200	350		-	Note 10-2
			Viewing angle					
Response time	Rise	Tr	$\theta = 0^{\circ}$		15	20	ms	Note 10-4
	Fall	Tf	0 -0		25	30	ms	
Uniformity		U	9 point	75	80		-	Note 10-3
Brightness		L	$\theta = 0^{\circ}$	300	350		cd/m²	
White Chromaticity		x	$\theta = 0^{\circ}$	0.29	0.32	0.35	-	
		У	$\theta = 0^{\circ}$	0.31	0.34	0.37	-	
LED Life time		-	+25°C	20000	30000		hrs	Note 10-5

Note 10-1: The definitions of viewing angles



Luminance when Testing point is White Note 10-2:CR =Luminance when Testing point is Black

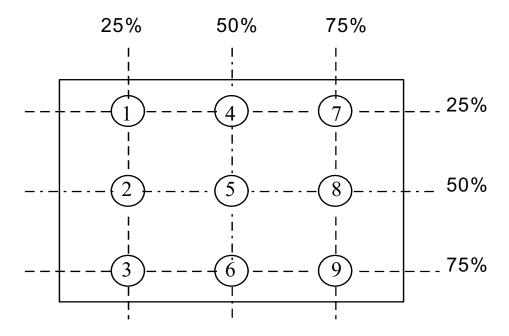
(Testing configuration see 10-2)

Contrast Ratio is measured in optimum common electrode voltage.

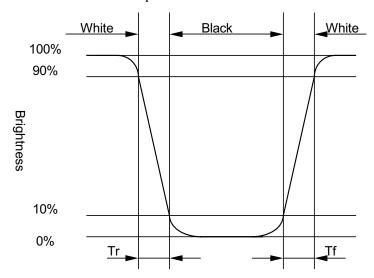


Note 10-3 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (after 10 minutes operation).

U = The Minimum Brightness of the 9 testing Points
The Maximum Brightness of the 9 testing Points

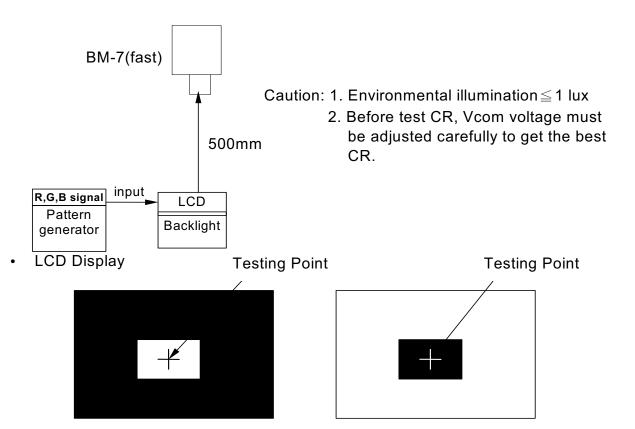


Note 10-4: The definition of response time:



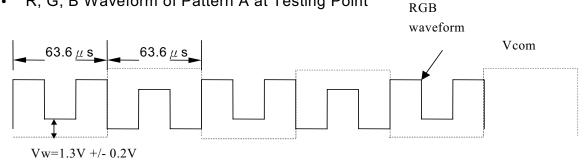
Note 10-5: The "LED Life time " is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25° C and I_{LED} =20mA.

10-2) Testing configuration

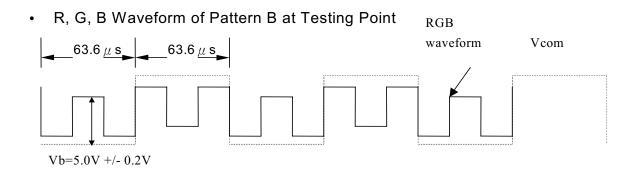


R, G, B Waveform of Pattern A at Testing Point

Pattern A



Pattern B





11. Handling Cautions

11-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

- a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

11-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.



12. Reliability Test

No	Test Item	Test Condition	Note
1	High Temperature Storage Test	$Ta = +85^{\circ}C$, 240 hrs	
2	Low Temperature Storage Test	$Ta = -30^{\circ}C$, 240 hrs	
3	High Temperature Operation Test	$Ta = +75^{\circ}C$, 240 hrs	
4	Low Temperature Operation Test	$Ta = -20^{\circ}C$, 240 hrs	
5	High Temperature & High Humidity Operation Test	$Ta = +60^{\circ}C$, 95%RH, 240 hrs	
6	Thermal Cycling Test	-30° C ← → $+80^{\circ}$ C , 100 Cycles	
	(non-operating)	60 min 60 min	
7	Vibration test (non-operating)	Frequency: 10 ~ 55Hz Amplitude: 1mm, sweep time: 11 mins Test period: 6 cycles for each direction of X,Y, Z	
8	Shock Test(non-operating)	100G, 6ms, 3cycles for each direction of X,Y,Z	
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ± 200 V	
		1 time / each terminal	

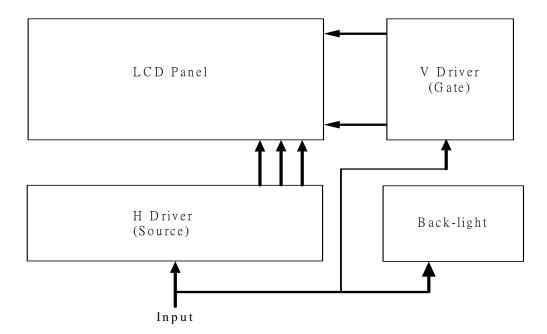
Ta: ambient temperature

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including: line defect, no image). All the cosmetic specification is judged before the reliability stress.



13. Block Diagram





14. Packing

