

Low Voltage, 1.2 Ω, Dual SPDT Analog Switch

DESCRIPTION

The DG2725 is a CMOS Dual SPDT (Dual Single Pole Double Throw) analog switch. It features low on-resistance of 0.7 Ω at 3 V power supply, fast switching speed, and low power consumption.

The DG2725 conducts signals equally at both directions and protects COM1 and COM2 pins at Power Off condition. The COM1 and COM2 leakage is guaranteed to be less than 1 μA when V+ is at 0 V. The DG2725 operates in a wide voltage range of 1.65 V to 5 V, and can be controlled by low voltage logic signals.

The DG2725 also features supply current even with control signal is at low voltage below the V+ voltage. The well matched dual SPDT is designed for break before make switching operation.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2725 are offered in a miniQFN package. The miniQFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free “-E4” suffix. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- Low Voltage Operation (1.65 V to 5 V)
- Low On-Resistance - 1.2 Ω at V+ = 3 V
- Power Off Protection on COM1 and COM2 pins
- Latch up current great than 300 mA per JESD78
- **Halogen-free according to IEC 61249-2-21 definition**
- **Compliant to RoHS Directive 2002/95/EC**

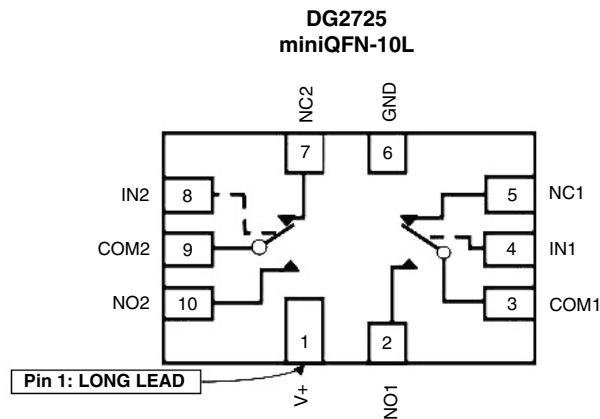


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

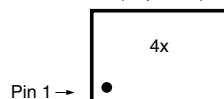
- PMPs and PDAs
- Modems and peripherals
- Computers and ebooks
- Tablet devices
- Displays and gaming
- STB

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: 4x for DG2725
x = Date/Lot Traceability Code

(Top View)



Note: Pin 1 has long lead

TRUTH TABLE		
Logic	NC1, 2	NO1, 2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85°C	miniQFN10	DG2725DN-T1-GE4



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Reference to GND	V+	- 0.3 to 5.5	V	
	IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)		
Current (Any terminal except NO, NC or COM)		30	mA	
Continuous Current (NO, NC, or COM)		± 350		
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500		
Storage Temperature (D Suffix)		- 65 to 150	°C	
Power Dissipation (Packages) ^b	miniQFN10 ^c	208	mW	

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 4.0 mW/C above 70 °C.

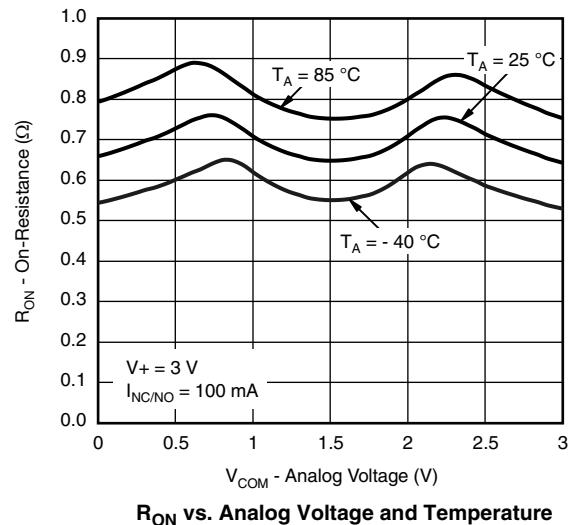
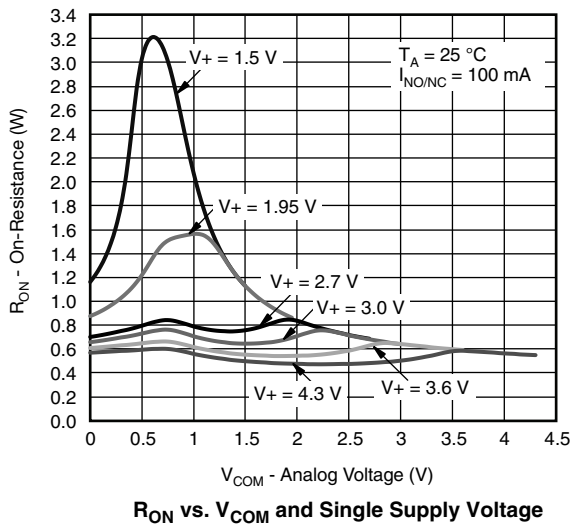
SPECIFICATIONS (V+ = 3 V)								
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 V or 1.65 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit	
				Min. ^b	Typ. ^c	Max. ^b		
Analog Switch								
Analog Signal Range ^d	V _{ANALOG}	R _{DS(on)}	Full	0		V+	V	
On-Resistance	R _{DS(on)}	V+ = 3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.7 V			0.7	1.2	Ω	
		V+ = 3 V, I _{NO/NC} = 100 mA, V _{COM} = 2.3 V			0.65			
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V			0.55	1		
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 2.5 V			0.42			
R _{ON} Match ^d	ΔR _{ON}	V+ = 3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.7 V V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V			0.02	0.25	Ω	
R _{ON} resistance flatness ^d	R _{ON} flatness	V+ = 3 V and 4.3 V, I _{NO/NC} = 100 mA			0.13	0.4		
Switch Off Leakage Current	I _{NO/NC(off)}	V+ = 4.3 V, V _{NO/NC} = 0.3 V/4.0 V, V _{COM} = 4.0 V/0.3 V	Room	- 10		10	nA	
			Full	- 50		50		
	Room		- 10		10			
	Full		- 50		50			
Channel-On Leakage Current	I _{COM(on)}	V+ = 4.3 V, V _{NO/NC} = V _{COM} = 4.0 V/0.3 V	Room	- 10		10	nA	
			Full	- 50		50		
Digital Control								
Input High Voltage	V _{INH}	V+ = 1.65 V to 4.3 V	Full	1.7			V	
Input Low Voltage	V _{INL}		Full			0.4		
Input Capacitance	C _{IN}		Full		6		pF	
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA	
Dynamic Characteristics								
Break-Before-Make Time ^e	t _{BBM}	V+ = 3.6 V, V _{NO} , V _{NC} = 1.5 V, R _L = 50 Ω, C _L = 35 pF	Room	2			ns	
Turn-On Time ^e	t _{ON}		Room			95		
			Full			100		
Turn-Off Time ^e	t _{OFF}		Room			50		
			Full			55		
Off-Isolation ^d	O _{IRR}	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz	Room		- 85		dB	
Crosstalk ^d	X _{TALK}		Room		- 95			
3dB bandwidth ^d		R _L = 50 Ω, C _L = 5 pF	Room		62		MHz	

SPECIFICATIONS ($V_+ = 3\text{ V}$)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3\text{ V}, \pm 10\%, V_{IN} = 0.4\text{ V}$ or 1.65 V^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Dynamic Characteristics							
NO, NC Off Capacitance ^d	$C_{NO(off)}$	$V_{IN} = 0\text{ V}$, or V_+ , $f = 1\text{ MHz}$	Room		24		pF
	$C_{NC(off)}$				30		
Channel On Capacitance ^d	$C_{NO(on)}$				100		
	$C_{NC(on)}$				100		
Power Supply							
Power Supply Range	V_+			1.65		4.3	V
Power Supply Current	I_+	$V_{IN} = 0$ or V_+	Full	- 1	0.01	1.0	μA
Supply Current per Logic Input	I_+T	$V_+ = 4.3\text{ V}, V_{INx} = 2.6\text{ V}$	Room		7		
		$V_+ = 4.3\text{ V}, V_{INx} = 1.8\text{ V}$	Room		15		
Power OFF COM pin Leakage	I_{OFF}	$V = 0\text{ V}, V_{IN} = 4.3\text{ V}, NCx, NOx$ floating	Full	- 1		+ 1	

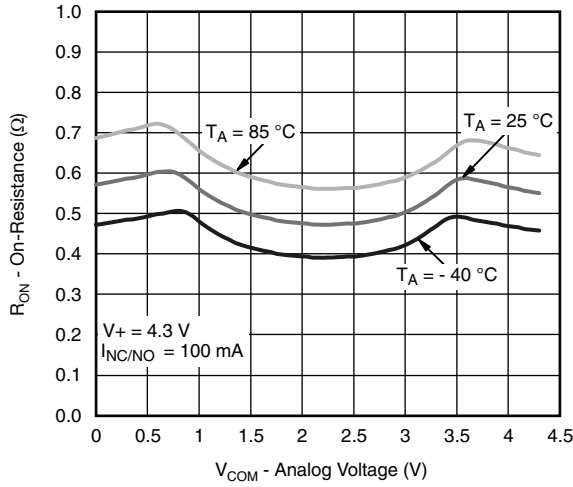
Notes:

- Room = 25 °C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, not subjected to production test.
- V_{IN} = input voltage to perform proper function.

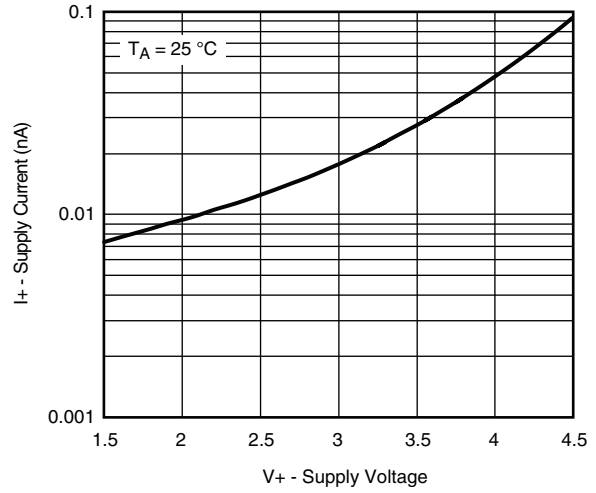
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ °C}$, unless otherwise noted)


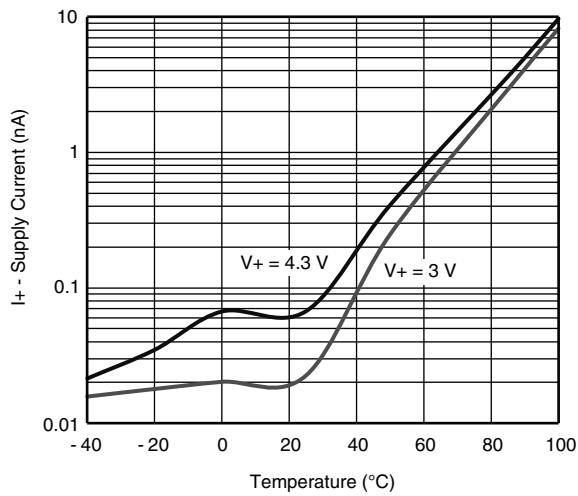
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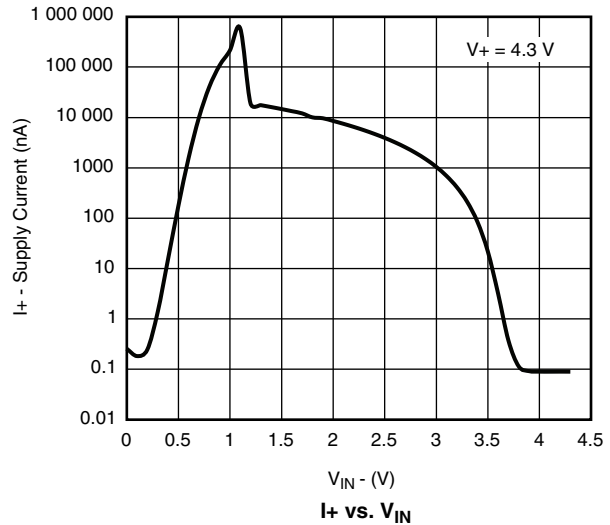
R_{ON} vs. Analog Voltage and Temperature



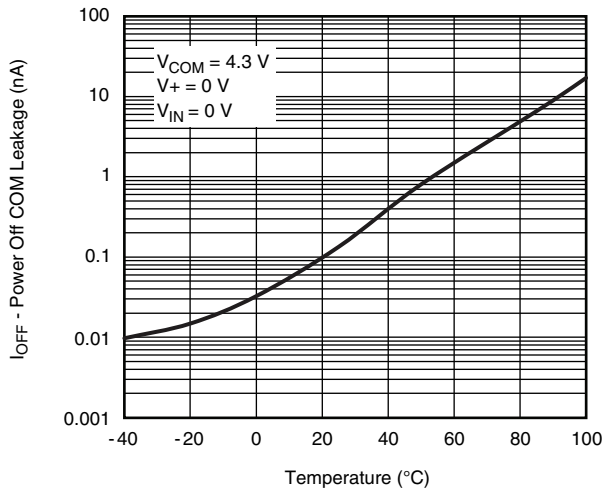
I+ vs. V+



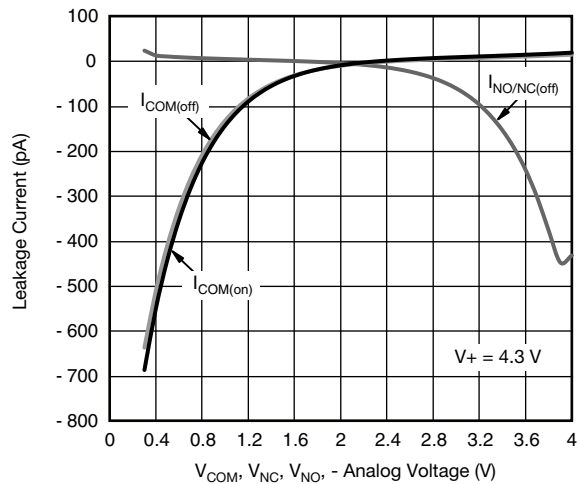
I+ Supply Current vs. Temperature



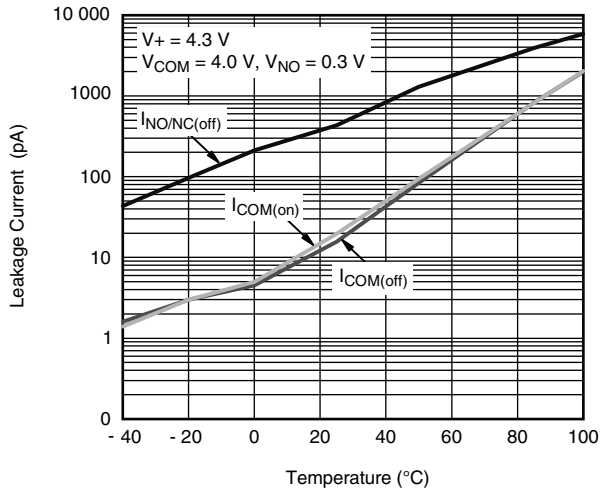
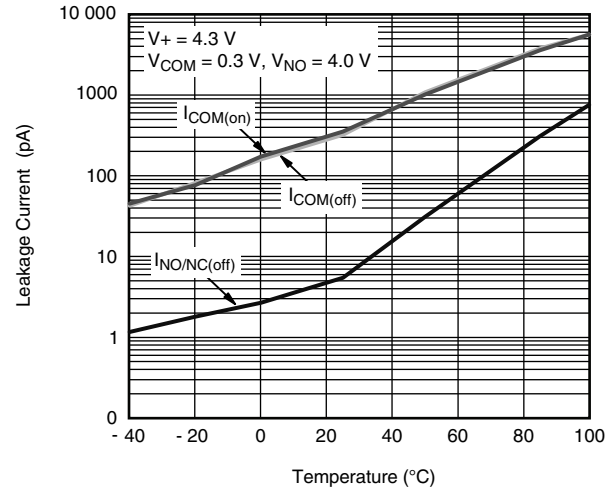
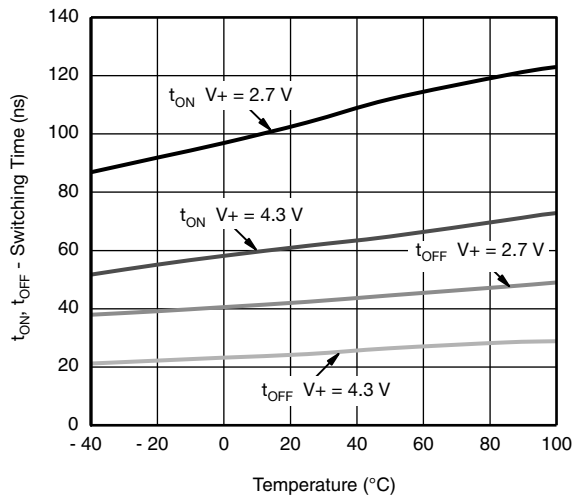
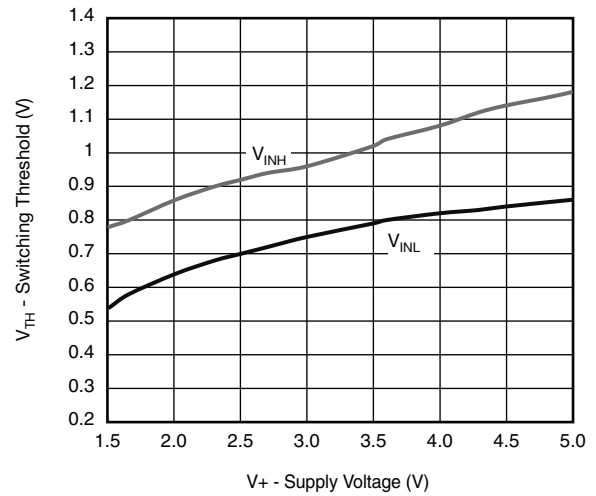
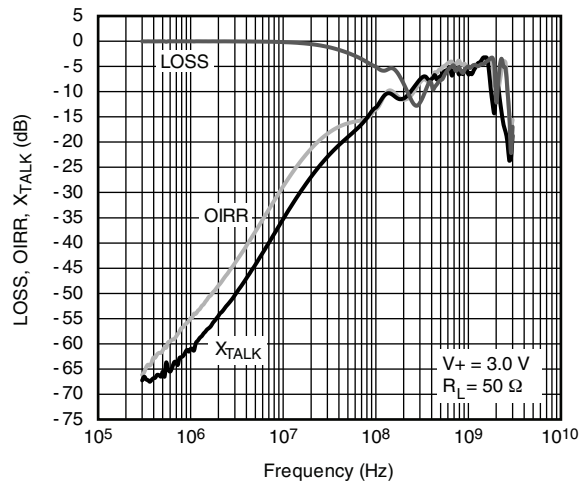
I+ vs. V_{IN}



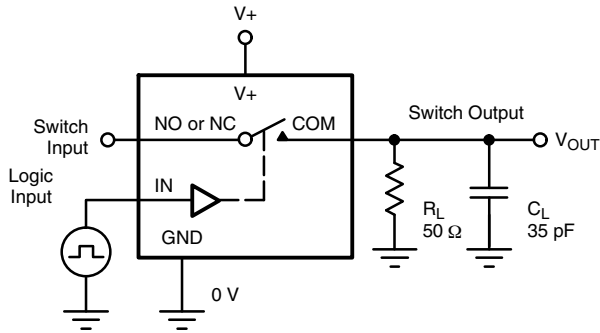
Power Off Leakage I_{OFF} (I_{COM}) vs. Temperature



Leakage vs. Analog Voltage, V+ = 4.3 V

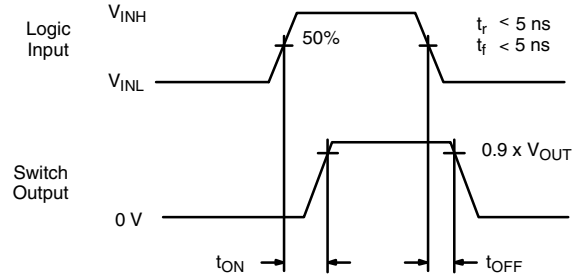
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Leakage Current vs. Temperature

Leakage Current vs. Temperature

 t_{ON}, t_{OFF} Switching Time vs. Temperature

Switching Threshold vs. Supply Voltage

PABK-A Insertion Loss, Off Isolation and Crosstalk

TEST CIRCUITS



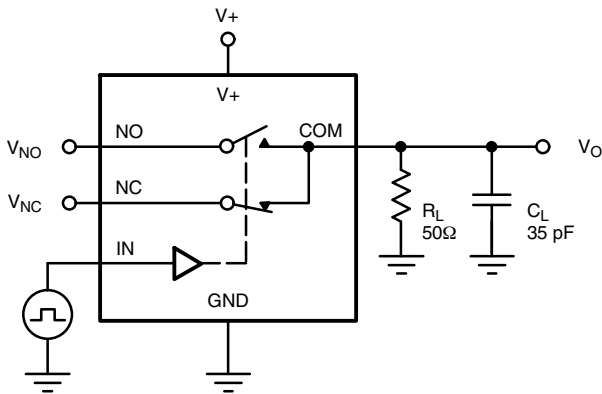
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

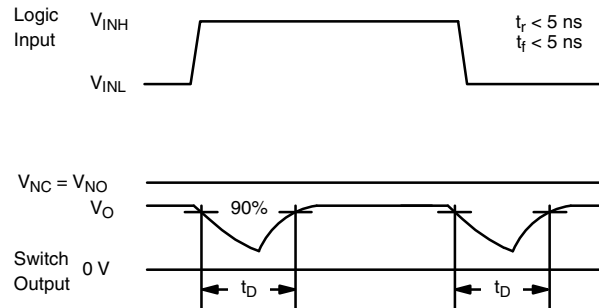
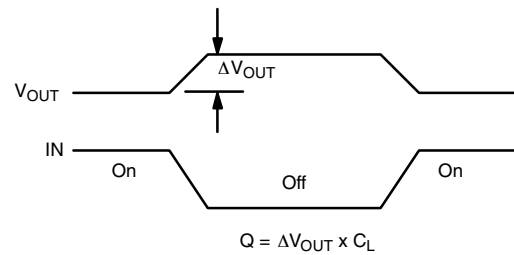
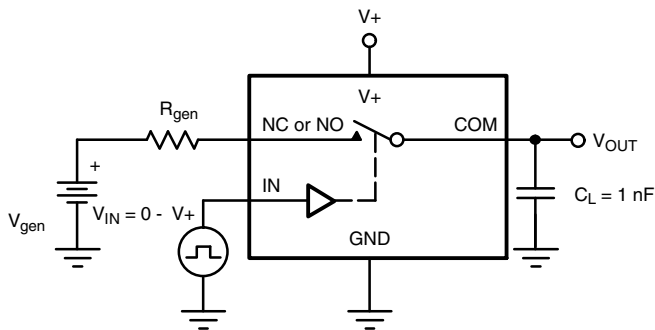
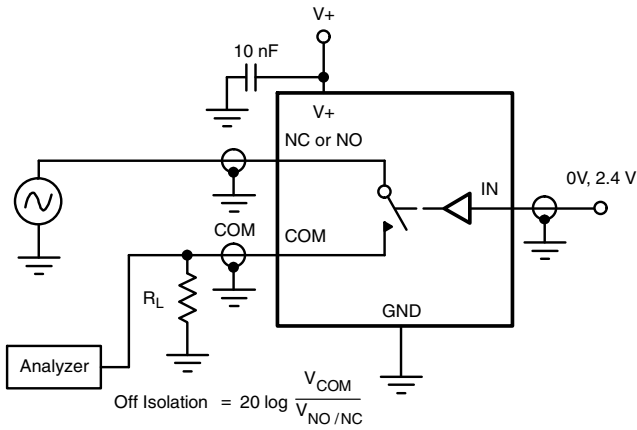
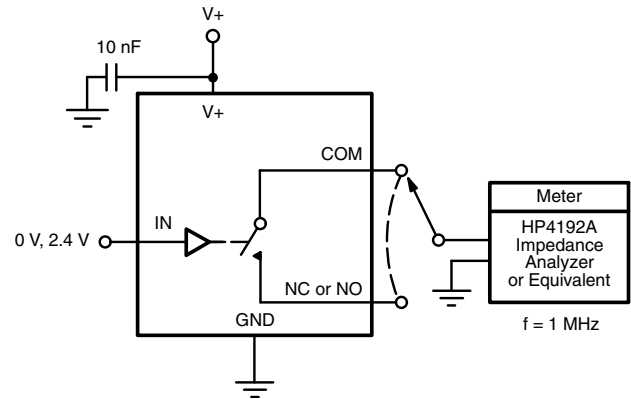


Figure 2. Break-Before-Make Interval



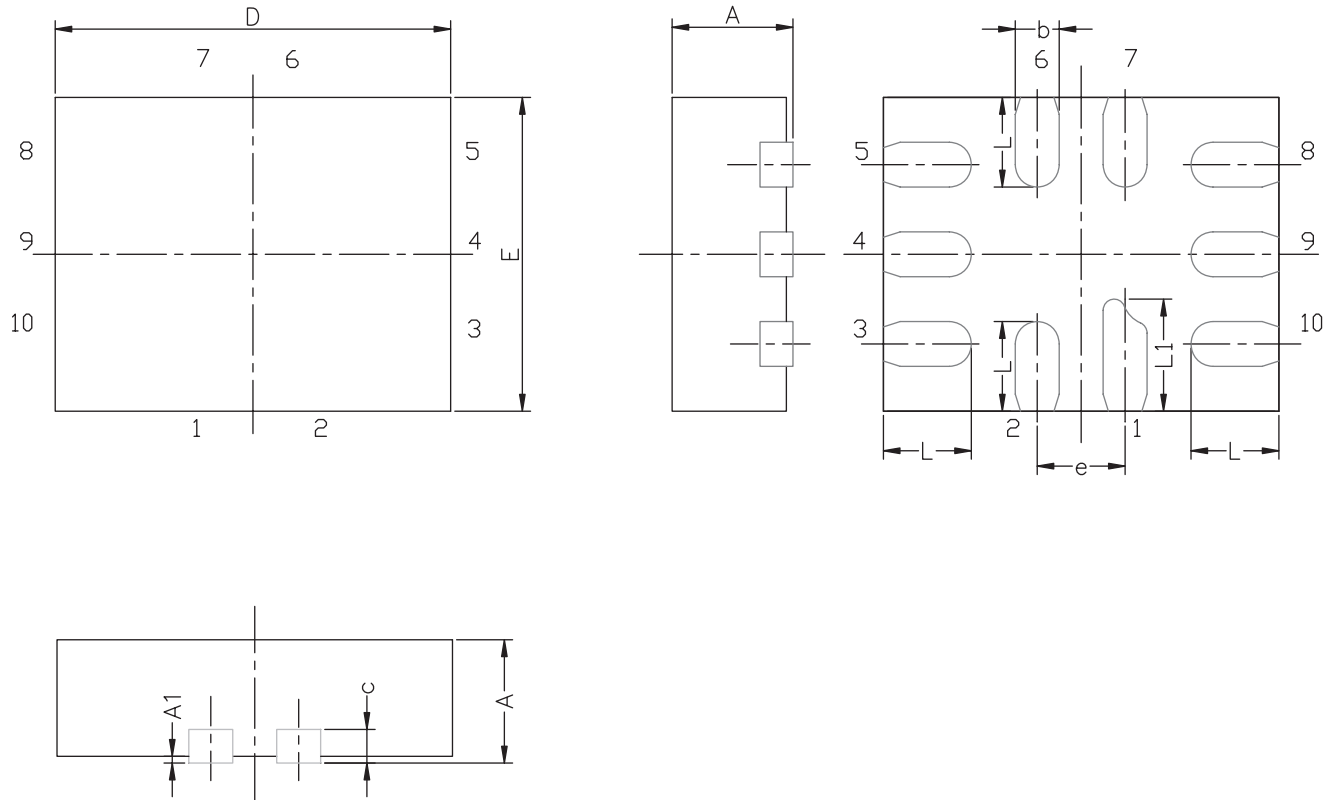
IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

Figure 4. Off-Isolation

Figure 5. Channel Off/On Capacitance

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MINI QFN-10L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.15 REF			0.006 REF		
D	1.75	1.80	1.85	0.069	0.071	0.073
E	1.35	1.40	1.45	0.053	0.055	0.057
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

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DWG: 5957



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