HEF4001B

Quad 2-input NOR gate

Rev. 8 — 13 September 2011 | Product data sheet

1. General description

The HEF4001B is a quad 2-input NOR gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

The device is suitable for use over both the industrial (–40 °C to +85 °C) and automotive (–40 °C to +125 °C) temperature ranges.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the automotive temperature range from –40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

3. Applications

- Automotive and industrial

4. Ordering information

Table 1. Ordering information

All types operate from –40 °C to +125 °C

Type number	Package		
	Name	Description	Version
HEF4001BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
HEF4001BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Functional diagram

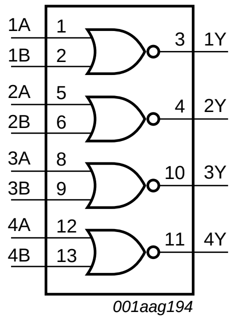


Fig 1. Functional diagram

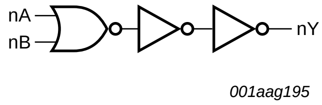


Fig 2. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

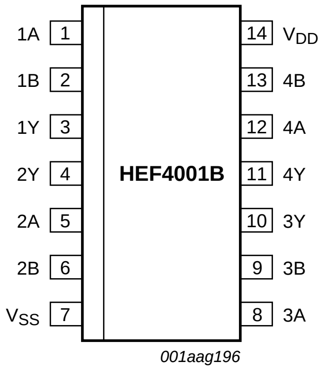


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 5, 8, 12	input
nB	2, 6, 9, 13	input
nY	3, 4, 10, 11	output
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

7. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	V_I < –0.5 V or V_I > V_{DD} + 0.5 V		-	±10	mA
V_I	input voltage			–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < –0.5 V or V_O > V_{DD} + 0.5 V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+125	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to + 125 °C				
		DIP14	[1]	-	750	mW
		SO14	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 12 mW/K.

[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\| < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\| < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\| < 1$ μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\| < 1$ μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–1.7	-	–1.4	-	–1.1	-	–1.1	mA
		V_O = 4.6 V	5 V	-	–0.64	-	–0.5	-	–0.36	-	–0.36	mA
		V_O = 9.5 V	10 V	-	–1.6	-	–1.3	-	–0.9	-	–0.9	mA
		V_O = 13.5 V	15 V	-	–4.2	-	–3.4	-	–2.4	-	–2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance			-	-	-	7.5	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C; for waveforms see Figure 4; for test circuit see Figure 5; unless otherwise specified.

Symbol	Parameter	Extrapolation formula[1]	V_{DD}	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$33 + 0.55 \times C_L$	5 V	-	60	120	ns
		$14 + 0.23 \times C_L$	10 V	-	25	50	ns
		$12 + 0.16 \times C_L$	15 V	-	20	40	ns
t_{PLH}	LOW to HIGH propagation delay	$23 + 0.55 \times C_L$	5 V	-	50	100	ns
		$14 + 0.23 \times C_L$	10 V	-	25	45	ns
		$12 + 0.16 \times C_L$	15 V	-	20	35	ns
t_{THL}	HIGH to LOW output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns
t_{TLH}	LOW to HIGH output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns

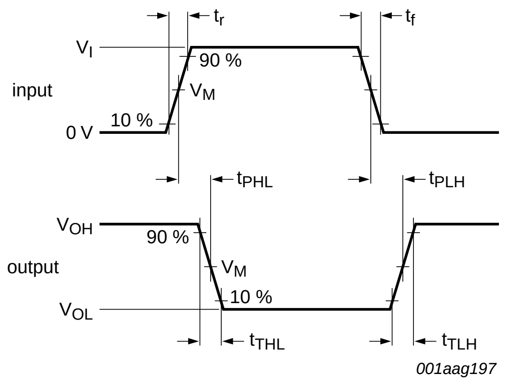
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 1100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (µW)	f_i = input frequency in MHz;
		10 V	$P_D = 5000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (µW)	f_o = output frequency in MHz;
		15 V	$P_D = 14200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (µW)	C_L = output load capacitance in pF;
				$\Sigma(f_o \times C_L)$ = sum of the outputs;
				V_{DD} = supply voltage in V.

12. Waveforms



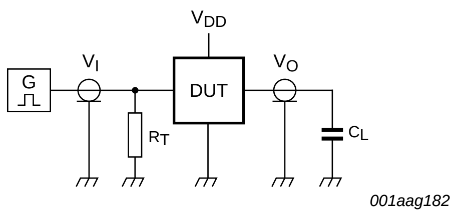
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay, output transition time

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

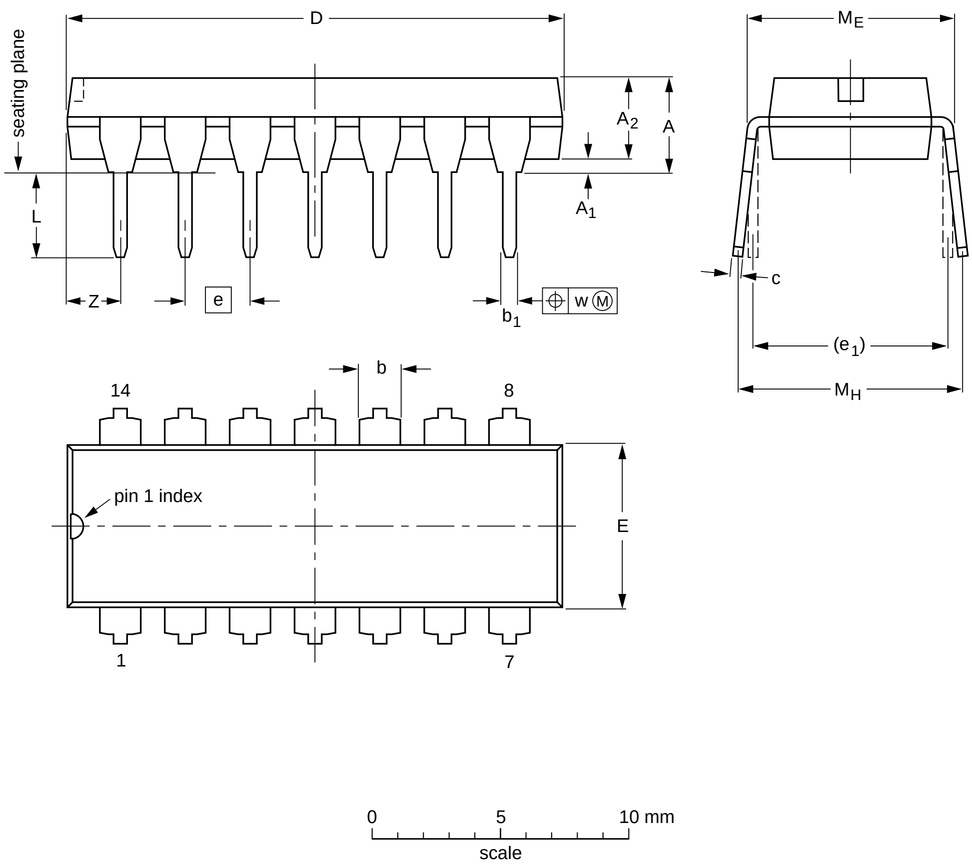
Fig 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

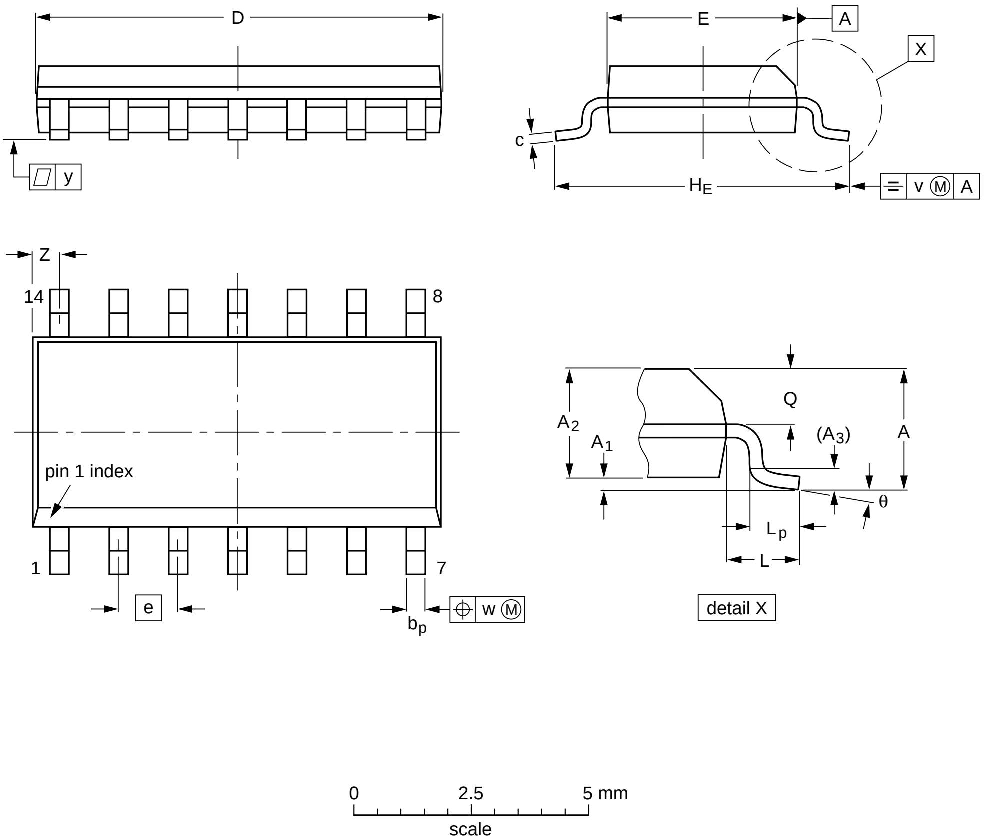
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 6. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT108-1 (SO14)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4001B v.8	20110913	Product data sheet	-	HEF4001B v.7
Modifications:	• Table 3: table note1 removed • Table 6: I_{OH} minimum values changed to maximum			
HEF4001B v.7	20091027	Product data sheet	-	HEF4001B v.6
HEF4001B v.6	20090618	Product data sheet	-	HEF4001B v.5
HEF4001B v.5	20080327	Product data sheet	-	HEF4001B v.4
HEF4001B v.4	20070731	Product data sheet	-	HEF4001B_CNV v.3
HEF4001B_CNV v.3	19950101	Product specification	-	HEF4001B_CNV v.2
HEF4001B_CNV v.2	19950101	Product specification	-	-

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16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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18. Contents

Date of release: 13 September 2011

Document identifier: HEF4001B