

4-BIT SINGLE-CHIP MICROCONTROLLERS

The μ PD750068 is one of the 75XL series 4-bit single-chip microcontrollers and has a data processing capability comparable to that of an 8-bit microcontroller.

The μ PD750068 provides more CPU functions compared to the 75X series and realizes high-speed operation at the low voltage of 1.8 V, making it ideal for battery-driven applications. In addition, this device has on-chip A/D converters, and sophisticated timers capable of operating as a 16-bit timer. The μ PD750068(A) has a higher reliability than the μ PD750068.

A version with on-chip one-time PROM, μ PD75P0076, is also available for the evaluation during system development or for small-scale production.

Detailed descriptions of functions are provided in the following document. Be sure to read the document before designing.

μ PD750068 User's Manual : U10670E

Features

- Low-voltage operation: $V_{DD} = 1.8$ to 5.5 V
- On-chip memory
 - Program memory (ROM):
 - 4096 \times 8 bits (μ PD750064, 750064(A))
 - 6144 \times 8 bits (μ PD750066, 750066(A))
 - 8192 \times 8 bits (μ PD750068, 750068(A))
 - Data memory (RAM):
 - 512 \times 4 bits
- Variable instruction execution time for high-speed operation and power-saved operation
 - 0.95, 1.91, 3.81, 15.3 μ s (@ 4.19 MHz)
 - 0.67, 1.33, 2.67, 10.7 μ s (@ 6.0 MHz)
 - 122 μ s (@ 32.768 kHz)
- Internal low-voltage A/D converters ($AV_{REF} = 1.8$ to 5.5 V)
 - 8-bit resolution \times 8 channels
- Small packages (shrink SOP, shrink DIP)
- Uses instructions of 75X series for easy replacement

Applications

- μ PD750064, 750066, 750068
Cordless phones, audio-visual equipment, home appliances, office machines, fitness machines, meters, gas ranges, etc.
- ★ ○ μ PD750064(A), 750066(A), 750068(A)
Electrical equipment for automobiles
- ★ The μ PD750064, 750066, 750068 and μ PD750064(A), 750066(A), 750068(A) differ only in quality grade. In this manual, the μ PD750068 is described as typical product unless otherwise specified.
Users of other than the μ PD750068 should read the μ PD750068 as referring to the pertinent product.
When the description differs among the μ PD750064, 750066, and 750068, they also refer to the pertinent (A) products.
 μ PD750064 \rightarrow μ PD750064(A), μ PD750066 \rightarrow μ PD750066(A), μ PD750068 \rightarrow μ PD750068(A)

The information in this document is subject to change without notice.

★ **Ordering Information**

Part number	Package	Quality grade
μPD750064CU-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Standard
μPD750064GT-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Standard
μPD750066CU-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Standard
μPD750066GT-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Standard
μPD750068CU-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Standard
μPD750068GT-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Standard
μPD750064CU(A)-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Special
μPD750064GT(A)-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Special
μPD750066CU(A)-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Special
μPD750066GT(A)-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Special
μPD750068CU(A)-xxx	42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)	Special
μPD750068GT(A)-xxx	42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)	Special

Remark xxx is ROM code suffix.

Please refer to “Quality grade on NEC Semiconductor Devices” (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ **Differences between μPD75006x and μPD75006x(A)**

Part number	μPD750064	μPD750064(A)
Item	μPD750066	μPD750066(A)
	μPD750068	μPD750068(A)
Quality grade	Standard	Special

Functional Outline

Parameter		Function	
Instruction execution time		<ul style="list-style-type: none"> • 0.95 μs, 1.91 μs, 3.81 μs, 15.3 μs (@ 4.19 MHz with main system clock) • 0.67 μs, 1.33 μs, 2.67 μs, 10.7 μs (@ 6.0 MHz with main system clock) • 122 μs (@ 32.768 kHz with subsystem clock) 	
★ On-chip memory	ROM	4096 × 8 bits (μ PD750064)	
		6144 × 8 bits (μ PD750066)	
		8192 × 8 bits (μ PD750068)	
	RAM	512 × 4 bits	
General-purpose register		<ul style="list-style-type: none"> • 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks 	
★ Input/output port	CMOS input	12	On-chip pull-up resistors can be specified by software: 7 Also used for analog input pins: 4
	CMOS input/output	12	On-chip pull-up resistors can be specified by software: 12 Also used for analog input pins: 4
	N-ch open-drain input/output pins	8	13 V withstand voltage On-chip pull-up resistors can be specified by mask option
	Total	32	
Timer		4 channels <ul style="list-style-type: none"> • 8-bit timer/event counter: 2 channels (can be used as the 16-bit timer/event counter) • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel 	
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit • 2-wire serial I/O mode 	
A/D converter		8-bit resolution × 8 channels (1.8 V - AVREF - VDD)	
Bit sequential buffer		16 bits	
★ Clock output (PCL)		<ul style="list-style-type: none"> • Φ, 1.05 MHz, 262 kHz, 65.5 kHz (@ 4.19 MHz with main system clock) • Φ, 1.5 MHz, 375 kHz, 93.8 kHz (@ 6.0 MHz with main system clock) 	
★ Buzzer output (BUZ)		<ul style="list-style-type: none"> • 2 kHz, 4 kHz, 32 kHz (@ 4.19 MHz with main system clock or @ 32.768 kHz with subsystem clock) • 2.93 kHz, 5.86 kHz, 46.9 kHz (@ 6.0 MHz with main system clock) 	
Vectored interrupt		External: 3, Internal: 4	
Test input		External: 1, Internal: 1	
System clock oscillator		<ul style="list-style-type: none"> • Ceramic or crystal oscillator for main system clock oscillation • Crystal oscillator for subsystem clock oscillation 	
Standby function		STOP/HALT mode	
Operating ambient temperature		T _A = -40 to +85 °C	
Power supply voltage		V _{DD} = 1.8 to 5.5 V	
Package		<ul style="list-style-type: none"> • 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch) • 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch) 	

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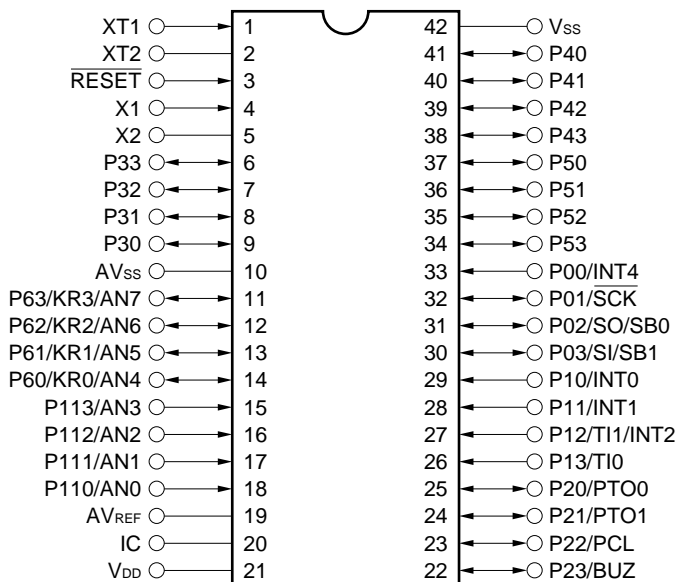
1. PIN CONFIGURATION (Top View)

★ • 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)

μ PD750064CU-xxx, μ PD750064CU(A)-xxx
 μ PD750066CU-xxx, μ PD750066CU(A)-xxx
 μ PD750068CU-xxx, μ PD750068CU(A)-xxx

★ • 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)

μ PD750064GT-xxx, μ PD750064GT(A)-xxx
 μ PD750066GT-xxx, μ PD750066GT(A)-xxx
 μ PD750068GT-xxx, μ PD750068GT(A)-xxx

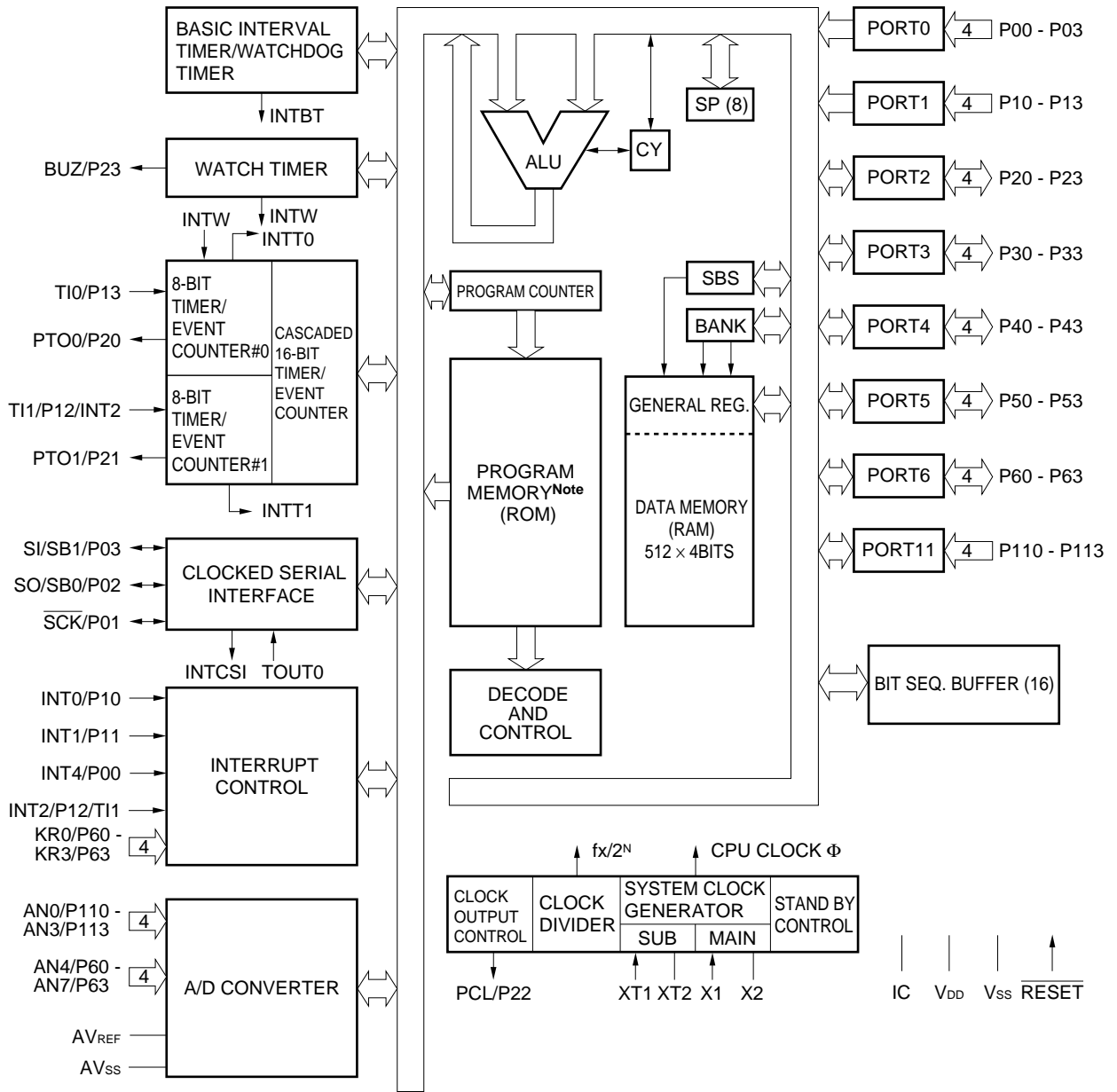


IC: Internally Connected (Connect pin directly to V_{DD}).

Pin Identification

AN0-AN7	: Analog Input 0-7	P60-P63	: Port 6
AV _{REF}	: Analog Reference	P110-P113	: Port 11
AV _{SS}	: Analog Ground	PCL	: Programmable Clock
BUZ	: Buzzer Clock	PTO0, PTO1	: Programmable Timer Output 0, 1
IC	: Internally Connected	RESET	: Reset Input
INT0, INT1, INT4	: External Vectored Interrupt 0, 1, 4	SB0, SB1	: Serial Data Bus 0, 1
INT2	: External Test Input 2	SCK	: Serial Clock
KR0-KR3	: Key Return 0-3	SI	: Serial Input
P00-P03	: Port 0	SO	: Serial Output
P10-P13	: Port 1	TI0, TI1	: Timer Input 0, 1
P20-P23	: Port 2	V _{DD}	: Positive Power Supply
P30-P33	: Port 3	V _{SS}	: Ground
P40-P43	: Port 4	X1, X2	: Main System Clock Oscillation 1, 2
P50-P53	: Port 5	XT1, XT2	: Subsystem Clock Oscillation 1, 2

2. BLOCK DIAGRAM



Note Capacity of the ROM depends on the product.

3. PIN FUNCTION

3.1 Port Pins (1/2)

Pin Name	Input/Output	Dual function pin	Description	8-bit I/O	After Reset	I/O Circuit TYPE ^{Note 1}
P00	Input	INT4	4-bit input port (PORT0). For P01 to P03, connection of on-chip pull-up resistors can be specified by software in 3-bit units.	No	Input	
P01	Input/Output	$\overline{\text{SCK}}$				<F>-A
P02	Input/Output	SO/SB0				<F>-B
P03	Input/Output	SI/SB1				<M>-C
P10	Input	INT0	4-bit input port (PORT1). Connection of on-chip pull-up resistors can be specified by software in 4-bit units. P10/INT0 can select noise elimination circuit.	No	Input	-C
P11		INT1				
P12		T11/INT2				
P13		T10				
P20	Input/Output	PTO0	4-bit input/output port (PORT2). Connection of on-chip pull-up resistors can be specified by software in 4-bit units.	No	Input	E-B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30-P33	Input/Output	–	Programmable 4-bit input/output port (PORT3). This port can be specified for input/output bit-wise. Connection of on-chip pull-up resistor can be specified by software in 4-bit units.	No	Input	E-B
★ P40-P43 ^{Note 2}	Input/Output	–	N-ch open-drain 4-bit input/output port (PORT4). A pull-up resistor can be contained bit-wise (mask option). Withstand voltage is 13 V in open-drain mode.	Yes	High level (when pull-up resistors are provided) or high-impedance	M-D
★ P50-P53 ^{Note 2}	Input/Output	–	N-ch open-drain 4-bit input/output port (PORT5). A pull-up resistor can be contained bit-wise (mask option). Withstand voltage is 13 V in open-drain mode.		High level (when pull-up resistors are provided) or high-impedance	M-D

Notes 1. Circuit types enclosed in brackets indicate the Schmitt trigger input.

2. If on-chip pull-up resistors are not specified by mask option (when used as N-ch open-drain input port), low level input leakage current increases when input or bit manipulation instruction is executed.

3.1 Port Pins (2/2)

Pin Name	Input/Output	Dual function pin	Description	8-bit I/O	After Reset	I/O Circuit TYPE ^{Note}
P60	Input/Output	KR0/AN4	Programmable 4-bit input/output port (PORT6). This port can be specified for input/output bit-wise. Connection of on-chip pull-up resistors can be specified by software in 4-bit units.	No	Input	<Y>-D
P61		KR1/AN5				
P62		KR2/AN6				
P63		KR3/AN7				
P110	Input	AN0	4-bit input port (PORT11).	No	Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Note Circuit types enclosed in brackets indicate the Schmitt trigger input.

3.2 Non-port Pins (1/2)

Pin Name	Input/Output	Dual function pin	Description		After Reset	I/O Circuit TYPE ^{Note}
T10	Input	P13	Inputs external event pulses to the timer/event counter.		Input	-C
T11		P12/INT2				
PTO0	Output	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PCL		P22	Clock output			
BUZ		P23	Optional frequency output (for buzzer output or system clock trimming)			
SCK	Input/Output	P01	Serial clock input/output		Input	<F>-A
SO	Output	P02	Serial data output			<F>-B
SB0	Input/Output		Serial data bus input/output			
SI	Input	P03	Serial data input			<M>-C
SB1	Input/Output		Serial data bus input/output			
INT4	Input	P00	Edge detection vectored interrupt input (both rising edge and falling edge detection)		Input	
INT0	Input	P10	Edge detection vectored interrupt input (detection edge can be selected).	Noise elimination circuit/asynchronous selection	Input	-C
INT1		P11	INT0/P10 can select noise elimination circuit.	Asynchronous		
INT2	Input	P12/T11	Rising edge detection testable input	Asynchronous	Input	-C
KR0-KR3	Input	P60/AN4-P63/AN7	Falling edge detection testable input		Input	<Y>-D
AN0-AN3	Input	P110-P113	Analog signal input		Input	Y-A
AN4-AN7		P60/KR0-P63/KR3				<Y>-D
AV _{REF}	-	-	A/D converter reference voltage		-	Z-N
AV _{SS}	-	-	A/D converter reference GND potential		-	Z-N

Note Circuit types enclosed in brackets indicate the Schmitt trigger input.

3.2 Non-port Pins (2/2)

Pin Name	Input/Output	Dual function pin	Description	After Reset	I/O Circuit TYPE ^{Note}
X1	Input	-	Crystal/ceramic connection pin for the main system clock oscillation. When inputting the external clock, input the external clock to pin X1, and the inverted phase of the external clock to pin X2.	-	-
X2	-				
XT1	Input	-	Crystal connection pin for the subsystem clock oscillation. When the external clock is used, input the external clock to pin XT1, and the inverted phase of the external clock to pin XT2. Pin XT1 can be used as a 1-bit input (test) pin.	-	-
XT2	-				
$\overline{\text{RESET}}$	Input	-	System reset input (low-level active)	-	
IC	-	-	Internally connected. Connect directly to V_{DD} .	-	-
V_{DD}	-	-	Positive power supply	-	-
V_{SS}	-	-	Ground potential	-	-

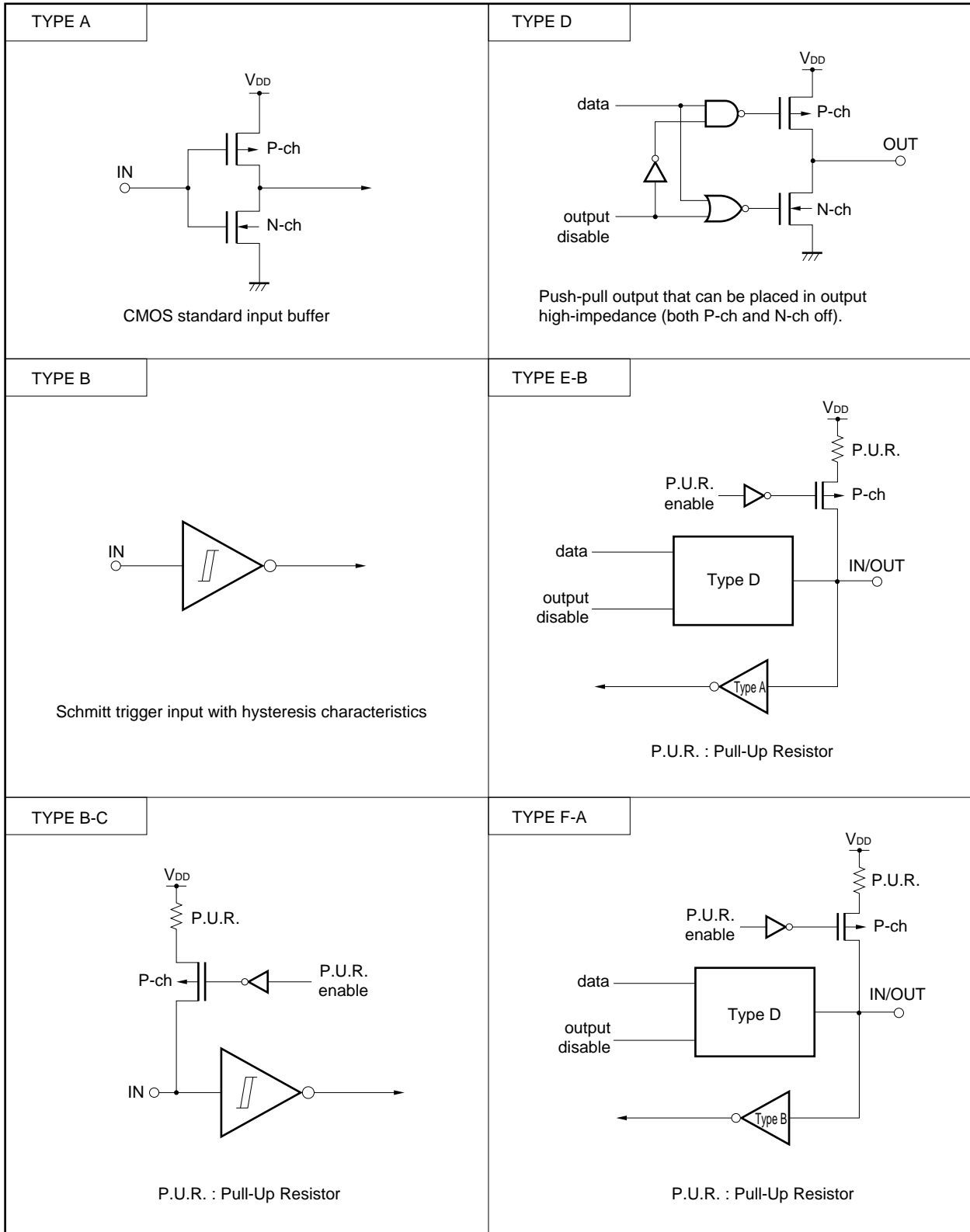
★

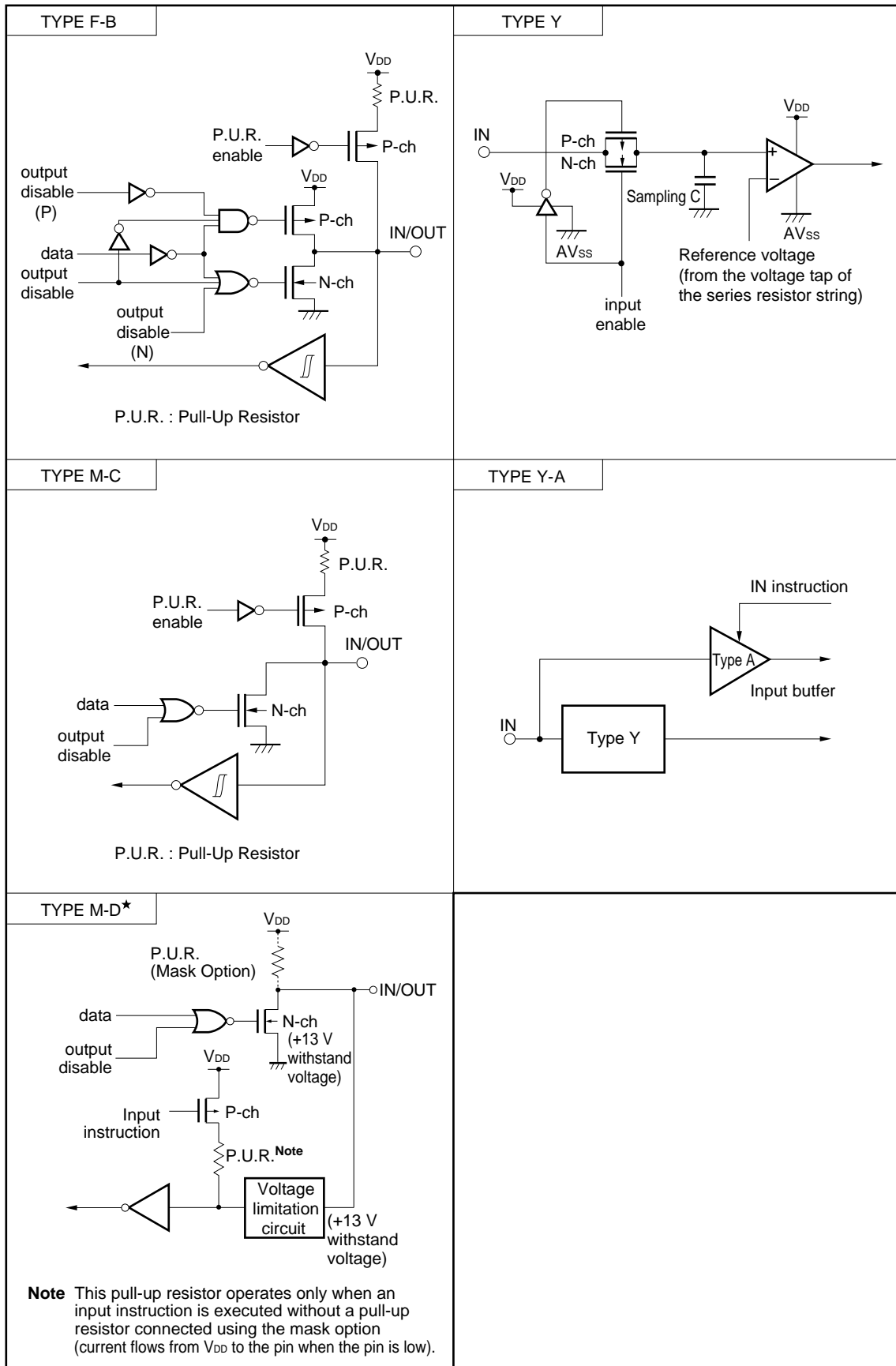
Note Circuit types enclosed in brackets indicate the Schmitt trigger input.

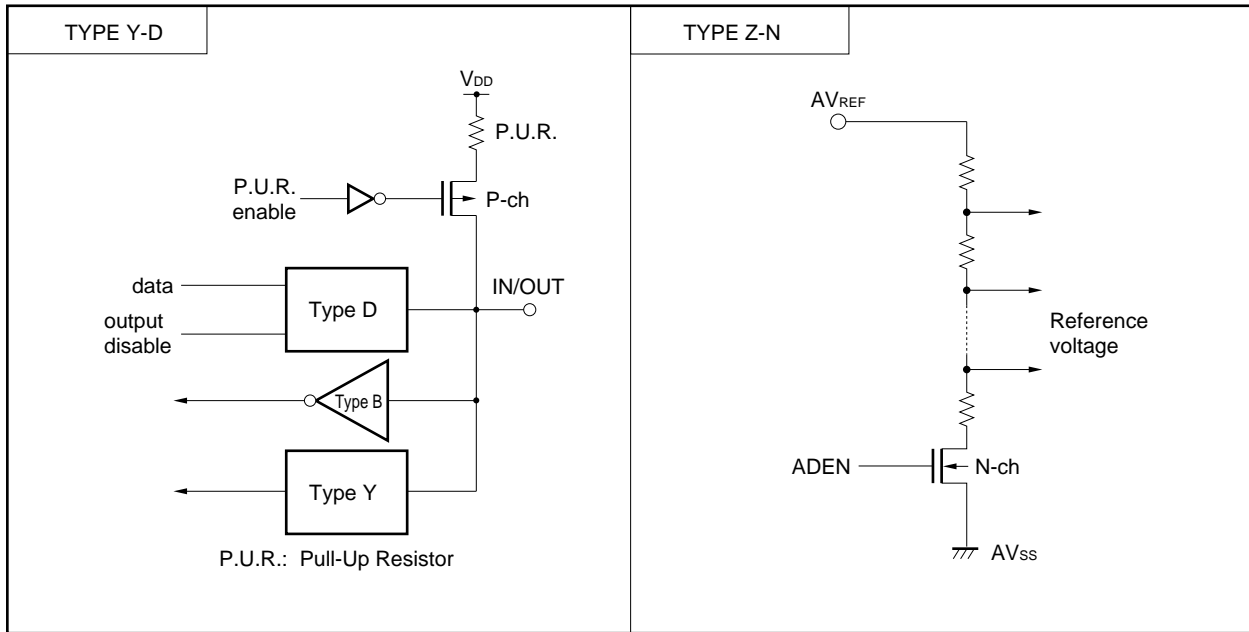
3.3 Pin Input/Output Circuits

The μ PD750068 pin input/output circuits are shown schematically.

(1/3)







★ 3.4 Recommended Connections for Unused Pins

Table 3-1. List of Recommended Connections for Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to V _{SS} or V _{DD}
P01/SCK	Connect to V _{SS} or V _{DD} via a resistor individually
P02/SO/SB0	
P03/SI/SB1	Connect to V _{SS}
P10/INT0, P11/INT1	Connect to V _{SS} or V _{DD}
P12/TI1/INT2	
P13/TI0	
P20/PTO0	Input state: Connect to V _{SS} or V _{DD} via a resistor individually Output state: Open
P21/PTO1	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	Connect to V _{SS} (do not connect a pull-up resistor of mask option)
P50-P53	
P60/KR0/AN4-P63/KR3/AN7	Input state: Connect to V _{SS} or V _{DD} via a resistor individually Output state: Open
P110/AN0-P113/AN3	Connect to V _{SS} or V _{DD} directly
XT1 ^{Note}	Connect to V _{SS} or V _{DD}
XT2 ^{Note}	Open
IC	Connect to V _{DD} directly
AV _{REF}	Connect to V _{SS}
AV _{SS}	

Note When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the internal feedback resistor).

4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

4.1 Differences between Mk I Mode and Mk II Mode

The CPU of the μ PD750068 has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by the bit 3 of the stack bank select register (SBS).

- Mk I mode: Upward compatible with μ PD75068. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with μ PD75068. Can be used in all the 75XL CPUs including those products whose ROM capacity is more than 16 Kbytes.

Table 4-1. Differences between Mk I Mode and Mk II Mode

	Mk I mode	Mk II mode
Number of stack bytes for subroutine instructions	2 bytes	3 bytes
BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

★ **Caution** The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL series. Therefore, this mode is effective for enhancing software compatibility with products exceeding 16 Kbytes.

When the Mk II mode is selected, the number of stack bytes used during execution of subroutine call instructions increases by one byte per stack compared to the Mk I mode. When the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by one machine cycle. Therefore, use the Mk I mode if the RAM efficiency and processing performance are more important than software compatibility.

4.2 Setting Method of Stack Bank Select Register (SBS)

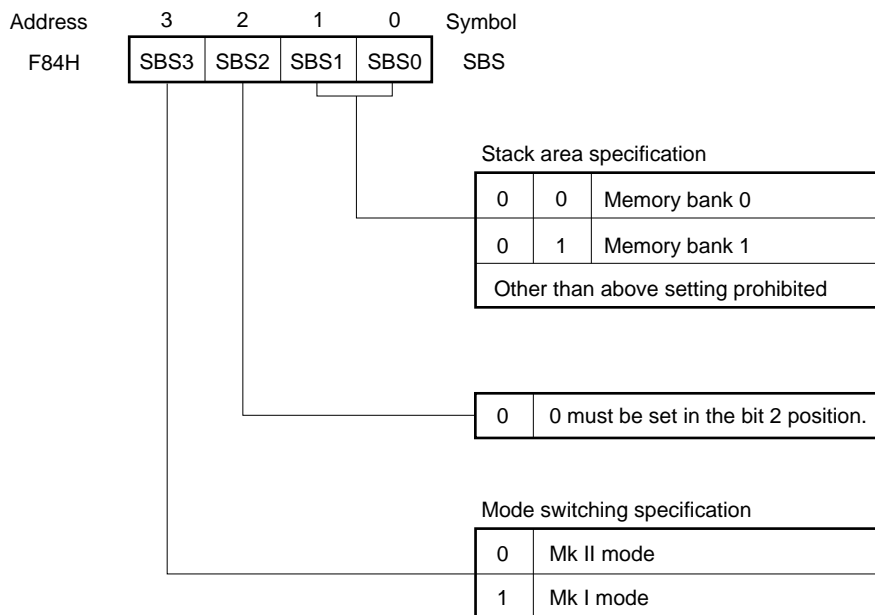
Switching between the Mk I mode and Mk II mode can be done by the stack bank select register (SBS). Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 100xB^{Note} at the beginning of a program. When using the Mk II mode, it must be initialized to 000xB^{Note}.

Note Set the desired value in the × position.

Figure 4-1. Stack Bank Select Register Format



Caution Since SBS. 3 is set to “1” after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to “0” to select the Mk II mode.

5. MEMORY CONFIGURATION

- Program memory (ROM) 4096 × 8 bits (μ PD750064)

- ★ 6144 × 8 bits (μ PD750066)
- 8192 × 8 bits (μ PD750068)

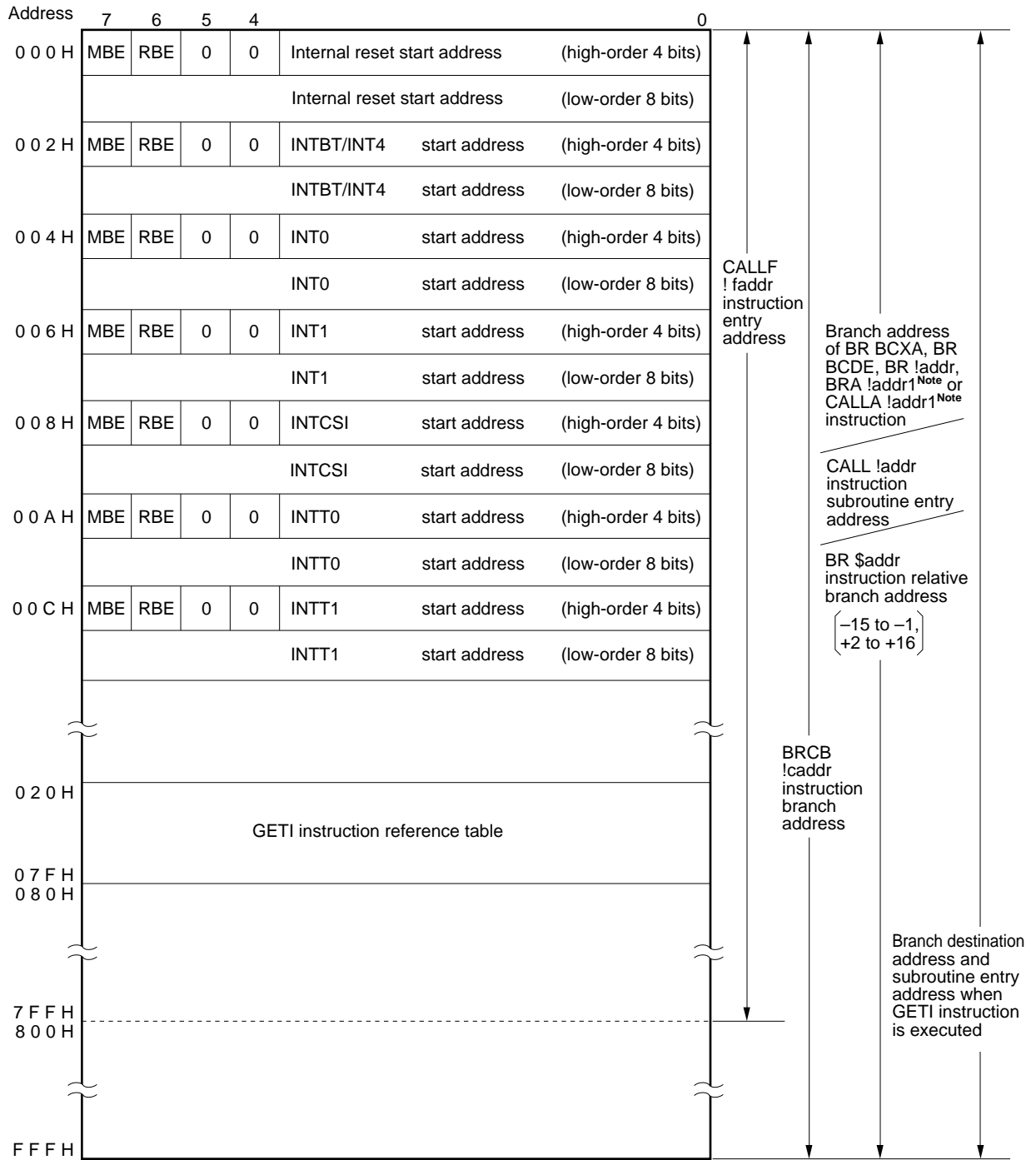
- Addresses 0000H and 0001H
Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset start is possible from any address.
- Addresses 0002H to 000DH
Vector table wherein the program start address and the values set for the RBE and MBE by each vectored interrupt are written. Interrupt processing can start from any address.
- Addresses 0020H to 007FH
Table area referenced by the GETI instruction^{Note}.

Note The GETI instruction realizes a 1-byte instruction on behalf of any 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the number of program steps.

- Data memory (RAM)

- Data area 512 words × 4 bits (000H to 1FFH)
- Peripheral hardware area 128 words × 4 bits (F80H to FFFH)

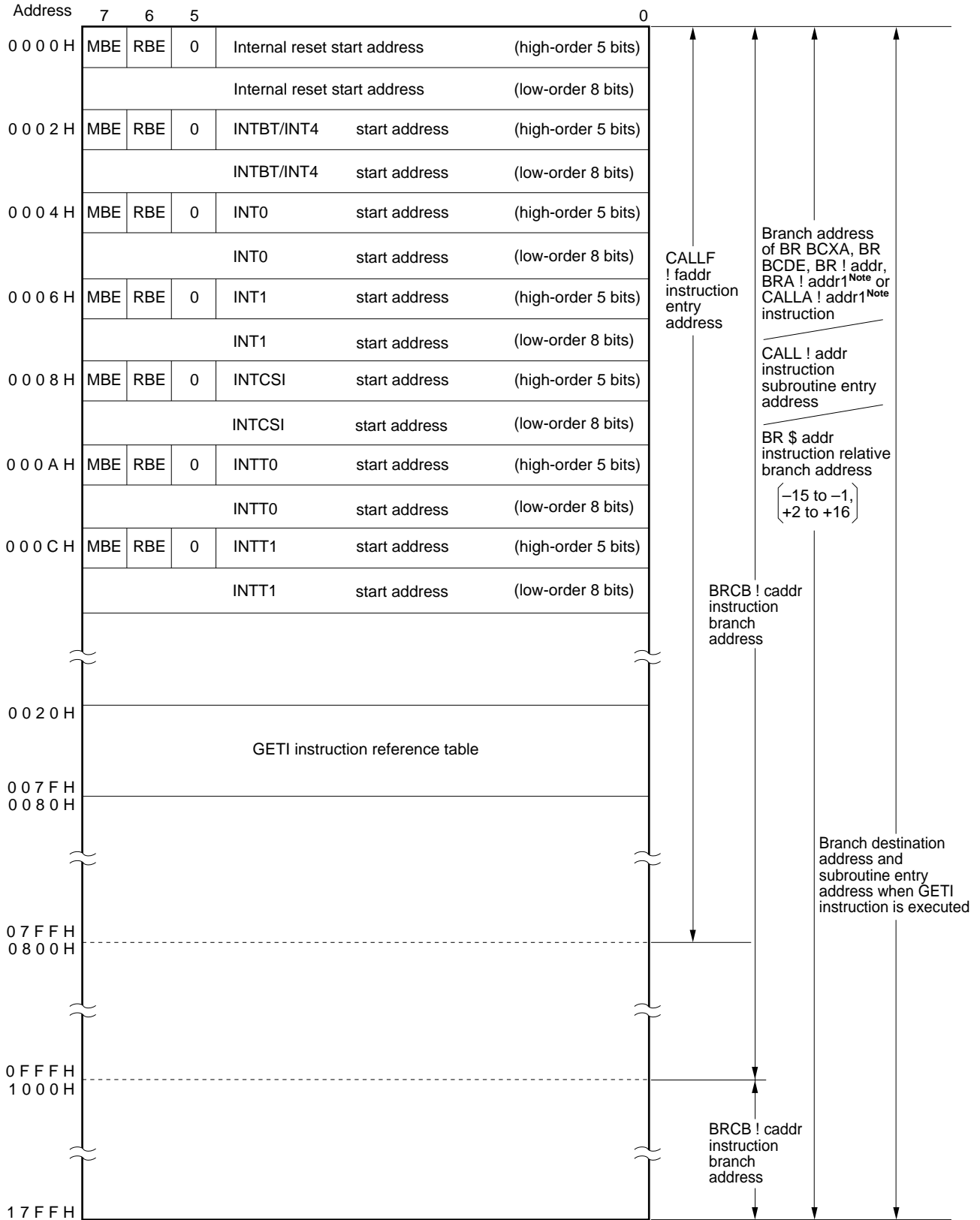
Figure 5-1. Program Memory Map (μ PD750064)



★ **Note** Can be used only in the Mk II mode.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

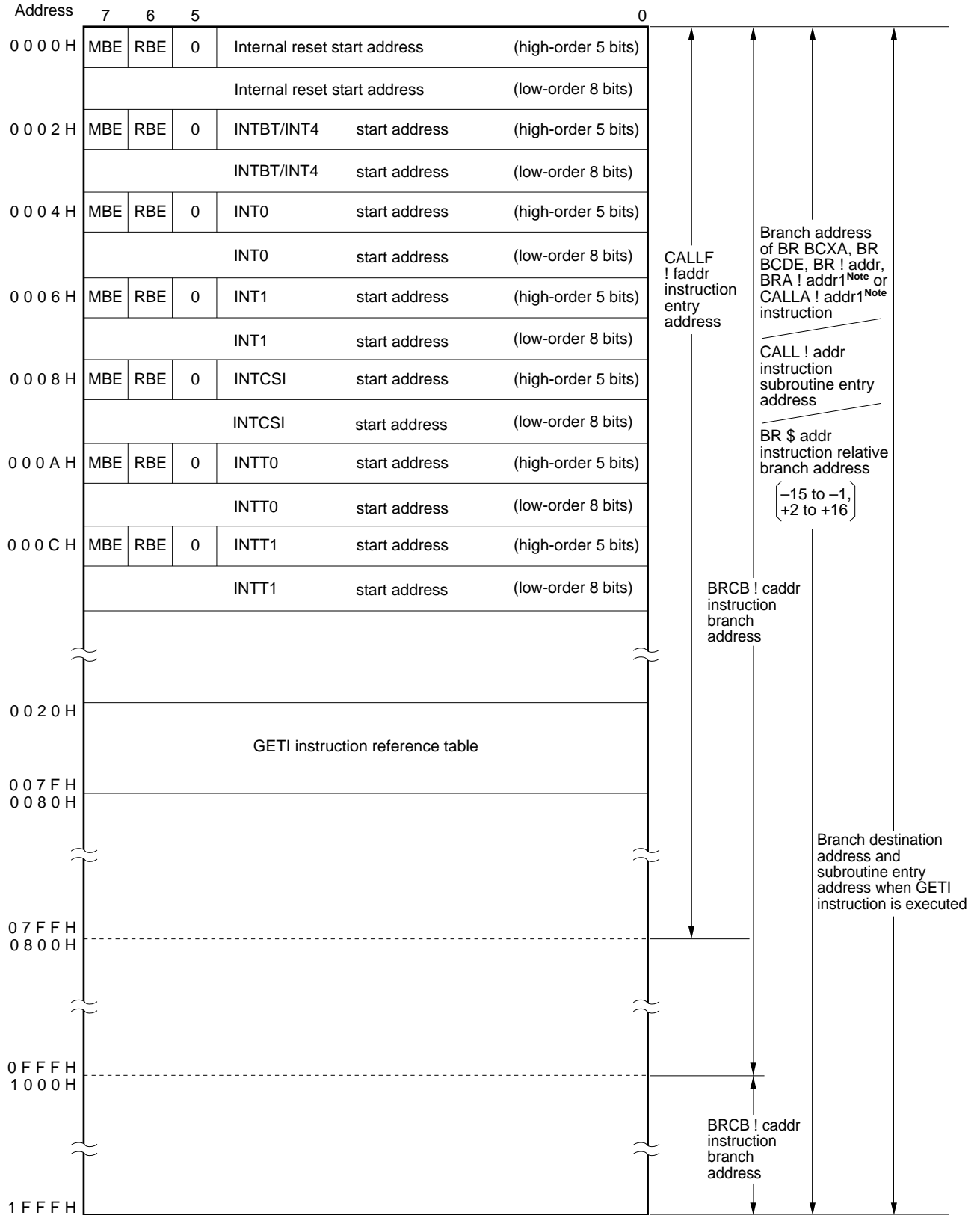
★ Figure 5-2. Program Memory Map (μ PD750066)



Note Can be used only in the Mk II mode.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

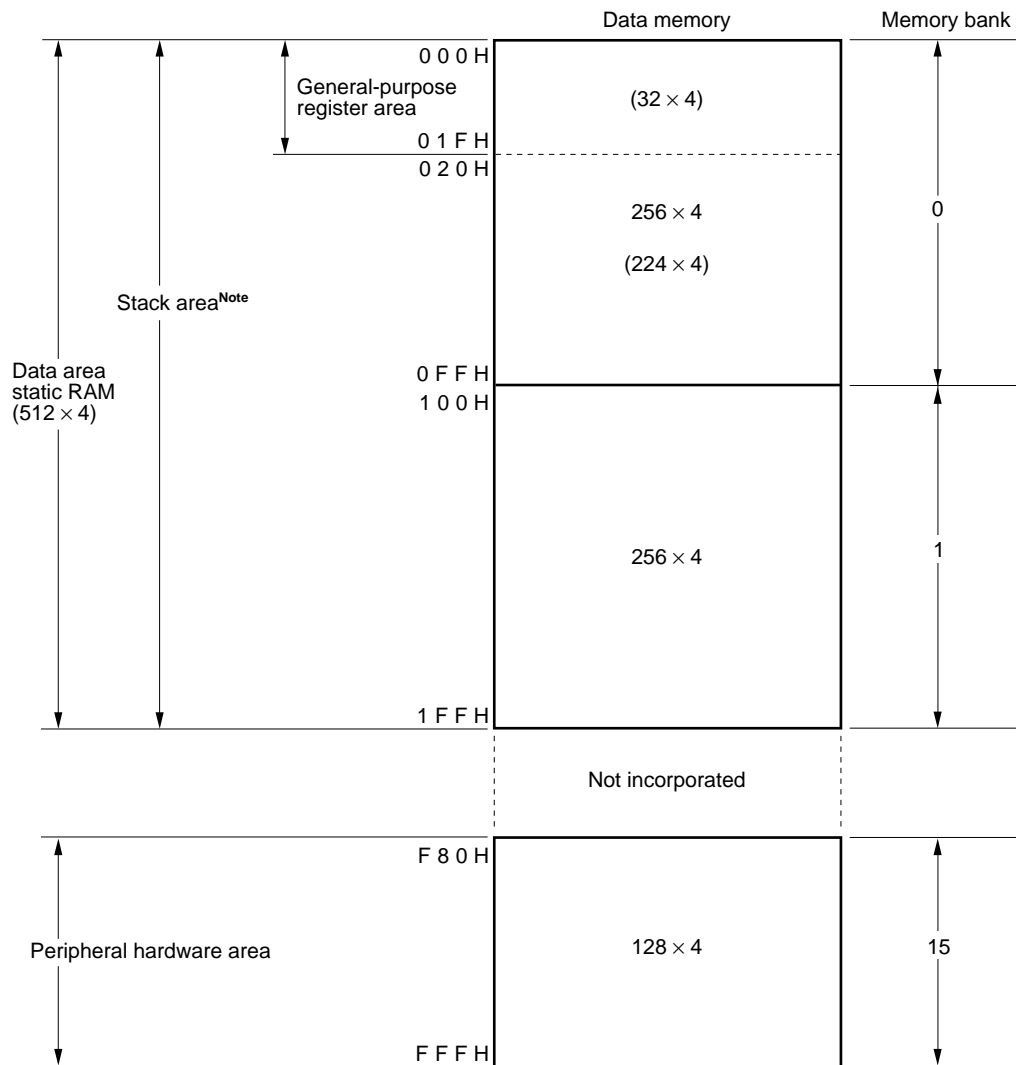
Figure 5-3. Program Memory Map (μ PD750068)



★ **Note** Can be used only in the Mk II mode.

Remark In addition to the above, a branch can be taken to the address indicated by changing only the low-order eight bits of PC by executing the BR PCDE or BR PCXA instruction.

Figure 5-4. Data Memory Map



★ **Note** Memory bank 0 or 1 can be selected as the stack area.

6. PERIPHERAL HARDWARE FUNCTION

6.1 Port

There are three types of I/O ports as follows.

• CMOS input (PORT0, 1, 11)	: 12
• CMOS input/output (PORT2, 3, 6)	: 12
• N-ch open drain input/output (PORT4, 5)	: 8
Total	32

Table 6-1. Types and Features of Digital Ports

Port name	Function	Operation and features		Remarks
PORT0	4-bit input	When the serial interface function is used, the dual function pins function as output ports depending on the operation mode.		Also used for the INT4, \overline{SCK} , SO/SB0, SI/SB1 pins.
PORT1		4-bit input only port.		Also used for the INT0-INT2/TI1, TI0 pins.
PORT2	4-bit input/output	Can be set to input mode or output mode in 4-bit units.		Also used for the PTO0, PTO1, PCL, BUZ pins.
PORT3		Can be set to input mode or output mode bit-wise.		
PORT4	4-bit input/output (N-ch open drain, 13 V withstand voltage)	Can be set to input mode or output mode in 4-bit units. On-chip pull-up resistor can be specified bit-wise by mask option.	Ports 4 and 5 are paired and data can be input/output in 8-bit units.	-
PORT5				
PORT6	4-bit input/output	Can be set to input mode or output mode bit-wise.		Also used for the KR0-KR3, AN4-AN7 pins.
PORT11	4-bit input	4-bit input only port.		Also used for the AN0-AN3 pins.

★

6.2 Clock Generator

The clock generator generates clocks which are supplied to the peripheral hardware in the CPU. Figure 6-1 shows the configuration of the clock generator.

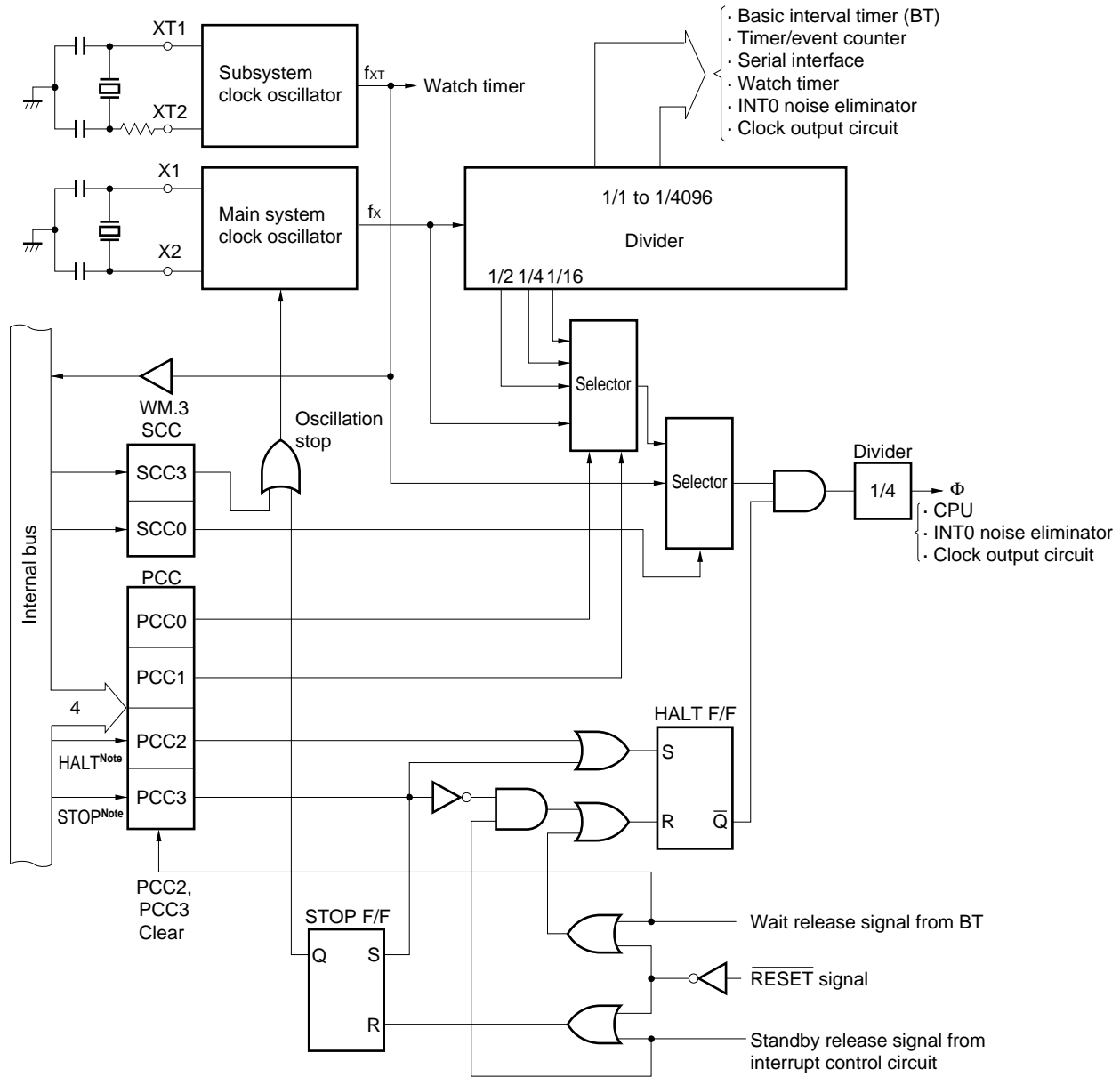
Operation of the clock generator is determined by the processor clock control register (PCC) and system clock control register (SCC).

Two types of system clocks are available; main system clock and subsystem clock.

The instruction execution time can also be changed.

- 0.95 μ s, 1.91 μ s, 3.81 μ s, 15.3 μ s (@ 4.19 MHz with main system clock)
- 0.67 μ s, 1.33 μ s, 2.67 μ s, 10.7 μ s (@ 6.0 MHz with main system clock)
- 122 μ s (@ 32.768 kHz with subsystem clock)

Figure 6-1. Clock Generator Block Diagram



Note Instruction execution

- Remarks 1.** f_x = Main system clock frequency
 2. f_{XT} = Subsystem clock frequency
 3. Φ = CPU clock
 4. PCC: Processor Clock Control Register
 5. SCC: System Clock Control Register
 6. One clock cycle (t_{CY}) of the CPU clock is equal to one machine cycle of the instruction.

6.3 Subsystem Clock Oscillator Control Function

The subsystem clock oscillator of the μ PD750068 has the following two control functions to decrease the supply current.

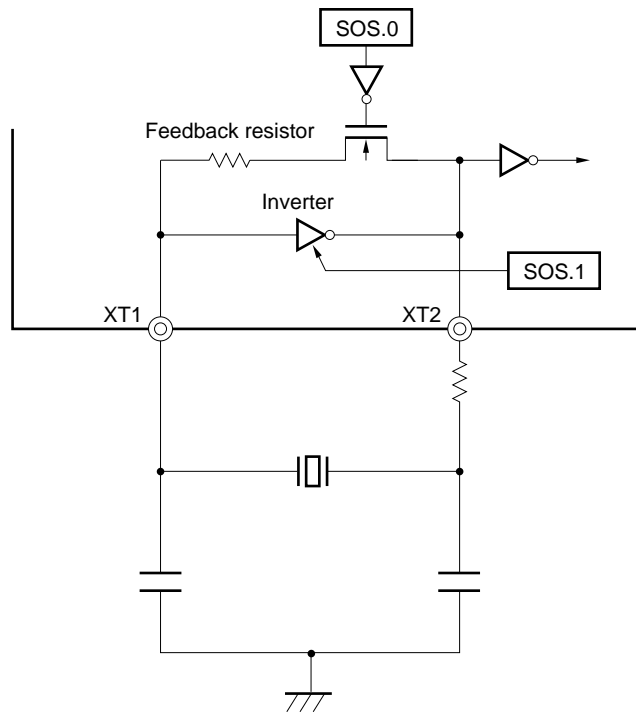
- Selects by software whether an internal feedback resistor is to be used or not^{Note}.
- Reduces current consumption by decreasing the drive current of the on-chip inverter when the supply voltage is high ($V_{DD} \cdot 2.7$ V).

Note When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the internal feedback resistor) by software, connect XT1 to V_{SS} or V_{DD} , and open XT2. This makes it possible to reduce the current consumption in the subsystem clock oscillator.

The above functions can be used by switching the bits 0 and 1 of the sub-oscillator control register (SOS). (Refer to Figure 6-2.)

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Figure 6-2. Subsystem Clock Oscillator



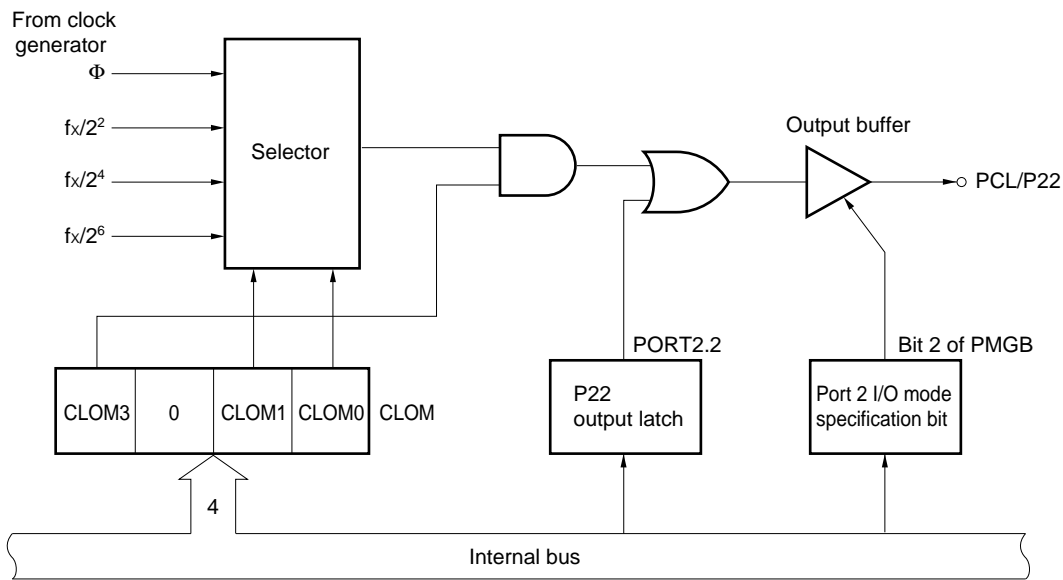
6.4 Clock Output Circuit

The clock output circuit is provided to output the clock pulses from the P22/PCL pin to the remote control wave outputs and peripheral LSIs.

- Clock output (PCL) : Φ , 1.05 MHz, 262 kHz, 65.5 kHz (at 4.19 MHz)
 : Φ , 1.5 MHz, 375 kHz, 93.8 kHz (at 6.0 MHz)

★

Figure 6-3. Clock Output Circuit Block Diagram



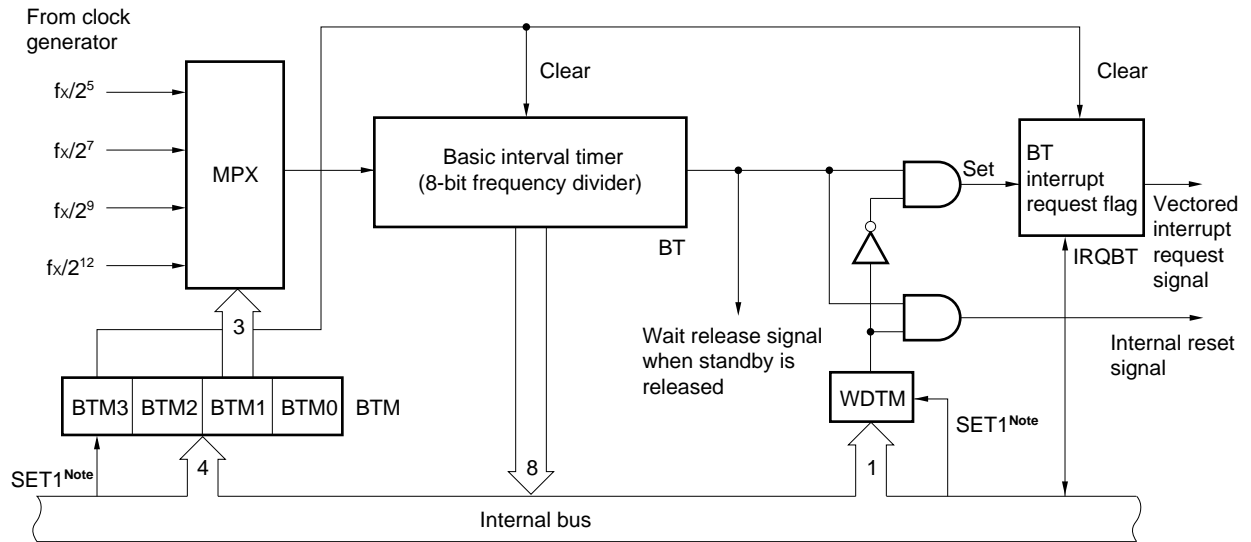
Remark Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

6.5 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- (a) Interval timer operation to generate a reference time interrupt
- (b) Watchdog timer operation to detect a runaway of program and reset the CPU
- (c) Selects and counts the wait time when the standby mode is released
- (d) Reads the contents of counting

Figure 6-4. Basic Interval Timer/Watchdog Timer Block Diagram



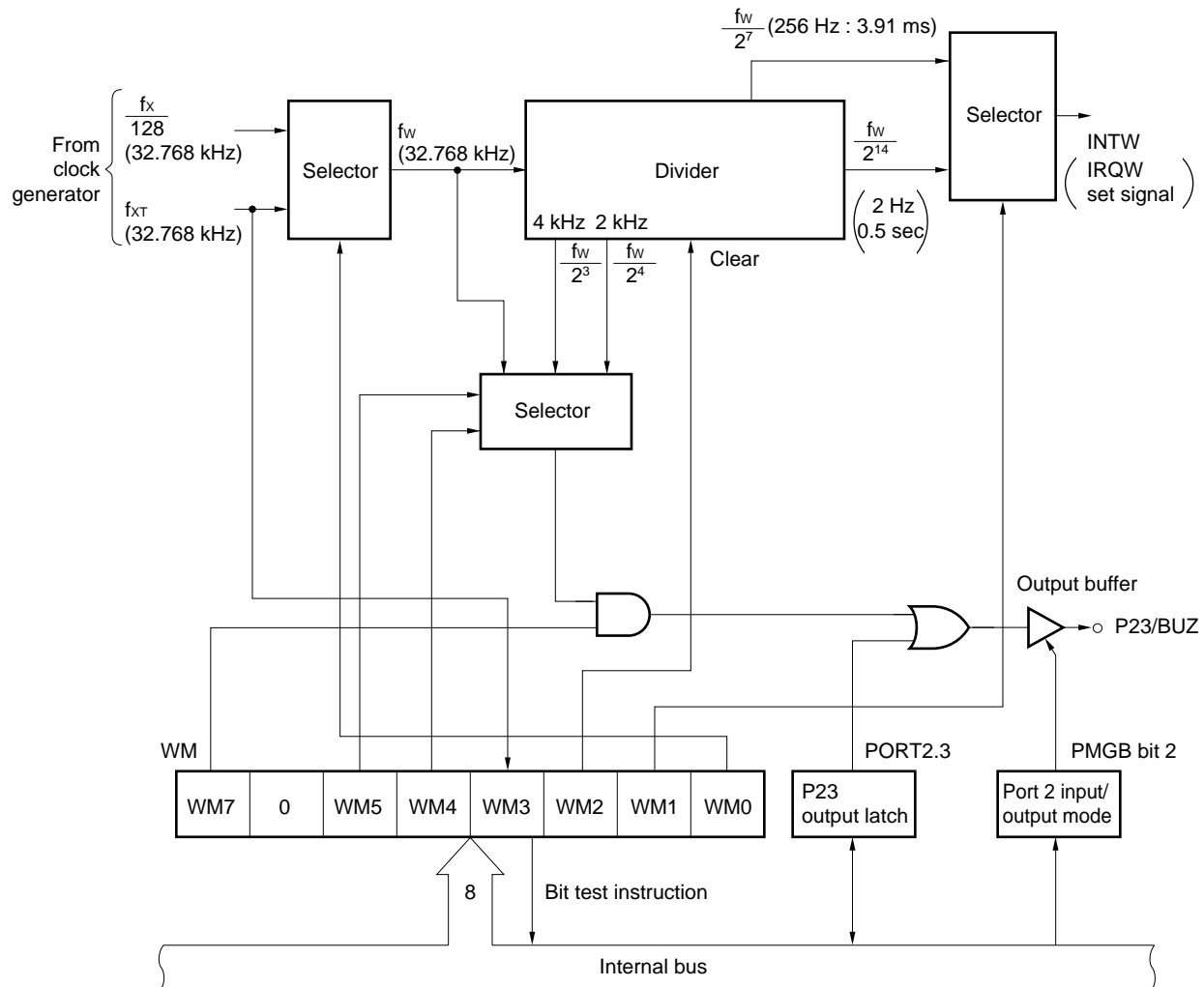
Note Instruction execution

6.6 Watch Timer

The μ PD750068 has one channel of watch timer. The watch timer has the following functions.

- (a) Sets the test flag (IRQW) with 0.5 sec interval. The standby mode can be released by the IRQW.
- (b) 0.5 sec interval can be created by both the main system clock (4.194304 MHz) and subsystem clock (32.768 kHz).
- (c) Convenient for program debugging and checking as interval becomes 128 times longer (3.91 ms) with the fast feed mode.
- (d) Outputs the frequencies (2.048, 4.096, 32.768 kHz) to the P23/BUZ pin, usable for buzzer and trimming of system clock frequencies.
- (e) Clears the frequency divider to make the clock start with zero seconds.
- (f) Uses the clock of 0.5 sec as the clock source of the timer/event counter to continue the standby mode until the longest time 9 hours (by using timer 0, 1) to be in the lowest consumption mode.

Figure 6-5. Watch Timer Block Diagram



Remark The values enclosed in parentheses are applied when $f_x = 4.194304$ MHz and $f_{xT} = 32.768$ kHz.

6.7 Timer/Event Counter

The μ PD750068 has two channels of timer/event counters. Its configuration is shown in Figures 6-6 and 6-7. The timer/event counter has the following functions.

- (a) Programmable interval timer operation
- (b) Square wave output of any frequency to the PTO_n pin (n = 0, 1)
- (c) Event counter operation
- (d) Divides the frequency of signal input via the TIn pin to 1-Nth of the original signal and outputs the divided frequency to the PTO_n pin (frequency divider operation).
- (e) Supplies the shift clock to the serial interface circuit.
- (f) Reads the count value.

The timer/event counter operates in the following two modes as set by the mode register.

Table 6-2. Operation Modes of Timer/Event Counter

Mode	Channel	
	Channel 0	Channel 1
8-bit timer/event counter mode	Yes	Yes
16-bit timer/event counter mode	Yes	

Figure 6-6. Timer/Event Counter Block Diagram (Channel 0)

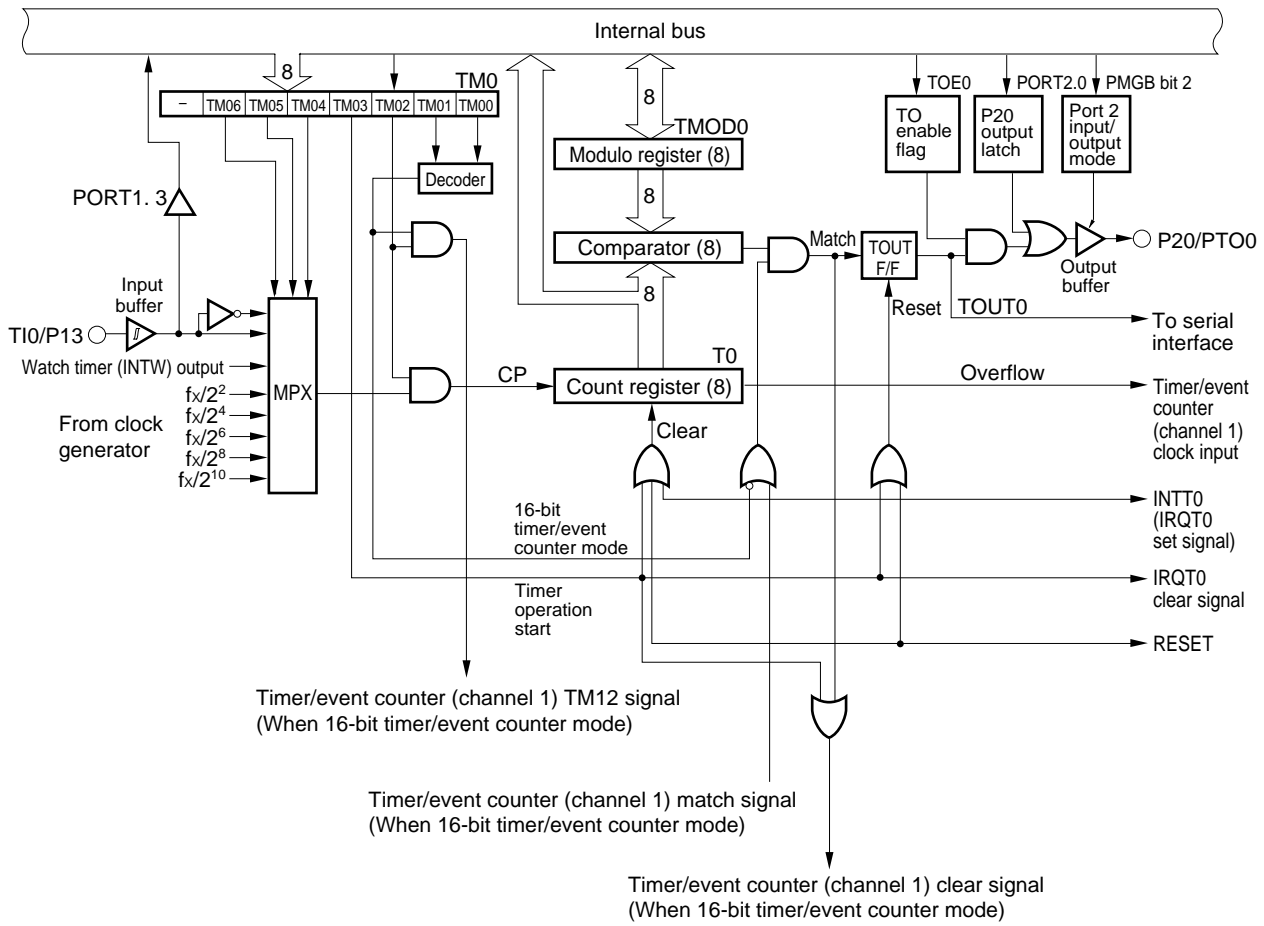
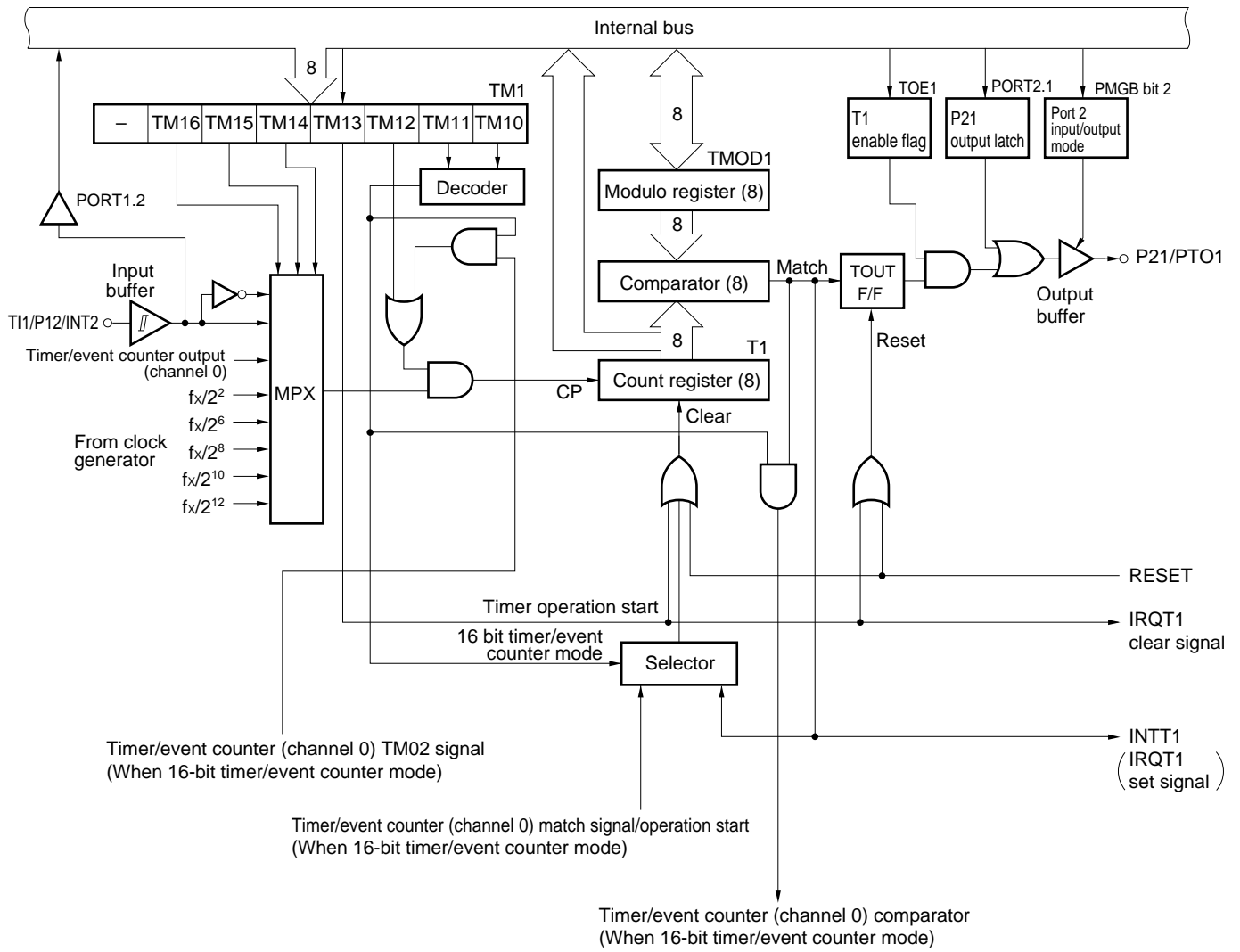


Figure 6-7. Timer/Event Counter Block Diagram (Channel 1)



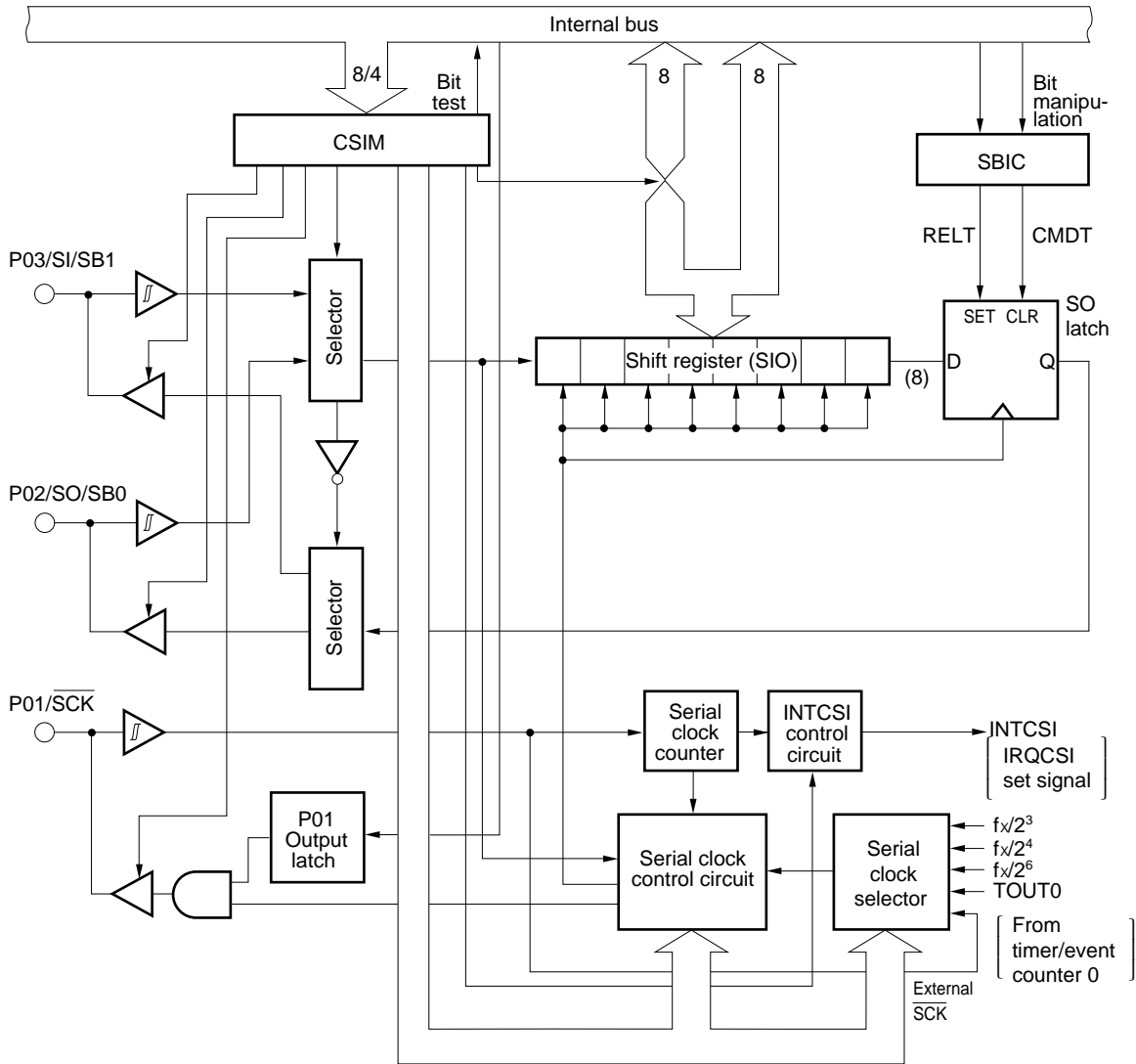
6.8 Serial Interface

The serial interface has the following three modes.

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode

The 3-wire serial I/O mode enables connections to be made with the 75X series, 78K series, and many other types of I/O devices. The 2-wire serial I/O mode enables communication with two or more devices.

Figure 6-8. Serial Interface Block Diagram



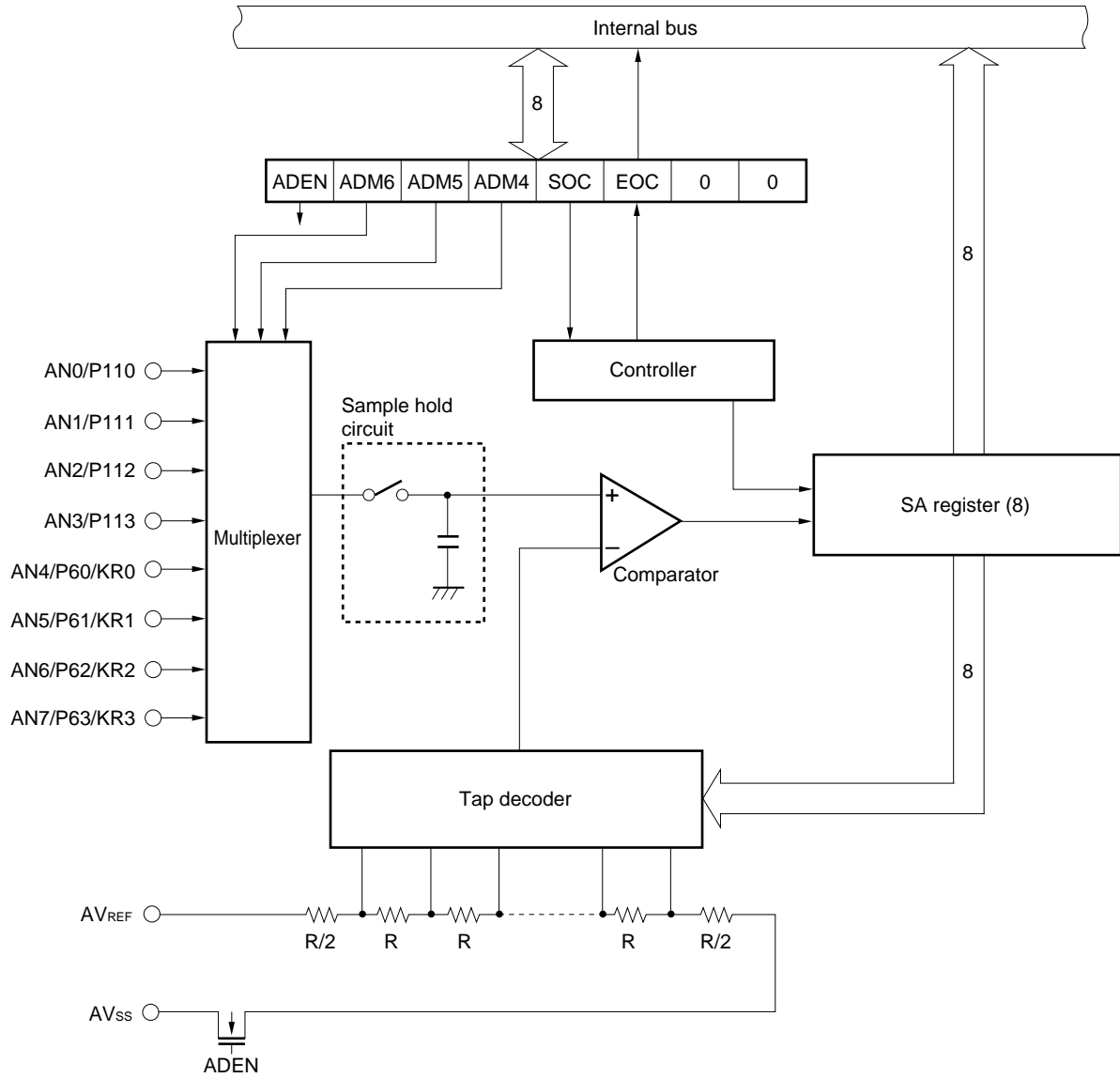
6.9 A/D Converter

The μ PD750068 incorporates the 8-bit resolution A/D converter which has eight channels analog input pins (AN0-AN7).

This A/D converter is a successive approximation type.

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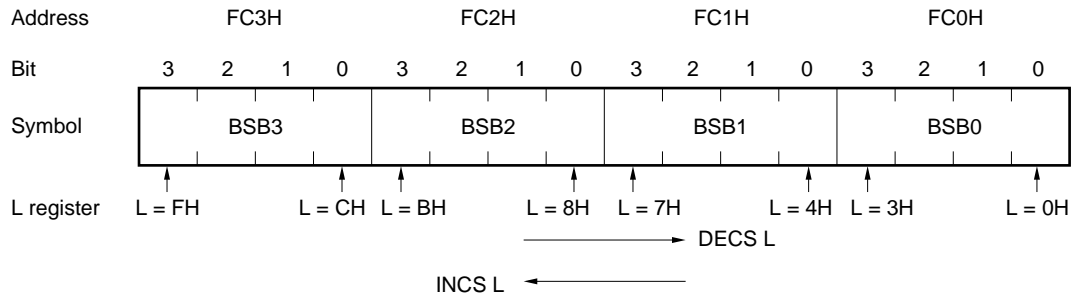
Figure 6-9. A/D Converter Block Diagram



6.10 Bit Sequential Buffer 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing a long data bit-wise.

Figure 6-10. Bit Sequential Buffer Format



- Remarks 1.** In the pmem.@L addressing, the specified bit moves corresponding to the L register.
- 2.** In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MBS specification.

7. INTERRUPT FUNCTION AND TEST FUNCTION

The μ PD750068 has seven interrupt sources and two test sources. One test source, INT2, has two types of edge detection testable inputs.

The interrupt control circuit of the μ PD750068 has the following functions.

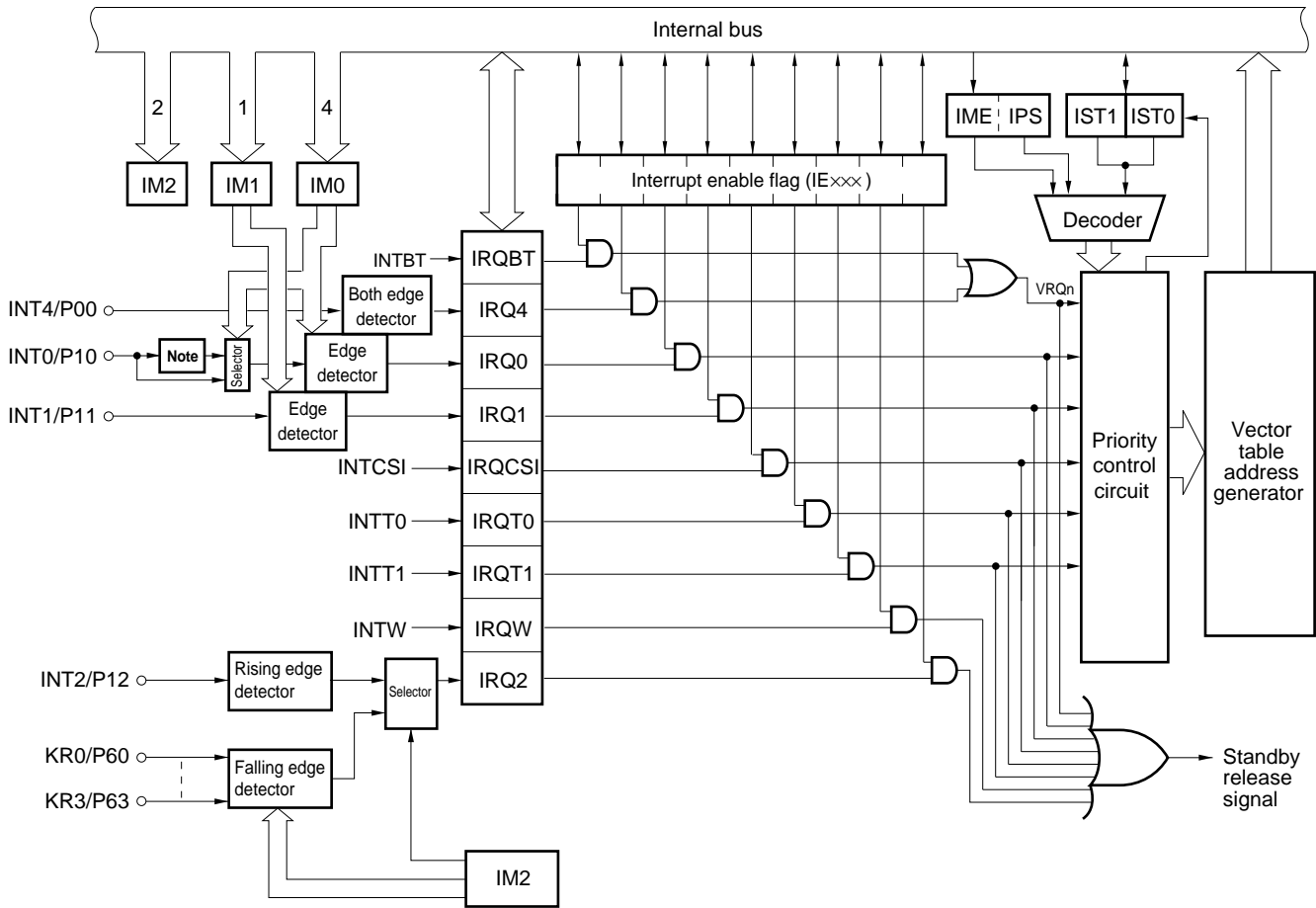
(1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IE $\times\times\times$) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ $\times\times\times$). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

(2) Test function

- Test request flag (IRQ $\times\times\times$) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 7-1. Interrupt Control Circuit Block Diagram



Note Noise elimination circuit (Standby release is disabled when noise elimination circuit is selected.)

8. STANDBY FUNCTION

In order to save power dissipation while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μ PD750068.

Table 8-1. Operation Status in Standby Mode

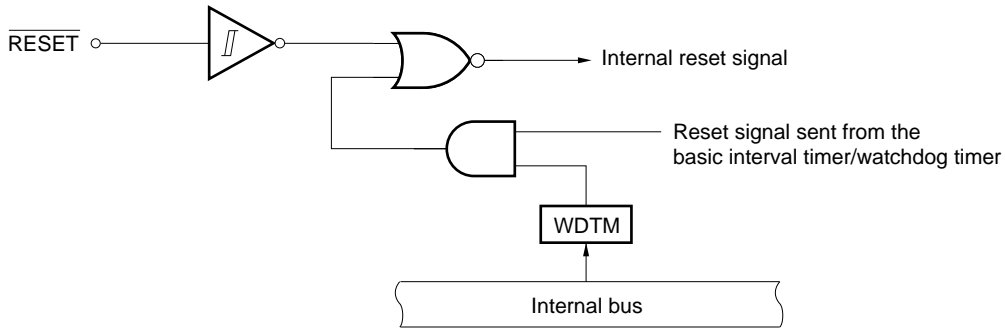
Mode		STOP mode	HALT mode
Item			
Set instruction		STOP instruction	HALT instruction
System clock when set		Settable only when the main system clock is used.	Settable both by the main system clock and subsystem clock.
Operation status	Clock generator	The main system clock stops oscillation.	Only the CPU clock Φ halts (oscillation continues).
	Basic interval timer/watchdog timer	Operation stops.	Operable only when the main system clock is oscillated (The IRQBT is set in the reference time interval).
	Serial interface	Operable only when an external \overline{SCK} input is selected as the serial clock.	Operable only when an external \overline{SCK} input is selected as the serial clock or when the main system clock is oscillated.
	Timer/event counter	Operable only when a signal input to the TI0 and TI1 pins or a watch timer which selected f_{XT} is specified as the count clock.	Operable only when a signal input to the TI0 and TI1 pins or a watch timer which selected f_{XT} is specified as the count clock or when the main system clock is oscillated.
	Watch timer	Operable when f_{XT} is selected as the count clock.	Operable.
	A/D converter	Operation stops.	Operable only when the main system clock is oscillated.
	External interrupt	The INT1, 2, and 4 are operable. Only the INT0 is not operated ^{Note} .	
	CPU	Operation stops.	
Release signal		Interrupt request signal sent from the operable hardware enabled by the interrupt enable flag or \overline{RESET} signal input.	

Note Can operate only when the noise elimination circuit is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

9. RESET FUNCTION

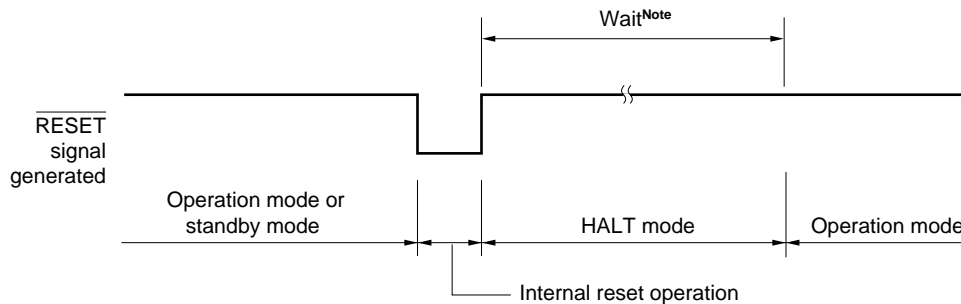
There are two reset inputs: external reset signal ($\overline{\text{RESET}}$) and reset signal sent from the basic interval timer/watchdog timer. When either one of the reset signals are input, an internal reset signal is generated. Figure 9-1 shows the configuration of the above two inputs.

Figure 9-1. Configuration of Reset Function



When the $\overline{\text{RESET}}$ signal is generated, each hardware is initialized as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation



Note The following two times can be selected by the mask option.

$2^{17}/f_x$ (21.8 ms: during 6.0-MHz operation, 31.3 ms: during 4.19-MHz operation)

$2^{15}/f_x$ (5.46 ms: during 6.0-MHz operation, 7.81 ms: during 4.19-MHz operation)

Table 9-1. Status of Each Hardware After Reset (1/2)

Hardware		RESET signal generation in the standby mode	RESET signal generation in operation
Program counter (PC)		μ PD750064	Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.
		μ PD750066, 750068	Sets the low-order 5 bits of program memory's address 0000H to the PC12-PC8 and the contents of address 0001H to the PC7-PC0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0-SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.
Stack pointer (SP)		Undefined	Undefined
Stack bank select register (SBS)		1000B	1000B
Data memory (RAM)		Held	Undefined
General-purpose register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank select register (MBS, RBS)		0, 0	0, 0
Basic interval timer/watchdog timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
	Watchdog timer enable flag (WDTM)	0	0
Timer/event counter (T0)	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Timer/event counter (T1)	Counter (T1)	0	0
	Modulo register (TMOD1)	FFH	FFH
	Mode register (TM1)	0	0
	TOE1, TOUT F/F	0, 0	0, 0
Watch timer	Mode register (WM)	0	0

Table 9-1. Status of Each Hardware After Reset (2/2)

Hardware		$\overline{\text{RESET}}$ signal generation in the standby mode	$\overline{\text{RESET}}$ signal generation in operation
Serial interface	Shift register (SIO)	Held	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Sub-oscillator control register (SOS)		0	0
A/D converter	Mode register (ADM)	04H	04H
	SA register (SA)	7FH	7FH
Interrupt function	Interrupt request flag (IRQ $\times\times\times$)	Reset (0)	Reset (0)
	Interrupt enable flag (IE $\times\times\times$)	0	0
	Interrupt priority selection register (IPS)	0	0
	INT0, 1, 2 mode registers (IM0, IM1, IM2)	0, 0, 0	0, 0, 0
Digital port	Output buffer	Off	Off
	Output latch	Cleared (0)	Cleared (0)
	I/O mode registers (PMGA, PMGB)	0	0
	Pull-up resistor setting register (POGA)	0	0
Bit sequential buffer (BSB0-BSB3)		Held	Undefined

★ 10. MASK OPTION

The μ PD750068 has the following mask options.

- Mask option of P40 to P43 and P50 to P53

Can select whether to incorporate the pull-up resistor.

- (1) The pull-up resistor is incorporated bit-wise.
- (2) The pull-up resistor is not incorporated.

- Mask option of standby function

Can select the wait time with the $\overline{\text{RESET}}$ signal.

- (1) $2^{17}/f_x$ (21.8 ms at $f_x = 6.0$ MHz, 31.3 ms at $f_x = 4.19$ MHz)
- (2) $2^{15}/f_x$ (5.46 ms at $f_x = 6.0$ MHz, 7.81 ms at $f_x = 4.19$ MHz)

- Mask option of subsystem clock

Can select whether to enable the internal feedback resistor.

- (1) The internal feedback resistor is enabled (switch internal feedback resistor ON/OFF by software).
- (2) The internal feedback resistor is disabled (disconnect internal feedback resistor by hardware).

11. INSTRUCTION SET

(1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to “**RA75X ASSEMBLER PACKAGE USERS’ MANUAL—LANGUAGE (EEU-1363)**”. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers or labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the register flags can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, see μ PD750068 User’s Manual (U10670E).

Expression format	Description method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label ^{Note} 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr, addr1 (Mk II mode only) caddr faddr	0000H-0FFFH immediate data or label (μ PD750064) 0000H-17FFH immediate data or label (μ PD750066) 0000H-1FFFH immediate data or label (μ PD750068) 12-bit immediate data or label 11-bit immediate data or label
taddr	20H-7FH immediate data (where bit0 = 0) or label
PORTn IExxx RBn MBn	PORT0-PORT6, PORT11 IEBT, IET0, IET1, IE0-IE2, IE4, IECSI, IEW RB0-RB3 MB0, MB1, MB15

Note mem can be only used for even address in 8-bit data processing.

(2) Legend in explanation of operation

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: XA register pair; 8-bit accumulator
BC	: BC register pair
DE	: DE register pair
HL	: HL register pair
XA'	: XA' expanded register pair
BC'	: BC' expanded register pair
DE'	: DE' expanded register pair
HL'	: HL' expanded register pair
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORT _n	: Port n (n = 0-6, 11)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IE _{xxx}	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Separation between address and bit
(xx)	: The contents addressed by xx
xxH	: Hexadecimal data

(3) Explanation of symbols under addressing area column

*1	MB = MBE•MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H-07FH) MB = 15 (F80H-FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-0FFFH (μ PD750064) 0000H-17FFH (μ PD750066) 0000H-1FFFH (μ PD750068)	Program memory addressing
*7	addr, addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH (μ PD750064) 0000H-0FFFH (PC ₁₂ = 0: μ PD750066, 750068) 1000H-17FFH (PC ₁₂ = 1: μ PD750066) 1000H-1FFFH (PC ₁₂ = 1: μ PD750068)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	Mk II mode only addr1 = 0000H-0FFFH (μ PD750064) 0000H-17FFH (μ PD750066) 0000H-1FFFH (μ PD750068)	

- Remarks 1.** MB indicates memory bank that can be accessed.
2. In *2, MB = 0 independently of how MBE and MBS are set.
 3. In *4 and *5, MB = 15 independently of how MBE and MBS are set.
 4. *6 to *11 indicate the areas that can be addressed.

(4) Explanation of number of machine cycles column

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction^{Note}: S = 2

Note 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle (= t_{cy}) of CPU clock Φ ; time can be selected from among four types by setting PCC.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	$A \leftarrow n4$		String effect A
		reg1, #n4	2	2	$reg1 \leftarrow n4$		
		XA, #n8	2	2	$XA \leftarrow n8$		String effect A
		HL, #n8	2	2	$HL \leftarrow n8$		String effect B
		rp2, #n8	2	2	$rp2 \leftarrow n8$		
		A, @HL	1	1	$A \leftarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftarrow (HL)$, then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftarrow (HL)$, then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftarrow (HL)$	*1	
		@HL, A	1	1	$(HL) \leftarrow A$	*1	
		@HL, XA	2	2	$(HL) \leftarrow XA$	*1	
		A, mem	2	2	$A \leftarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftarrow (mem)$	*3	
		mem, A	2	2	$(mem) \leftarrow A$	*3	
		mem, XA	2	2	$(mem) \leftarrow XA$	*3	
		A, reg1	2	2	$A \leftarrow reg1$		
		XA, rp'	2	2	$XA \leftarrow rp'$		
		reg1, A	2	2	$reg1 \leftarrow A$		
		rp'1, XA	2	2	$rp'1 \leftarrow XA$		
	XCH	A, @HL	1	1	$A \leftrightarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftrightarrow (HL)$, then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftrightarrow (HL)$, then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftrightarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftrightarrow (HL)$	*1	
		A, mem	2	2	$A \leftrightarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftrightarrow (mem)$	*3	
		A, reg1	1	1	$A \leftrightarrow reg1$		
		XA, rp'	2	2	$XA \leftrightarrow rp'$		

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Table reference	MOVT	XA, @PCDE	1	3	μ PD750064 $XA \leftarrow (PC_{11-8}+DE)_{ROM}$		
					μ PD750066, 750068 $XA \leftarrow (PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	μ PD750064 $XA \leftarrow (PC_{11-8}+XA)_{ROM}$		
					μ PD750066, 750068 $XA \leftarrow (PC_{12-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	$XA \leftarrow (BCDE)_{ROM}$ ^{Note}	*6	
	XA, @BCXA	1	3	$XA \leftarrow (BCXA)_{ROM}$ ^{Note}	*6		
Bit transfer	MOV1	CY, fmem.bit	2	2	$CY \leftarrow (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow (pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow (H+mem_{3-0}.bit)$	*1	
		fmem.bit, CY	2	2	$(fmem.bit) \leftarrow CY$	*4	
		pmem.@L, CY	2	2	$(pmem_{7-2}+L_{3-2}.bit(L_{1-0})) \leftarrow CY$	*5	
		@H+mem.bit, CY	2	2	$(H+mem_{3-0}.bit) \leftarrow CY$	*1	
Operation	ADDS	A, #n4	1	1+S	$A \leftarrow A+n4$		carry
		XA, #n8	2	2+S	$XA \leftarrow XA+n8$		carry
		A, @HL	1	1+S	$A \leftarrow A+(HL)$	*1	carry
		XA, rp'	2	2+S	$XA \leftarrow XA+rp'$		carry
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1+XA$		carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A+(HL)+CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA+rp'+CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1+XA+CY$		
	SUBS	A, @HL	1	1+S	$A \leftarrow A-(HL)$	*1	borrow
		XA, rp'	2	2+S	$XA \leftarrow XA-rp'$		borrow
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1-XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A-(HL)-CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA-rp'-CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1-XA-CY$		

Note Set "0" to register B if the μ PD750064 is used. Only low-order one bit of register B will be valid if the μ PD750066, 750068 is used.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Operation	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
	XOR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		
Increment and Decrement	INCS	reg	1	1+S	$reg \leftarrow reg+1$		reg = 0
		rp1	1	1+S	$rp1 \leftarrow rp1+1$		rp1 = 00H
		@HL	2	2+S	$(HL) \leftarrow (HL)+1$	*1	(HL) = 0
		mem	2	2+S	$(mem) \leftarrow (mem)+1$	*3	(mem) = 0
	DECS	reg	1	1+S	$reg \leftarrow reg-1$		reg = FH
		rp'	2	2+S	$rp' \leftarrow rp'-1$		rp' = FFH
Comparison	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	$CY \leftarrow 1$		
	CLR1	CY	1	1	$CY \leftarrow 0$		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) \leftarrow 1	*3	
		fmem.bit	2	2	(fmem.bit) \leftarrow 1	*4	
		pmem.@L	2	2	(pmem _{7-2+L3-2} .bit(L ₁₋₀)) \leftarrow 1	*5	
		@H+mem.bit	2	2	(H+mem ₃₋₀ .bit) \leftarrow 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) \leftarrow 0	*3	
		fmem.bit	2	2	(fmem.bit) \leftarrow 0	*4	
		pmem.@L	2	2	(pmem _{7-2+L3-2} .bit(L ₁₋₀)) \leftarrow 0	*5	
		@H+mem.bit	2	2	(H+mem ₃₋₀ .bit) \leftarrow 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if (fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if (pmem _{7-2+L3-2} .bit(L ₁₋₀))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if (H+mem ₃₋₀ .bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if (mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if (fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if (pmem _{7-2+L3-2} .bit(L ₁₋₀))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if (H+mem ₃₋₀ .bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if (pmem _{7-2+L3-2} .bit(L ₁₋₀))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if (H+mem ₃₋₀ .bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY \leftarrow CY \wedge (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY \leftarrow CY \wedge (pmem _{7-2+L3-2} .bit(L ₁₋₀))	*5	
		CY, @H+mem.bit	2	2	CY \leftarrow CY \wedge (H+mem ₃₋₀ .bit)	*1	
	OR1	CY, fmem.bit	2	2	CY \leftarrow CY \vee (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY \leftarrow CY \vee (pmem _{7-2+L3-2} .bit(L ₁₋₀))	*5	
		CY, @H+mem.bit	2	2	CY \leftarrow CY \vee (H+mem ₃₋₀ .bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY \leftarrow CY \vee (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY \leftarrow CY \vee (pmem _{7-2+L3-2} .bit(L ₁₋₀))	*5	
		CY, @H+mem.bit	2	2	CY \leftarrow CY \vee (H+mem ₃₋₀ .bit)	*1	

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Branch	BR ^{Note}	addr	-	-	μ PD750064 PC ₁₁₋₀ ← addr (Select appropriate instruction from among BR !addr, BRCB !caddr and BR \$addr according to the assembler being used.)	*6	
					μ PD750066, 750068 PC ₁₂₋₀ ← addr (Select appropriate instruction from among BR !addr, BRCB !caddr and BR \$addr according to the assembler being used.)		
		addr1	-	-	μ PD750064 PC ₁₁₋₀ ← addr1 (Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR \$addr1 according to the assembler being used.)	*11	
					μ PD750066, 750068 PC ₁₂₋₀ ← addr1 (Select appropriate instruction from among BR !addr, BRA !addr1, BRCB !caddr and BR \$addr1 according to the assembler being used.)		
		!addr	3	3	μ PD750064 PC ₁₁₋₀ ← addr μ PD750066, 750068 PC ₁₂₋₀ ← addr	*6	
\$addr	1	2	μ PD750064 PC ₁₁₋₀ ← addr μ PD750066, 750068 PC ₁₂₋₀ ← addr	*7			
\$addr1	1	2	μ PD750064 PC ₁₁₋₀ ← addr1 μ PD750066, 750068 PC ₁₂₋₀ ← addr1				

Note The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition	
Branch	BR	PCDE	2	3	μ PD750064 PC ₁₁₋₀ ← PC ₁₁₋₈ +DE			
					μ PD750066, 750068 PC ₁₂₋₀ ← PC ₁₂₋₈ +DE			
		PCXA		2	3	μ PD750064 PC ₁₁₋₀ ← PC ₁₁₋₈ +XA		
						μ PD750066, 750068 PC ₁₂₋₀ ← PC ₁₂₋₈ +XA		
		BCDE		2	3	μ PD750064 PC ₁₁₋₀ ← BCDE ^{Note 1}	*6	
						μ PD750066, 750068 PC ₁₂₋₀ ← BCDE ^{Note 2}		
		BCXA		2	3	μ PD750064 PC ₁₁₋₀ ← BCXA ^{Note 1}	*6	
						μ PD750066, 750068 PC ₁₂₋₀ ← BCXA ^{Note 2}		
		BRA^{Note 3}		3	3	μ PD750064 PC ₁₁₋₀ ← addr1	*11	
						μ PD750066, 750068 PC ₁₂₋₀ ← addr1		
	BRCB	!caddr	2	2	μ PD750064 PC ₁₁₋₀ ← caddr ₁₁₋₀	*8		
					μ PD750066, 750068 PC ₁₂₋₀ ← PC ₁₂ +caddr ₁₁₋₀			
Subroutine stack control	CALLA ^{Note 3}		3	3	μ PD750064 (SP-2) ← X, X, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC ₁₁₋₀ (SP-5) ← 0, 0, 0, 0 PC ₁₁₋₀ ← addr1, SP ← SP-6	*11		
					μ PD750066, 750068 (SP-2) ← X, X, MBE, RBE (SP-6) (SP-3) (SP-4) ← PC ₁₁₋₀ (SP-5) ← 0, 0, 0, PC ₁₂ PC ₁₂₋₀ ← addr1, SP ← SP-6			

- Notes**
1. "0" must be set to B register.
 2. Only low-order one bit is valid in B register.
 3. The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control	CALL ^{Note}	!addr	3	3	μ PD750064 (SP-3) \leftarrow MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) \leftarrow PC ₁₁₋₀ PC ₁₁₋₀ \leftarrow addr, SP \leftarrow SP-4	*6	
					μ PD750066, 750068 (SP-3) \leftarrow MBE, RBE, 0, PC ₁₂ (SP-4) (SP-1) (SP-2) \leftarrow PC ₁₁₋₀ PC ₁₂₋₀ \leftarrow addr, SP \leftarrow SP-4		
				4	μ PD750064 (SP-2) \leftarrow x, x, MBE, RBE (SP-6) (SP-3) (SP-4) \leftarrow PC ₁₁₋₀ (SP-5) \leftarrow 0, 0, 0, 0 PC ₁₁₋₀ \leftarrow addr, SP \leftarrow SP-6		
					μ PD750066, 750068 (SP-2) \leftarrow x, x, MBE, RBE (SP-6) (SP-3) (SP-4) \leftarrow PC ₁₁₋₀ (SP-5) \leftarrow 0, 0, 0, PC ₁₂ PC ₁₂₋₀ \leftarrow addr, SP \leftarrow SP-6		
	CALLF ^{Note}	!faddr	2	2	μ PD750064 (SP-3) \leftarrow MBE, RBE, 0, 0 (SP-4) (SP-1) (SP-2) \leftarrow PC ₁₁₋₀ PC ₁₁₋₀ \leftarrow 0+faddr, SP \leftarrow SP-4	*9	
				μ PD750066, 750068 (SP-3) \leftarrow MBE, RBE, 0, PC ₁₂ (SP-4) (SP-1) (SP-2) \leftarrow PC ₁₁₋₀ PC ₁₂₋₀ \leftarrow 00+faddr, SP \leftarrow SP-4			
				3	μ PD750064 (SP-2) \leftarrow x, x, MBE, RBE (SP-6) (SP-3) (SP-4) \leftarrow PC ₁₁₋₀ (SP-5) \leftarrow 0, 0, 0, 0 PC ₁₁₋₀ \leftarrow 0+faddr, SP \leftarrow SP-6		
					μ PD750066, 750068 (SP-2) \leftarrow x, x, MBE, RBE (SP-6) (SP-3) (SP-4) \leftarrow PC ₁₁₋₀ (SP-5) \leftarrow 0, 0, 0, PC ₁₂ PC ₁₂₋₀ \leftarrow 00+faddr, SP \leftarrow SP-6		

Note The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control	RET ^{Note}		1	3	<p>μPD750064 $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ MBE, RBE, 0, 0 $\leftarrow (SP+1)$, $SP \leftarrow SP+4$</p> <p>μPD750066, 750068 $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ MBE, RBE, 0, $PC_{12} \leftarrow (SP+1)$, $SP \leftarrow SP+4$</p> <p>μPD750064 X, X, MBE, RBE $\leftarrow (SP+4)$ 0, 0, 0, 0, $\leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$, $SP \leftarrow SP+6$</p> <p>μPD750066, 750068 X, X, MBE, RBE $\leftarrow (SP+4)$ MBE, 0, 0, $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$, $SP \leftarrow SP+6$</p>		
	RETS ^{Note}		1	3+S	<p>μPD750064 MBE, RBE, 0, 0 $\leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ $SP \leftarrow SP+4$ then skip unconditionally</p> <p>μPD750066, 750068 MBE, RBE, 0, $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ $SP \leftarrow SP+4$ then skip unconditionally</p> <p>μPD750064 0, 0, 0, 0 $\leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ X, X, MBE, RBE $\leftarrow (SP+4)$ $SP \leftarrow SP+6$ then skip unconditionally</p> <p>μPD750066, 750068 0, 0, 0, $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP) (SP+3) (SP+2)$ X, X, MBE, RBE $\leftarrow (SP+4)$ $SP \leftarrow SP+4$ then skip unconditionally</p>		Unconditional

Note The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control	RET ^{Note 1}		1	3	μ PD750064 MBE, RBE, 0, 0 \leftarrow (SP+1) PC ₁₁₋₀ \leftarrow (SP) (SP+3) (SP+2) PSW \leftarrow (SP+4) (SP+5), SP \leftarrow SP+6 μ PD750066, 750068 MBE, RBE, 0, PC ₁₂ \leftarrow (SP+1) PC ₁₁₋₀ \leftarrow (SP) (SP+3) (SP+2) PSW \leftarrow (SP+4) (SP+5), SP \leftarrow SP+6 μPD750064 0, 0, 0, 0 \leftarrow (SP+1) PC ₁₁₋₀ \leftarrow (SP) (SP+3) (SP+2) PSW \leftarrow (SP+4) (SP+5), SP \leftarrow SP+6 μPD750066, 750068 0, 0, 0, PC ₁₂ \leftarrow (SP+1) PC ₁₁₋₀ \leftarrow (SP) (SP+3) (SP+2) PSW \leftarrow (SP+4) (SP+5), SP \leftarrow SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) \leftarrow rp, SP \leftarrow SP-2		
		BS	2	2	(SP-1) \leftarrow MBS, (SP-2) \leftarrow RBS, SP \leftarrow SP-2		
	POP	rp	1	1	rp \leftarrow (SP+1) (SP), SP \leftarrow SP+2		
		BS	2	2	MBS \leftarrow (SP+1), RBS \leftarrow (SP), SP \leftarrow SP+2		
	Interrupt control	EI		2	2	IME (IPS.3) \leftarrow 1	
IE _{xxx}			2	2	IE _{xxx} \leftarrow 1		
DI			2	2	IME (IPS.3) \leftarrow 0		
		IE _{xxx}	2	2	IE _{xxx} \leftarrow 0		
Input/output	IN ^{Note 2}	A, PORT _n	2	2	A \leftarrow PORT _n (n = 0-6, 11)		
		XA, PORT _n	2	2	XA \leftarrow PORT _{n+1} , PORT _n (n = 4)		
	OUT ^{Note 2}	PORT _n , A	2	2	PORT _n \leftarrow A (n = 2-6)		
		PORT _n , XA	2	2	PORT _{n+1} , PORT _n \leftarrow XA (n = 4)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 \leftarrow 1)		
	STOP		2	2	Set STOP Mode (PCC.3 \leftarrow 1)		
	NOP		1	1	No Operation		
Special	SEL	RB _n	2	2	RBS \leftarrow n (n = 0-3)		
		MB _n	2	2	MBS \leftarrow n (n = 0, 1, 15)		

- Notes 1.** The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.
- 2.** While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1, and MBS must be set to 15.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition	
Special	GETI ^{Notes 1, 2}	taddr	1	3	μPD750064 • When TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$	*10		
					• When TCALL instruction $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, 0$ $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ $SP \leftarrow SP-4$			
					• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction	
					μPD750066, 750068 • When TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$			
					• When TCALL instruction $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$ $SP \leftarrow SP-4$			
					• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction	
					3 μPD750064 • When TBR instruction $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$		*10	
					4 • When TCALL instruction $(SP-6) (SP-3) (SP-4) \leftarrow PC_{11-0}$ $(SP-5) \leftarrow 0, 0, 0, 0$ $(SP-2) \leftarrow \times, \times, MBE, RBE$ $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr+1)$ $SP \leftarrow SP-6$			
					• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.			Depending on the reference instruction
					3 μPD750066, 750068 • When TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$			
4 • When TCALL instruction $(SP-6) (SP-3) (SP-4) \leftarrow PC_{11-0}$ $(SP-5) \leftarrow 0, 0, 0, PC_{12}$ $(SP-2) \leftarrow \times, \times, MBE, RBE$ $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr+1)$ $SP \leftarrow SP-6$								
• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.	Depending on the reference instruction							

- Notes 1.** The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.
- 2.** The operations indicated with thick lines can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

★ **12. ELECTRICAL SPECIFICATIONS**

Absolute Maximum Ratings (T_A = 25 °C)

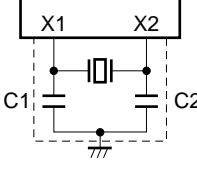
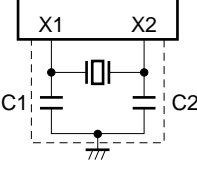
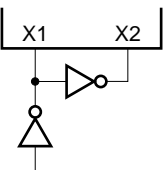
Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V _{DD}		-0.3 to +7.0	V	
Input voltage	V _{I1}	Other than ports 4, 5	-0.3 to V _{DD} +0.3	V	
	V _{I2}	Ports 4, 5	Pull-up resistor provided	-0.3 to V _{DD} +0.3	V
			N-ch open drain	-0.3 to +14	V
Output voltage	V _O		-0.3 to V _{DD} +0.3	V	
High-level output current	I _{OH}	Per pin	-10	mA	
		Total of all pins	-30	mA	
Low-level output current	I _{OL}	Per pin	30	mA	
		Total of all pins	220	mA	
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Caution If the absolute maximum rating of even one of the parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are therefore values which, when exceeded, can cause the product to be damaged. Be sure that these values are never exceeded when using the product.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz			15	pF
Output capacitance	C _{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C _{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

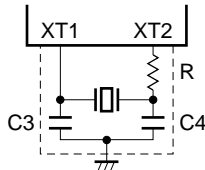
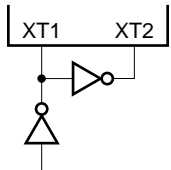
Resonator	Recommended Constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		6.0 ^{Note 2}	MHz
		Oscillation stabilization time ^{Note 3}	After V _{DD} has reached MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		6.0 ^{Note 2}	MHz
		Oscillation stabilization time ^{Note 3}	V _{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		6.0 ^{Note 2}	MHz
		X1 input high-, low-level widths (t _{xH} , t _{xL})			83.3		500

- Notes 1.** The oscillation frequency and X1 input frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to AC Characteristics.
- If the oscillation frequency is 4.19 MHz < f_x - 6.0 MHz at 1.8 V - V_{DD} < 2.7 V, do not select the processor clock control register (PCC) = 0011. If PCC = 0011, one machine cycle time is less than 0.95 μs, falling short of the rated value of 0.95 μs.
 - The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied or STOP mode has been released.

Caution When using the main system clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- Keep the wiring length as short as possible.
- Do not cross the wiring with other signal lines.
- Do not route the wiring in the vicinity of a line through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.
- Do not ground to a ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

Subsystem Clock Oscillation Circuit Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Resonator	Recommended Constants	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) ^{Note 1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	$V_{DD} = 4.5$ to 5.5 V		1.0	2	s
External clock		XT1 input frequency (f_{XT}) ^{Note 1}		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH} , t_{XTL})		5		15	μ s

- Notes 1.** The oscillation frequency and XT1 input frequency shown above indicate characteristics of the oscillation circuit only. For the instruction execution time, refer to AC Characteristics.
- 2.** The oscillation stabilization time is the time required for oscillation to be stabilized after V_{DD} has been applied.

Caution When using the subsystem clock oscillation circuit, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:

- Keep the wiring length as short as possible.
- Do not cross the wiring with other signal lines.
- Do not route the wiring in the vicinity of a line through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS} .
- Do not ground to a ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

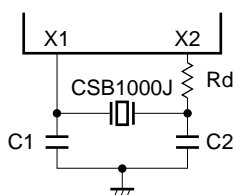
The subsystem clock oscillation circuit has a low amplification factor to reduce current dissipation and is more susceptible to noise than the main system clock oscillation circuit. Therefore, exercise utmost care in wiring the subsystem clock oscillation circuit.

Recommended Oscillation Circuit Constants

Ceramic resonator (T_A = -40 to +85 °C)

Manufacturer	Part Number	Frequency (MHz)	Oscillation Circuit Constant (pF)		Oscillation Voltage Range (V _{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB1000J ^{Note}	1.0	100	100	2.0	5.5	Rd = 1 kΩ
	CSA2.00MG040	2.0	100	100	2.3		-
	CST2.00MG040		-	-			Capacitor-contained model
	CSA4.19MG	4.19	30	30	1.9		-
	CST4.19MGW		-	-			Capacitor-contained model
	CSA4.19MGU		30	30	1.8		-
	CST4.19MGWU		-	-			Capacitor-contained model
	CSA6.00MG	6.0	30	30	3.0		-
	CST6.00MGW		-	-			Capacitor-contained model
	CSA6.00MGU		30	30	2.4		-
	CST6.00MGWU		-	-			Capacitor-contained model
	Kyocera Corp.	KBR-1000F/Y	1.0	100	100		1.8
KBR-2.0MS		2.0	68	68	1.95		
KBR-4.19MSA		4.19	33	33	1.8		
KBR-6.0MSA		6.0	33	33			
TDK	CCR1000K2	1.0	100	100	1.8	5.5	-
	CCR2.0MC33	2.0	-	-	2.0		Capacitor-contained model
	CCR4.19MC3	4.19			2.2		
	FCR4.19MC5				2.2		
	CCR6.0MC3	6.0			2.0		
	FCR6.0MC5				2.2		

Note When using the CSB1000J (1.0 MHz) by Murata Mfg. Co., Ltd. as a ceramic resonator, a limiting resistor (Rd = 1 kΩ) is necessary (refer to the figure below). The limiting resistor is not necessary when using the other recommended resonators.



Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit		
Low-level output current	I_{OL}	Per pin				15	mA		
		Total of all pins				150	mA		
High-level input voltage	V_{IH1}	Ports 2, 3, 11		$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	$0.7 V_{DD}$	V_{DD}	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	$0.9 V_{DD}$	V_{DD}	V		
	V_{IH2}	Ports 0, 1, 6, $\overline{\text{RESET}}$		$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	$0.8 V_{DD}$	V_{DD}	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	$0.9 V_{DD}$	V_{DD}	V		
	V_{IH3}	Ports 4, 5	Pull-up resistor provided	$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	$0.7 V_{DD}$	V_{DD}	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	$0.9 V_{DD}$	V_{DD}	V		
			N-ch open drain	$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	$0.7 V_{DD}$	13	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	$0.9 V_{DD}$	13	V		
V_{IH4}	X1, XT1		$V_{DD}-0.1$		V_{DD}	V			
Low-level input voltage	V_{IL1}	Ports 2, 3, 4, 5, 11		$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	0	$0.3 V_{DD}$	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	0	$0.1 V_{DD}$	V		
	V_{IL2}	Ports 0, 1, 6, $\overline{\text{RESET}}$		$2.7\text{ V} - V_{DD} - 5.5\text{ V}$	0	$0.2 V_{DD}$	V		
				$1.8\text{ V} - V_{DD} < 2.7\text{ V}$	0	$0.1 V_{DD}$	V		
V_{IL3}	X1, XT1		0		0.1	V			
High-level output voltage	V_{OH}	$\overline{\text{SCK}}$, SO, ports 2, 3, 6 $I_{OH} = -1.0\text{ mA}$		$V_{DD}-0.5$			V		
Low-level output voltage	V_{OL1}	$\overline{\text{SCK}}$, SO, ports 2, 3, 4, 5, 6		$I_{OL} = 15\text{ mA}$ $V_{DD} = 4.5$ to 5.5 V		0.2	2.0	V	
				$I_{OL} = 1.6\text{ mA}$			0.4	V	
V_{OL2}	SB0, SB1	N-ch open drain Pull-up resistor • 1 k Ω				$0.2 V_{DD}$	V		
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	Pins other than X1, XT1				3	μA	
	I_{LIH2}		X1, XT1				20	μA	
	I_{LIH3}	$V_{IN} = 13\text{ V}$	Ports 4, 5 (N-ch open drain)				20	μA	
Low-level input leakage current	I_{LIL1}	$V_{IN} = 0\text{ V}$	Pins other than ports 4, 5, X1, XT1				-3	μA	
	I_{LIL2}		X1, XT1				-20	μA	
	I_{LIL3}		Ports 4, 5 (N-ch open drain) When input instruction is not executed					-3	μA
			Ports 4, 5 (N-ch open drain) When input instruction is executed		$V_{DD} = 5.0\text{ V}$		-10	-27	μA
			$V_{DD} = 3.0\text{ V}$		-3	-8	μA		
High-level output leakage current	I_{LOH1}	$V_{OUT} = V_{DD}$	$\overline{\text{SCK}}$, SO/SB0, SB1, ports 2, 3, 6, ports 4, 5 (Pull-up resistor provided)				3	μA	
	I_{LOH2}	$V_{OUT} = 13\text{ V}$	Ports 4, 5 (N-ch open drain)				20	μA	
Low-level output leakage current	I_{LOL}	$V_{OUT} = 0\text{ V}$				-3	μA		
Internal pull-up resistor	R_{L1}	$V_{IN} = 0\text{ V}$	Ports 0, 1, 2, 3, 6 (except pin P00)		50	100	200	k Ω	
	R_{L2}		Ports 4, 5		15	30	60	k Ω	

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD1}	6.0 MHz ^{Note 2} crystal oscillation	V _{DD} = 5.0 V ±10 % ^{Note 3}			2.2	6.6	mA
			V _{DD} = 3.0 V ±10 % ^{Note 4}			0.48	1.5	mA
	I _{DD2}	C1 = C2 = 22 pF	HALT mode	V _{DD} = 5.0 V ±10 %		0.86	2.6	mA
				V _{DD} = 3.0 V ±10 %		0.43	1.3	mA
	I _{DD1}	4.19 MHz ^{Note 2} crystal oscillation	V _{DD} = 5.0 V ±10 % ^{Note 3}			1.7	4.5	mA
			V _{DD} = 3.0 V ±10 % ^{Note 4}			0.4	1.2	mA
	I _{DD2}	C1 = C2 = 22 pF	HALT mode	V _{DD} = 5.0 V ±10 %		0.7	2	mA
				V _{DD} = 3.0 V ±10 %		0.39	1.2	mA
	I _{DD3}	32.768 kHz ^{Note 5} crystal oscillation	Low- voltage mode ^{Note 6}	V _{DD} = 3.0 V ±10 %		11	33	μA
				V _{DD} = 2.0 V ±10 %		5.5	17	μA
				V _{DD} = 3.0 V, T _A = 25 °C		11	22	μA
			Low current dissipation mode ^{Note 7}	V _{DD} = 3.0 V ±10 %		9.2	27	μA
				V _{DD} = 3.0 V, T _A = 25 °C		9.2	18	μA
	I _{DD4}	HALT mode	Low- voltage mode ^{Note 6}	V _{DD} = 3.0 V ±10 %		6.4	20	μA
V _{DD} = 2.0 V ±10 %					2.5	8	μA	
Low current dissipation mode ^{Note 7}			V _{DD} = 3.0 V, T _A = 25 °C		6.4	12.8	μA	
			V _{DD} = 3.0 V ±10 %		4.6	13.8	μA	
I _{DD5}	XT1 = 0 V ^{Note 8} STOP mode	V _{DD} = 5.0 V ±10 %			0.05	10	μA	
		V _{DD} = 3.0 V ±10 %			0.02	5	μA	
		T _A = 25 °C			0.02	3	μA	

- Notes**
1. The current flowing through the internal pull-up resistor is not included.
 2. Including the case when the subsystem clock oscillates.
 3. When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.
 4. When the device operates in low-speed mode with PCC set to 0000.
 5. When the device operates on the subsystem clock, with the system clock control register (SCC) set to 1001 and oscillation of the main system clock stopped.
 6. When the sub-oscillation circuit control register (SOS) is set to 0000.
 7. When SOS is set to 0010.
 8. When SOS is set to 00×1, and the sub-oscillation circuit feedback resistor is not used (×: don't care).

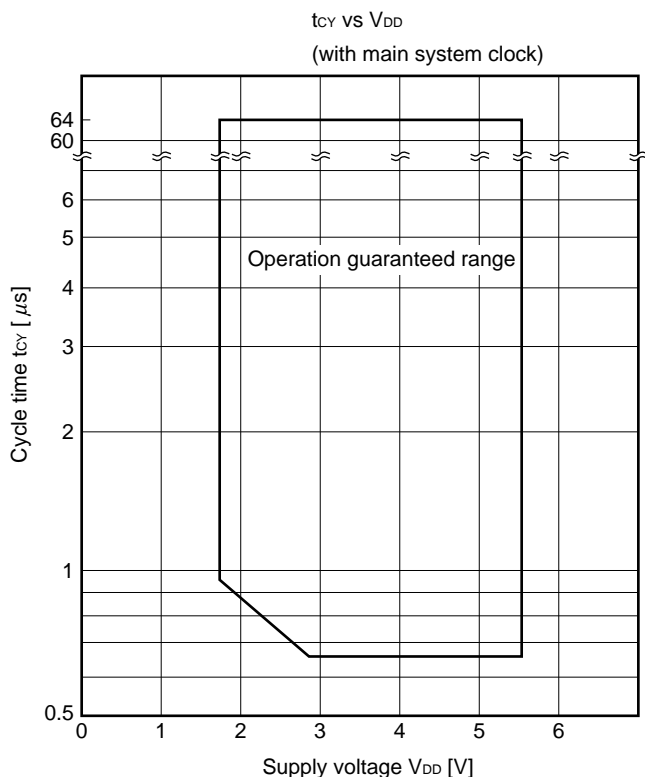
AC Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time ^{Note 1} (minimum instruction execution time = 1 machine cycle)	t _{cy}	Operates with main system clock	V _{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operates with subsystem clock		114	122	125	μs
T10, T11 input frequency	f _{TI}	V _{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
T10, T11 input high-, low-level widths	t _{TIH} , t _{TIL}	V _{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-, low-level widths	t _{INTH} , t _{INTL}	INT0	IM02 = 0	Note 2			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0-3		10			μs
RESET low-level width	t _{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC), and processor clock control register (PCC).

The figure on the right shows the supply voltage V_{DD} vs. cycle time t_{cy} characteristics when the device operates with the main system clock.

2. 2t_{cy} or 128/f_x depending on the setting of the interrupt mode register (IM0).



Serial transfer operation

2-wire and 3-wire serial I/O modes ($\overline{\text{SCK}}$... internal clock output): ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY1}	$V_{DD} = 2.7$ to 5.5 V	1300			ns
			3800			ns
$\overline{\text{SCK}}$ high-, low-level widths	$t_{\text{KL1}},$ t_{KH1}	$V_{DD} = 2.7$ to 5.5 V	$t_{\text{KCY1}}/2-50$			ns
			$t_{\text{KCY1}}/2-150$			ns
SI ^{Note 1} setup time (to $\overline{\text{SCK}}$ ↑)	t_{SIK1}	$V_{DD} = 2.7$ to 5.5 V	150			ns
			500			ns
SI ^{Note 1} hold time (from $\overline{\text{SCK}}$ ↑)	t_{KSI1}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			600			ns
$\overline{\text{SCK}}$ ↓ → SO ^{Note 1} output delay time	t_{KSO1}	$R_L = 1$ k Ω , $C_L = 100$ pF	$V_{DD} = 2.7$ to 5.5 V		250	ns
				0		1000

- Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.
2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

2-wire and 3-wire serial I/O modes ($\overline{\text{SCK}}$... external clock input): ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY2}	$V_{DD} = 2.7$ to 5.5 V	800			ns
			3200			ns
$\overline{\text{SCK}}$ high-, low-level widths	$t_{\text{KL2}},$ t_{KH2}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			1600			ns
SI ^{Note 1} setup time (to $\overline{\text{SCK}}$ ↑)	t_{SIK2}	$V_{DD} = 2.7$ to 5.5 V	100			ns
			150			ns
SI ^{Note 1} hold time (from $\overline{\text{SCK}}$ ↑)	t_{KSI2}	$V_{DD} = 2.7$ to 5.5 V	400			ns
			600			ns
$\overline{\text{SCK}}$ ↓ → SO ^{Note 1} output delay time	t_{KSO2}	$R_L = 1$ k Ω , $C_L = 100$ pF	$V_{DD} = 2.7$ to 5.5 V		300	ns
				0		1000

- Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.
2. R_L and C_L respectively indicate the load resistance and load capacitance of the SO output line.

A/D Converter Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V, 1.8 V - AV_{REF} - V_{DD})

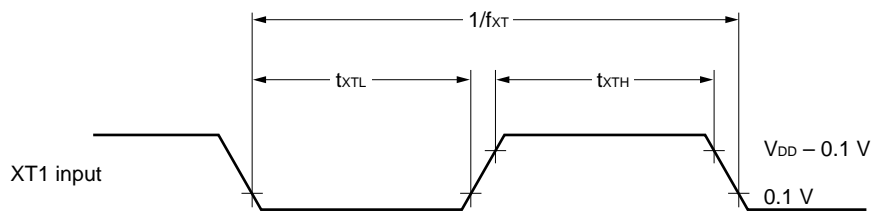
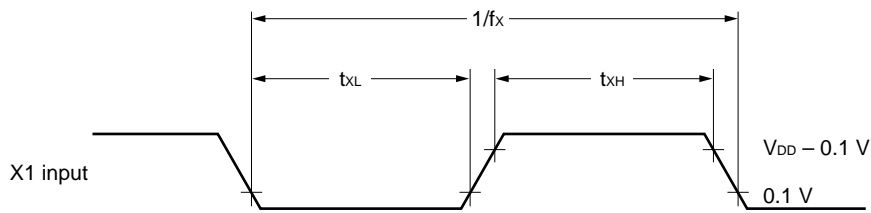
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution			8	8	8	bit	
Absolute accuracy ^{Note 1}		$V_{DD} = AV_{REF}$	2.7 V - V_{DD}			1.5	LSB
			1.8 V - $V_{DD} < 2.7$ V			3	LSB
		$V_{DD} \cdot AV_{REF}$				3	LSB
Conversion time	t_{CONV}	Note 2			$168/f_X$	μ s	
Sampling time	t_{SAMP}	Note 3			$44/f_X$	μ s	
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V	
Analog input impedance	R_{AN}			1000		M Ω	
AV_{REF} current	I_{REF}			0.25	2.0	mA	

- Notes**
1. Absolute accuracy excluding quantization error ($\pm 1/2$ LSB)
 2. Time until end of conversion (EOC = 1) after execution of conversion start instruction (40.1μ s: $f_X = 4.19$ MHz).
 3. Time until end of sampling after execution of conversion start instruction (10.5μ s: $f_X = 4.19$ MHz).

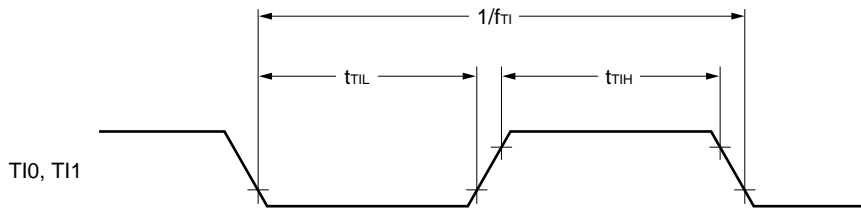
AC timing test points (except X1 and XT1 inputs)



Clock timing

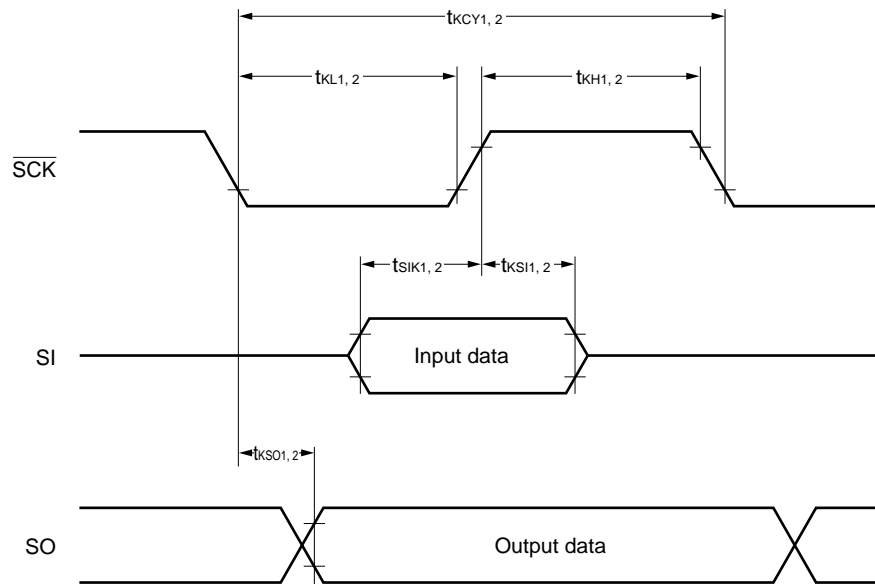


T10, T11 timing

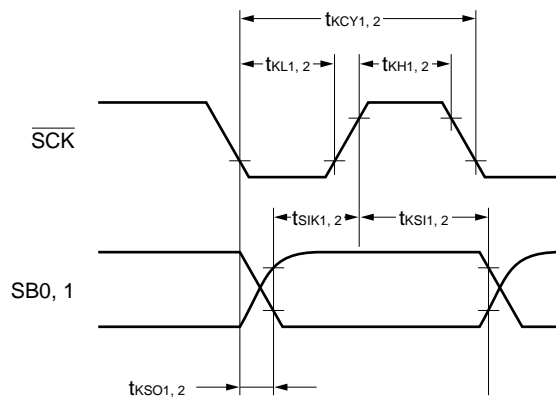


Serial transfer timing

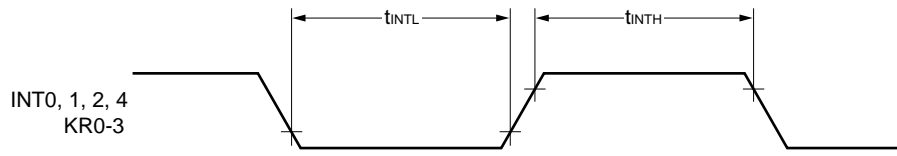
3-wire serial I/O mode



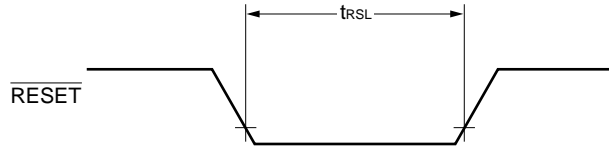
2-wire serial I/O mode



Interrupt input timing



$\overline{\text{RESET}}$ input timing



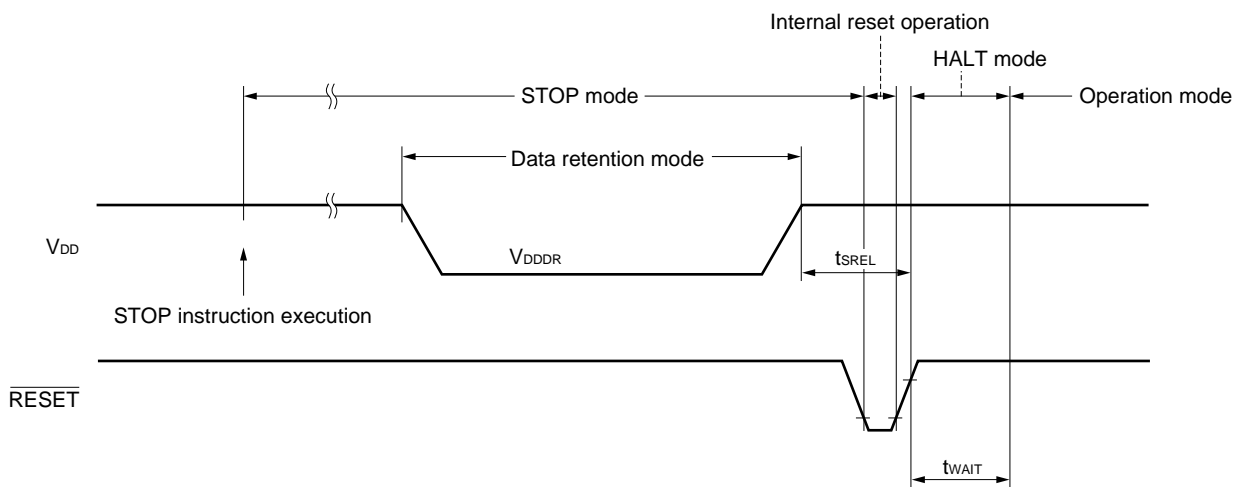
Data retention characteristics of data memory in STOP mode and at low supply voltage
 (T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Release signal setup time	t _{SREL}		0			μs
Oscillation stabilization wait time ^{Note 1}	t _{WAIT}	Released by $\overline{\text{RESET}}$		Note 2		ms
		Released by interrupt request		Note 3		ms

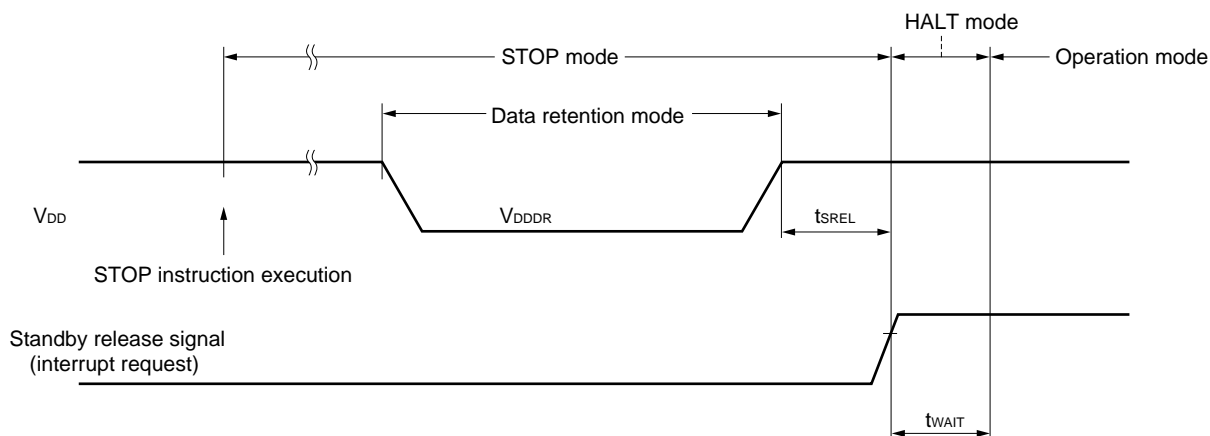
- Notes**
- The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.
 - Either 2¹⁷/f_x or 2¹⁵/f_x can be selected by mask option.
 - Set by the basic interval timer mode register (BTM). (Refer to the table below.)

BTM3	BTM2	BTM1	BTM0	Wait Time	
				f _x = 4.19 MHz	f _x = 6.0 MHz
-	0	0	0	2 ²⁰ /f _x (approx. 250 ms)	2 ²⁰ /f _x (approx. 175 ms)
-	0	1	1	2 ¹⁷ /f _x (approx. 31.3 ms)	2 ¹⁷ /f _x (approx. 21.8 ms)
-	1	0	1	2 ¹⁵ /f _x (approx. 7.81 ms)	2 ¹⁵ /f _x (approx. 5.46 ms)
-	1	1	1	2 ¹³ /f _x (approx. 1.95 ms)	2 ¹³ /f _x (approx. 1.37 ms)

Data retention timing (when STOP mode released by $\overline{\text{RESET}}$)

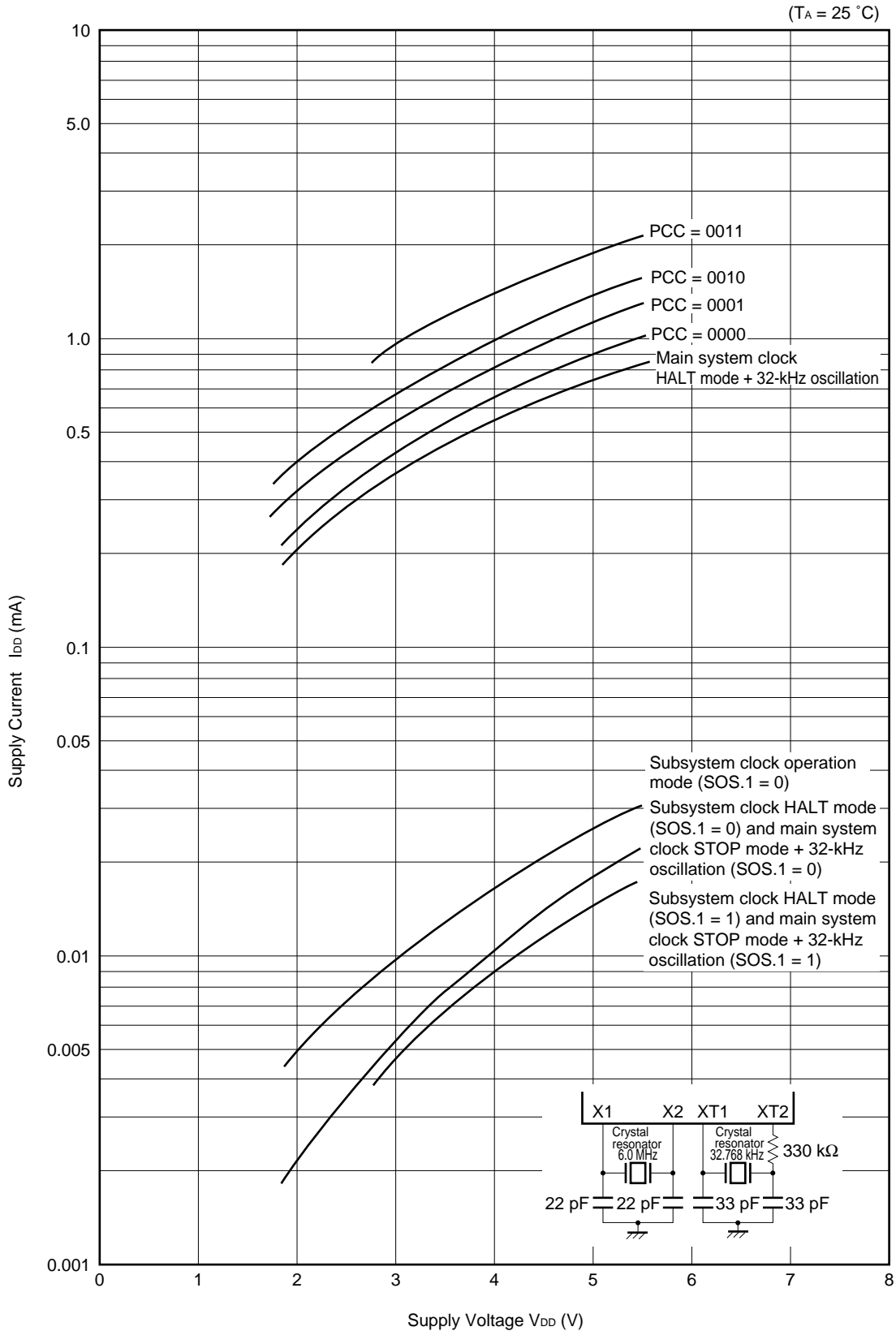


Data retention timing (standby release signal: when STOP mode released by interrupt signal)



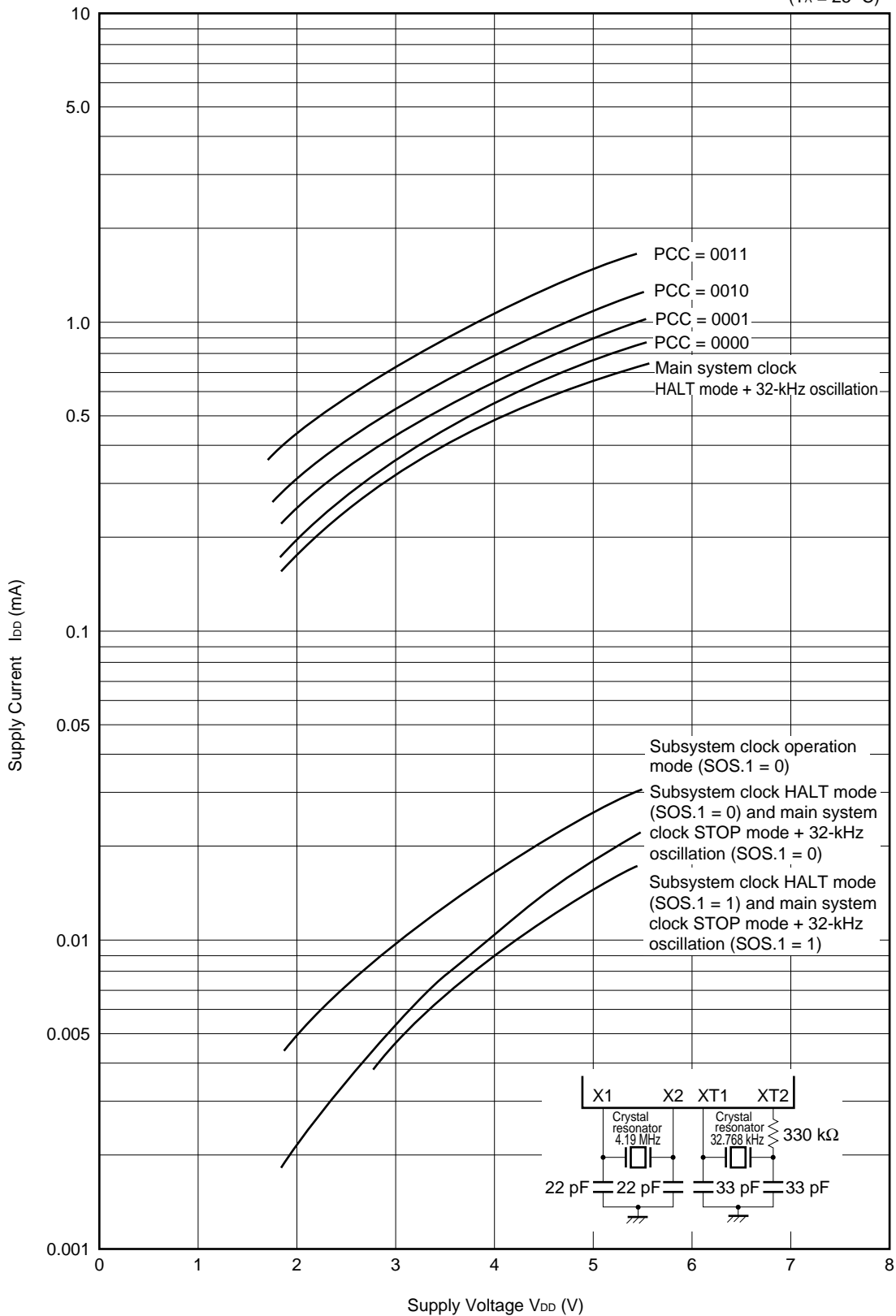
★ 13. CHARACTERISTIC CURVES (FOR REFERENCE ONLY)

I_{DD} vs V_{DD} (main system clock: 6.0-MHz crystal resonator)



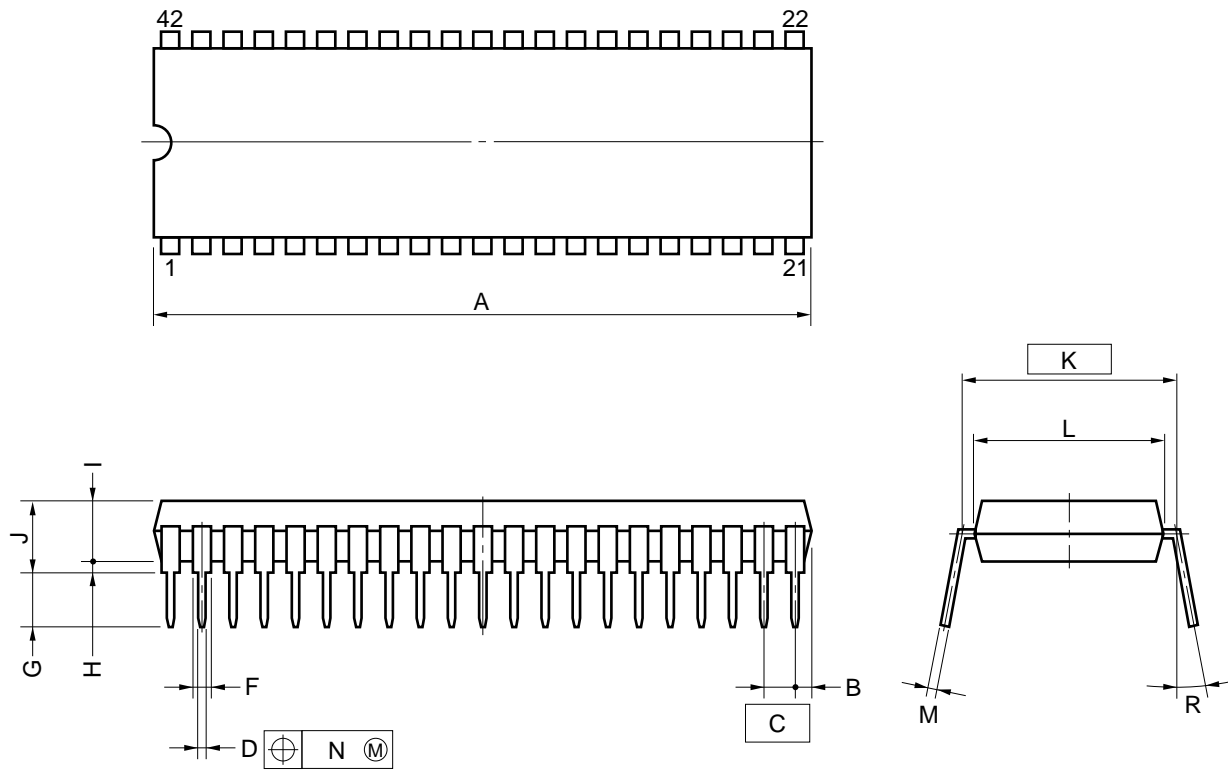
I_{DD} vs V_{DD} (main system clock: 4.19-MHz crystal resonator)

(T_A = 25 °C)



14. PACKAGE DRAWINGS

42 PIN PLASTIC SHRINK DIP (600 mil)



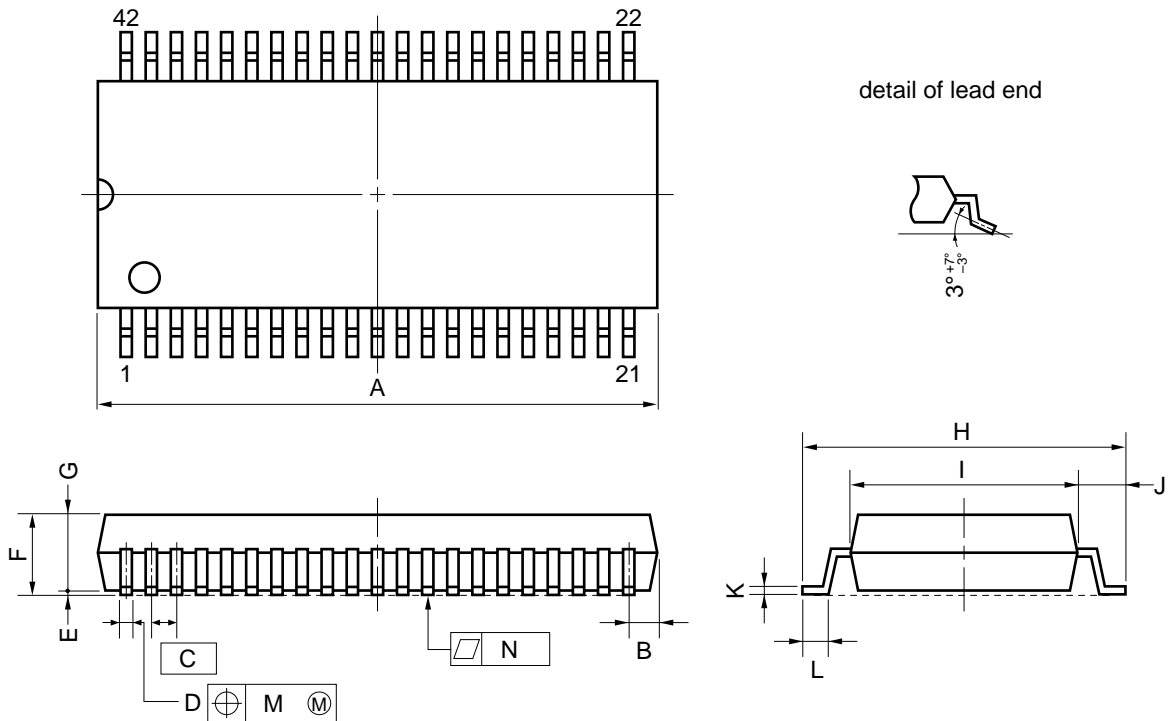
NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0-15°	0-15°

P42C-70-600A-1

42 PIN PLASTIC SHRINK SOP (375 mil)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

S42GT-80-375B-1

ITEM	MILLIMETERS	INCHES
A	18.16 MAX.	0.715 MAX.
B	1.13 MAX.	0.044 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.35 ^{+0.10} _{-0.05}	0.014 ^{+0.004} _{-0.003}
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.5±0.2	0.098 ^{+0.009} _{-0.008}
H	10.3±0.3	0.406 ^{+0.012} _{-0.013}
I	7.15±0.2	0.281 ^{+0.009} _{-0.008}
J	1.6±0.2	0.063±0.008
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.10	0.004
N	0.10	0.004

★ 15. RECOMMENDED SOLDERING CONDITIONS

Solder the μ PD750068 under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and conditions other than those recommended, consult NEC.

Table 15-1. Soldering Conditions of Surface Mount Type

- μ PD750064GT-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)
- μ PD750066GT-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)
- μ PD750068GT-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)
- μ PD750064GT(A)-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)
- μ PD750066GT(A)-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)
- μ PD750068GT(A)-xxx : 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: 2 max.	IR35-00-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: 2 max.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow processes: 1 Preheating temperature: 120 °C or below (package surface temperature)	WS60-00-1
Pin partial heating	Pin temperature: 300 °C or below, Time: 3 seconds or below (per side of device)	—

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 15-2. Soldering Conditions of Through Hole Type

- μ PD750064CU-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
- μ PD750066CU-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
- μ PD750068CU-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
- μ PD750064CU(A)-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
- μ PD750066CU(A)-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
- μ PD750068CU(A)-xxx : 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Pin partial heating	Pin temperature: 300 °C or below, Time: 3 seconds or below (per pin)

Caution In wave soldering, apply solder only to the pins. Care must be taken that jet solder does not come in contact with the main body of the package.

APPENDIX A. μ PD75068, 750068 AND 75P0076 FUNCTIONAL LIST

Parameter		μ PD75068	μ PD750068	μ PD75P0076
Program memory		Mask ROM 0000H-1F7FH (8064 × 8 bits)	Mask ROM 0000H-1FFFH (8192 × 8 bits)	One-time PROM 0000H-3FFFH (16384 × 8 bits)
Data memory		000H-1FFFH (512 × 4 bits)		
CPU		75X Standard CPU	75XL CPU	
General-purpose register		4 bits × 8 or 8 bits × 4	(4 bits × 8 or 8 bits × 4) × 4 banks	
Instruction execution time	When main system clock is selected	0.95, 1.91, 15.3 μ s (during 4.19-MHz operation)	<ul style="list-style-type: none"> • 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation) • 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation) 	
	When subsystem clock is selected	122 μ s (32.768-kHz operation)		
I/O port	CMOS input	12 (on-chip pull-up resistor specified by software: 7)		
	CMOS input/output	12 (on-chip pull-up resistor specified by software)		
	N-ch open-drain input/output	8 (on-chip pull-up resistor specified by mask option) Withstand voltage is 10 V	8 (on-chip pull-up resistor specified by mask option) Withstand voltage is 13 V	8 (no mask option) Withstand voltage is 13 V
	Total	32		
Timer		3 channels <ul style="list-style-type: none"> • 8-bit timer/event counter • 8-bit basic interval timer • Watch timer 	4 channels <ul style="list-style-type: none"> • 8-bit timer/event counter 0 (watch timer output added) • 8-bit timer/event counter 1 (can be used as a 16-bit timer/event counter) • 8-bit basic interval timer/watchdog timer • Watch timer 	
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution × 8 channels (successive approximation) • Can operate at the voltage from $V_{DD} = 2.7$ V 	<ul style="list-style-type: none"> • 8-bit resolution × 8 channels (successive approximation) • Can operate at the voltage from $V_{DD} = 1.8$ V 	

★

Parameter	μ PD75068	μ PD750068	μ PD75P0076
★ ★ Clock output (PCL)	Φ , 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation)	<ul style="list-style-type: none"> Φ, 1.05 MHz, 262 kHz, 65.5 kHz (Main system clock: during 4.19-MHz operation) Φ, 1.5 MHz, 375 kHz, 93.8 kHz (Main system clock: during 6.0-MHz operation) 	
Buzzer output (BUZ)	2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation)	<ul style="list-style-type: none"> 2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation) 2.93, 5.86, 46.9 kHz (Main system clock: during 6.0-MHz operation) 	
Serial interface	3 modes are available <ul style="list-style-type: none"> 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit 2-wire serial I/O mode SBI mode 	2 modes are available <ul style="list-style-type: none"> 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit 2-wire serial I/O mode 	
Vectored interrupt	External: 3, internal: 3	External: 3, internal: 4	
Test input	External: 1, internal: 1		
Supply voltage	$V_{DD} = 2.7$ to 6.0 V	$V_{DD} = 1.8$ to 5.5 V	
Operating ambient temperature	$T_A = -40$ to $+85$ °C		
Package	<ul style="list-style-type: none"> 42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm) 	<ul style="list-style-type: none"> 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch) 	

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μ PD750068.

In the 75XL series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

Language processor

RA75X relocatable assembler	Host machine	OS	Supply media	Part number (product name)
		PC-9800 series	MS-DOS™ (Ver. 3.30 to Ver. 6.2 ^{Note})	
	5-inch 2HD		μ S5A10RA75X	
IBM PC/AT™ and compatible machines	Refer to "OS for IBM PC"	3.5-inch 2HC	μ S7B13RA75X	
		5-inch 2HC	μ S7B10RA75X	

★

Device file	Host machine	OS	Supply media	Part number (product name)
		PC-9800 series	MS-DOS (Ver. 3.30 to Ver. 6.2 ^{Note})	
	5-inch 2HD		μ S5A10DF750068	
IBM PC/AT and compatible machines	Refer to "OS for IBM PC"	3.5-inch 2HC	μ S7B13DF750068	
		5-inch 2HC	μ S7B10DF750068	

★

Note Ver. 5.00 or later has the task swap function, but it cannot be used for this software.

Remark Operation of the assembler and device file is guaranteed only on the above host machines and OSs.

PROM write tools

Hardware	PG-1500	PG-1500 is a PROM programmer which enables you to program single-chip microcontrollers including PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256K bits to 4M bits.			
	PA-75P0076CU	PROM programmer adapter for the μ PD75P0076CU and 75P0076GT. Connect the programmer adapter to PG-1500 for use.			
Software	PG-1500 controller	PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine.			
		Host machine	OS	Supply media	Part number (product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μ S5A13PG1500
			(Ver. 3.30 to Ver. 6.2 ^{Note})	5-inch 2HD	μ S5A10PG1500
		IBM PC/AT and compatible machines	Refer to "OS for IBM PC"	3.5-inch 2HD	μ S7B13PG1500
5-inch 2HC	μ S7B10PG1500				

★

Note Ver. 5.00 or later has the task swap function, but it cannot be used for this software.

Remark Operation of the PG-1500 controller is guaranteed only on the above host machines and OSs.

Debugging tool

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μ PD750068.

The system configurations are described as follows.

Hardware	IE-75000-R ^{Note 1}	In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μ PD750068 subseries, the emulation board IE-75300-R-EM and emulation probe that are sold separately must be used with the IE-75000-R. By connecting with the host machine and the PROM programmer, efficient debugging can be made. It contains the emulation board IE-75000-R-EM which is connected.			
	IE-75001-R	In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μ PD750068 subseries, the emulation board IE-75300-R-EM and emulation probe that are sold separately must be used with the IE-75001-R. It can debug the system efficiently by connecting the host machine and PROM programmer.			
	IE-75300-R-EM	Emulation board for evaluating the application systems that use a μ PD750068 subseries. It must be used with the IE-75000-R or IE-75001-R.			
	EP-750068CU-R	Emulation probe for the μ PD750068CU. It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM.			
	EP-750068GT-R EV-9500GT-42	Emulation probe for the μ PD750068GT. It must be connected to the IE-75000-R (or IE-75001-R) and IE-75300-R-EM. It is supplied with the flexible board EV-9500GT-42 which facilitates connection to a target system.			
Software	IE control program	Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the IE-75000-R or IE-75001-R on a host machine.			
		Host machine	OS	Supply media	Part number (product name)
		PC-9800 series	MS-DOS (Ver. 3.30 to Ver. 6.2 ^{Note 2})	3.5-inch 2HD	μ S5A13IE75X
				5-inch 2HD	μ S5A10IE75X
		IBM PC/AT and compatible machines	Refer to "OS for IBM PC"	3.5-inch 2HC	μ S7B13IE75X
5-inch 2HC	μ S7B10IE75X				



Notes 1. Maintenance product

2. Ver. 5.00 or later has the task swap function, but it cannot be used for this software.

Remarks 1. Operation of the IE control program is guaranteed only on the above host machines and OSs.

2. The μ PD750064, 750066, 750068, and 75P0076 are commonly referred to as the μ PD750068 subseries.

★ OS for IBM PC

The following IBM PC OS's are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.3 J6.1/V ^{Note} to J6.3/V ^{Note}
MS-DOS	Ver. 5.0 to Ver. 6.22 5.0/V ^{Note} to 6.2/V ^{Note}
IBM DOS™	J5.02/V ^{Note}

Note Only English version is supported.

Caution Ver. 5.0 or later has the task swap function, but it cannot be used for this software.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to device

Document Name	Document No.	
	Japanese	English
μ PD750064, 750066, 750068, 750064(A), 750066(A), 750068(A) Data Sheet	U10165J	U10165E (this document)
μ PD75P0076 Data Sheet	U10232J	U10232E ^{Note}
μ PD750068 User's Manual	U10670J	U10670E
μ PD750068 Instruction Table	IEM-5606	–
75XL Series Selection Guide	U10453J	U10453E

Note Preliminary Product Information

Documents related to development tool

Document Name		Document No.		
		Japanese	English	
Hardware	IE-75000-R/IE-75001-R User's Manual	EEU-846	EEU-1416	
	IE-75300-R-EM User's Manual	U11354J	U11354E	
	EP-750068CU/GT-R User's Manual	U10950J	U10950E	
	PG-1500 User's Manual	EEU-651	EEU-1335	
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC-9800 Series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC Series (PC DOS) base	EEU-5008	U10540E

Other related documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	–
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcontroller-Related Product Guide –Third Party Products–	U11416J	–

Caution The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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