# CAN-LDO ASIC                                      TLE 6272

## Target Data Sheet

## 1        Overview

### 1.1        Features

- High speed CAN transceiver for data transmission rate up to 1 Mbaud
- 5V very low drop voltage regulator
- Excellent EMC behaviour
- Very low quiescent current voltage regulator, typ. 65µA
- Separate enable/inhibit input for transceiver and voltage regulator
- Power-on and under-voltage reset
- CAN outputs short circuit proof to ground and battery
- Reverse polarity proof
- Over-temperatur protection
- Over-load and short circuit protected
- Wide temperature range
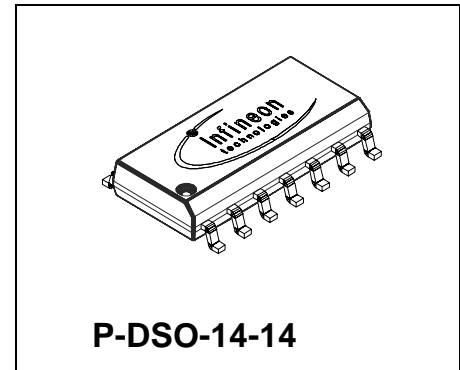


**P-DSO-14-14**

| Type | Ordering Code | Package |
|------|---------------|---------|
| TLE 6272 | on request | P-DSO-14-14 |

### Description

The TLE 6272 is an integration of a high speed CAN-tansceiver functionality together with a low dropout fixed 5V regulator in an enhanced Power P-DSO-14-14 package. The 5V output is designed  loads up to 150 mA.

In addition the device offers a reset circuitry as well as separate mode control inputs for the transceiver and the voltage regulator to minimize power consumption. The power-on delay time of the reset feature can be adjusted via a delay input.

By this the TLE 6272 is optimized to support high speed differential mode data transmission in automotive and industrial applications.

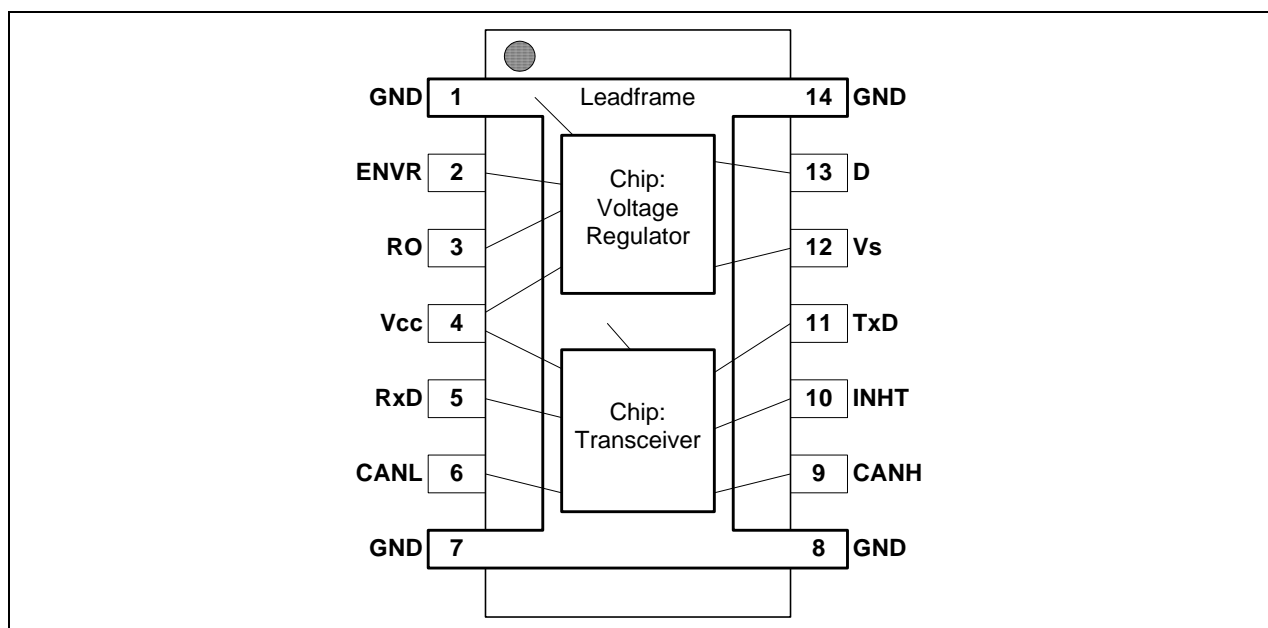The TLE 6272 is designed to withstand the severe conditions of automotive applications.

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## 1.2 Pin Configuration (top view)



**Figure 1**

## 1.3 Pin Definitions and Functions: 5V-version

| Pin No. | Symbol | Function |
|---|---|---|
| 1, 7, 8, 14 | GND | **Ground;** directly connected to chip carrier, place to cooling tabs to improve thermal behaviour |
| 2 | ENVR | **Enable input voltage regulator;** high active, if not needed connect to Vs, 1 MΩ pull down resistor |
| 3 | RO | **Reset output;** open collector output, 20 kΩ pull up |
| 4 | $V_{CC}$ | **5V Output;** connect ot GND with a 22µF capacitor, ESR < 3Ω, |
| 5 | RxD | **CAN receive data output;** LOW in dominant state |
| 6 | CANL | **Low line input;** LOW in dominant state |
| 9 | CANH | **High line output;** HIGH in dominant state |
| 10 | INHT | **Inhibit Transceiver;** 20 kΩ pull up, set LOW for CAN normal mode |
| 11 | TxD | **CAN transmit data input;** 20 kΩ pull up, LOW in dominant state |
| 12 | Vs | **Battery supply input;** block to ground with ceramic capacitor of 100nF |
| 13 | D | **Reset Delay;** to adjust power-on delay time connect to ground via ceramic capacitor |

## 1.4 Functional Block Diagram
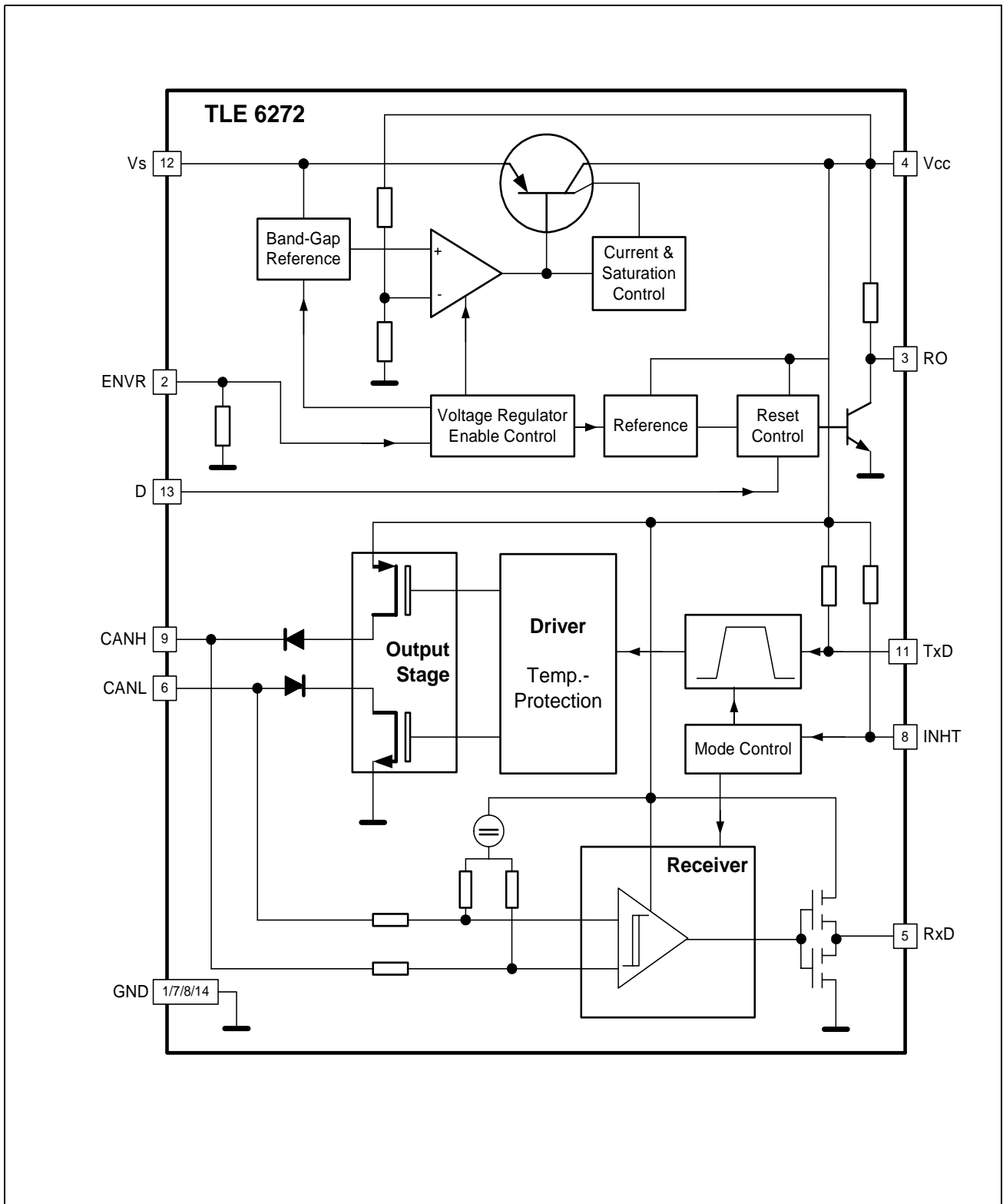


**Figure 2**

## 2        Application Information

The TLE 6272 is a dual chip IC that offers features of the CAN-transceiver TLE 6250 and the voltage regulator TLE 4299 in one package.

The voltage regulator of the TLE 6272 is a PNP based very low drop linear voltage regulator. It regulates the output voltage $V_{CC} = 5V$ at an input voltage range of $5.5V \leq V_S \leq 45V$. The control circuirtry protects the device against damages like overcurrent and overtemperature.

The internal control circuit achieves a 5V output voltage with a tolerance of ± 2%.

The device includes a power-on reset and an under-voltage reset function with adjustable reset delay time. Further there is implemented a separate enable / inhibit function for both, the voltage regulator (including reset circuitry) and the CAN-transceiver. By this the CAN-transceiver circuitry can be switched off to reduce the power consumption while the voltage regulator still supplies other loads. When the voltage regulator is disabled via the ENVR input also the CAN-transceiver is automatically switched off due to the missing supply voltage via $V_{CC}$.

The reset logic compares the output voltage $V_{CC}$ to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor $C_D$ is discharged. When $V_D$ is lower than $V_{st}$, the output reset is switched Low . If the output voltage drop is very short, the $V_{st}$ level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e. g. caused by load changes. Please see figure 3, reset timing diagram.

As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches $V_{DU}$ the reset output RO is set High again. (Reset-hysteresis)

The reset threshold $V_{RT}$ is internally defined (typical 4.65V). The reset delay time is defined by the external capacitor $C_D$ that is charged by a constant current $I_d$ up to a certain threshold $V_{dt}$ during power on phase. Please see figure 3, reset timing diagram.

The reset function is active down to $V_{cc} = 1V$.

When the INHT is low while $V_{CC}$ is present, the CAN-transceiver circuitry is in the normal operation mode. Then messages can be transmitted or received respectively via the RxD and TxD pin. The CAN stand-by mode is a low power mode that disables both, the receiver as well as the transmitter within the CAN-transceiver.

A message sent by the microcontroller to the TxD input is transformed to a differential mode signal and sent to other CAN nodes via the CANH and CANL output. Differential mode data on the bus lines is reported to the microcontroller via the RxD ouput.

**Application description**

The input capacitor $C_{VS}$ compenstates line influences. A resistor of approx. $1\,\Omega$ in series with $C_{VS}$, damps the oscillating circuit of input inductivity and input capacitance. The output capacitor $C_Q$ stabilizes the regulating circuit. Stability is guaranteed at values $C_{VCC} \geq 22\,\mu F$ and an ESR $\leq 3\,\Omega$ within the operating temperature range. Please consider the capacitance-tolerance and temperature coefficient of the reset delay capacitor when calculating the timings.

The reset timing and its calculation is shown in figure 3.

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# 3 Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| **Voltages** | | | | | |
| Supply voltage | $V_S$ | - 40 | 42 | | |
| Output voltage | $V_{CC}$ | - 0.3 | 6.5 | V | |
| Output current | $I_{CC}$ | – 5 | *) | mA | *) internally limited |
| ENVR input voltage | $V_{ENVR}$ | - 40 | 42 | | |
| CAN input voltage (CANH, CANL) | $V_{CANH/L}$ | -20 | 40 | V | |
| Logic voltages at INHT, TxD, RxD, RO, D | $V_I$ | -0.3 | $V_{CC}$ + 0.3 | V | $0 V < V_{CC} < 5.5 V$ |
| Electrostatic discharge voltage at CANH, CANL | $V_{ESD}$ | -4 | 4 | kV | human body model (100 pF via 1.5 kΩ) |
| Electrostatic discharge voltage | $V_{ESD}$ | -2 | 2 | kV | human body model (100 pF via 1.5 kΩ) |
| **Temperatures** | | | | | |
| Junction temperature | $T_j$ | - 40 | 150 | °C | |
| Storage temperature | $T_{Stg}$ | - 50 | 150 | °C | |

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

## 3.2 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply voltage | $V_S$ | 5.5 | 42 | V | |
| Junction temperature | $T_j$ | − 40 | 150 | °C | − |

**Thermal Resistances**

| Junction ambient | $R_{thj\text{-}a}$ | − | 70 | K/W | − |
|---|---|---|---|---|---|

**Thermal Shut Down (junction temperature)**

| Thermal shutdown temp. CAN | $T_{jSD,CAN}$ | 150 | 190 | °C | 10°K hysteresis |
|---|---|---|---|---|---|
| Thermal shutdown temp. voltage regulator | $T_{jSD,VR}$ | 150 | 190 | °C | 10°K hysteresis |

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## 3.3 Electrical Characteristics

$V_S$ = 13.5 V; $R_L$ = 60 Ω; $V_{ENVR} > V_{ENVR,ON}$; $V_{INHT} < V_{INHT,ON}$; −40 °C < $T_j$ < 125 °C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |

**Current Consumption**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Current consumption $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | | 6 | 10 | mA | $I_{CC} \leq$ 1mA; CAN recessive state; $V_{TxD} = V_{CC}$ |
| Current consumption $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | | 45 | 70 | mA | $I_{CC} \leq$ 1mA; CAN dominant state; $V_{TxD} = 0V$ |
| Current consumption $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | | | 100 | μA | $V_{INHT} > V_{INHT,off}$ $I_{CC} \leq$ 1mA; Tj < 85°C |
| Current consumption; $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | − | 250 | 700 | μA | $V_{INHT} > V_{INHT,off}$ $I_{CC}$ = 10mA |
| Current consumption; $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | − | 2 | 8 | mA | $V_{INHT} > V_{INHT,off}$ $I_{CC}$ = 50mA |
| Current consumption; $(I_q+I_{TR}) = I_S - I_{LOAD}$ | $I_q+I_{TR}$ | | | 15 | μA | $V_{ENVR} < V_{ENVR,off}$ Tj < 85°C |

**Voltage Regulator**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Output voltage | $V_{CC}$ | 4.90 | 5.00 | 5.10 | V | 1mA ≤ $I_{CC}$ ≤ 100mA 6V ≤ $V_S$ ≤ 16V |
| Current limit | $I_{CC}$ | 150 | 200 | 500 | mA | $I_{CC} = I_{TR} + I_{LOAD}$ |
| Drop voltage | $V_{dr}$ | − | 0.25 | 0.5 | V | $I_{CC}$ = 100mA *) |
| Load regulation | $\Delta V_{CC}$ | − | 10 | 30 | mV | 1mA ≤ $I_{CC}$ ≤ 100mA |
| Line regulation | $\Delta V_{CC}$ | − | 10 | 40 | mV | $V_S$ = 6V to 26V $I_{CC}$ = 1mA |
| Power Supply Ripple rejection | $PSRR$ | − | 50 | − | dB | fr= 100Hz; Vr = 0,5 $V_{PP}$; guaranteed by design |

*) Drop voltage = $V_S - V_{CC}$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.)

## 3.3    Electrical Characteristics (cont'd)

$V_S$ = 13.5 V; $R_L$ = 60 Ω; $V_{ENVR}$ > $V_{ENVR,ON}$; $V_{INHT}$ < $V_{INHT,ON}$; −40 °C < $T_j$ < 125 °C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |

**Enable Voltage Regulator ENVR**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Enable VR OFF voltage | $V_{ENVR,off}$ | | | 1.5 | V | |
| Enable VR ON voltage | $V_{ENVR,on}$ | 4.0 | | | V | |
| Pull down resistor | $R_{ENVR}$ | 0.8 | 1 | 1.2 | MΩ | |

**Reset Generator**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Switching threshold | $V_{rt}$ | 4.50 | 4.65 | 4.80 | V | |
| Reset pull up | $R_{RO}$ | 10 | 20 | 40 | kΩ | |
| Reset low voltage | $V_R$ | – | 0.1 | 0.4 | V | $V_{CC}$ < 4.5V, |
| Reset current | $I_R$ | | tbd | | µA | $V_{RO(Low)}$ < 400 mV, Reset operational down to 1V |
| Delay switching threshold | $V_{dt}$ | 1.4 | 1.8 | 2.2 | V | |
| Switching threshold | $V_{st}$ | 0.3 | 0.45 | 0.60 | V | |
| Reset delay low voltage | $V_D$ | – | | 0.1 | V | $V_{CC}$ < $V_{RT}$ |
| Charge current | $I_d$ | 3.0 | 6.5 | 9.5 | µA | $V_D$ = 1V |
| Delay time L → H | $t_d$ | 17 | 28 | – | ms | $C_D$ = 100nF |
| Delay time H → L | $t_{rr}$ | – | 1 | – | µs | $C_D$ = 100nF |
| Switching voltage | $V_{re}$ | 1.26 | 1.35 | 1.44 | V | $V_{CC}$ > 3.5V |

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## 3.3 Electrical Characteristics (cont'd)

$V_S = 13.5$ V; $R_L = 60$ Ω; $V_{ENVR} > V_{ENVR,ON}$; $V_{INHT} < V_{INHT,ON}$; $-40$ °C $< T_j < 125$ °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |

**CAN-Transceiver**

**Receiver Output R×D**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| HIGH level output current | $I_{RD,H}$ | | -300 | | µA | $V_{RD} > 0.8$ x $V_{CC}$, $V_{diff} < 0.4$ V *) |
| LOW level output current | $I_{RD,L}$ | | 1 | 2 | mA | $V_{RD} < 0.2$ x $V_{CC}$, $V_{diff} > 1$V *) |

**Bus receiver**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Differential receiver threshold voltage, recessive to dominant edge | $V_{diff,d}$ | | 0.8 | 0.9 | V | $-20$V $< (V_{CANH}, V_{CANL}) < 25$V $V_{diff} = V_{CANH} - V_{CANL}$ |
| Differential receiver threshold voltage dominant to recessive edge | $V_{diff,r}$ | 0.5 | 0.6 | | V | $-20$V $< (V_{CANH}, V_{CANL}) < 25$V $V_{diff} = V_{CANH} - V_{CANL}$ |
| Differential receiver hysteresis | $V_{diff,hys}$ | | 200 | | mV | |
| CANH, CANL input resistance | $R_i$ | | 20 | | kΩ | recessive state |
| Differential input resistance | $R_{diff}$ | | 40 | | kΩ | recessive state |

**Transmission Input T×D**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| HIGH level input voltage threshold | $V_{TD,H}$ | | 2.5 | 3.5 | V | recessive state; |
| TxD input hysteresis | $V_{TD,hys}$ | | 100 | | mV | |
| LOW level input voltage threshold | $V_{TD,L}$ | 1.5 | 2.4 | | V | dominant state |
| HIGH level input current | $I_{TD}$ | -60 | -20 | - | µA | $V_{TxD} = V_{CC}$ |
| TxD pull up resistance | $R_{TD}$ | 10 | 20 | 30 | kΩ | |

## 3.3 Electrical Characteristics (cont'd)

$V_S$ = 13.5 V; $R_L$ = 60 Ω; $V_{ENVR}$ > $V_{ENVR,ON}$; $V_{INHT}$ < $V_{INHT,ON}$; −40 °C < $T_j$ < 125 °C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |

**Bus transmitter**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| CANL/CANH recessive output voltage | $V_{CANL/H}$ | 0.4x $V_{CC}$ | | 0.6x $V_{CC}$ | V | $V_{TxD}$ = $V_{CC}$ |
| CANH, CANL recessive output voltage difference $V_{diff}$ = $V_{CANH}$ - $V_{CANL}$ | $V_{diff}$ | −500 | | 50 | mV | $V_{TxD}$ = $V_{CC}$; no load |
| CANL dominant output voltage | $V_{CANL}$ | | | 1.8 | V | $V_{TxD}$ = 0V; |
| CANH dominant output voltage | $V_{CANH}$ | 2.8 | | | V | $V_{TxD}$ = 0V |
| CANH, CANL dominant output voltage difference $V_{diff}$ = $V_{CANH}$ - $V_{CANL}$ | $V_{diff}$ | 1.5 | | 3.0 | V | $V_{TxD}$ = 0V; |
| CANL short circuit current | $I_{CANLsc}$ | 50 | 100 | | mA | $V_{CANLshort}$ = 18V |
| | | | 150 | | mA | $V_{CANLshort}$ = 36V |
| CANH short circuit current | $I_{CANHsc}$ | | -110 | -50 | mA | $V_{CANHshort}$ = 0V |
| | | | -120 | | mA | $V_{CANHshort}$ = - 5V |
| Leakage current | $I_{CANH,lk}$ $I_{CANL,lk}$ | | -80 | | µA | $V_{CC}$ = 0V, $V_{CANH}$ = $V_{CANL}$ = -2V $T_j$ < 85°C |
| Leakage current | $I_{CANH,lk}$ $I_{CANL,lk}$ | | 280 | | µA | $V_{CC}$ = 0V, $V_{CANH}$ = $V_{CANL}$ = 7V $T_j$ < 85°C |

**Inhibit transceiver input INHT**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| HIGH level input voltage threshold | $V_{INHT,H}$ | | 2.5 | 3.5 | V | CAN stand-by mode; |
| LOW level input voltage threshold | $V_{INHT,L}$ | 1.5 | 2.4 | | V | CAN normal mode |
| HIGH level input current | $I_{INHT}$ | -60 | -20 | - | µA | $V_{INHT}$ = $V_{CC}$ |
| INHT pull up resistance | $R_{INHT}$ | 10 | 20 | 30 | kΩ | |

### 3.3    Electrical Characteristics (cont'd)

$V_S$ = 13.5 V; $R_L$ = 60 Ω;  $V_{ENVR}$ > $V_{ENVR,ON}$;  $V_{INHT}$ < $V_{INHT,ON}$; −40 °C < $T_j$ < 125 °C;
all voltages with respect to ground; positive current flowing into pin;  unless otherwise specified.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |

**Dynamic CAN-Transceiver Characteristics**

| Parameter | Symbol | min. | typ. | max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Propagation delay TxD-to-RxD LOW (recessive to dominant) | $t_{d(L),TR}$ | | 150 | 280 | ns | $C_L$ = 47pF; $R_L$ = 60Ω; $C_{RxD}$ = 20pF |
| Propagation delay TxD-to-RxD HIGH (dominant to recessive) | $t_{d(H),TR}$ | | 150 | 280 | ns | $C_L$ = 47pF; $R_L$ = 60Ω; $C_{RxD}$ = 20pF |
| Propagation delay TxD LOW to bus dominant | $t_{d(L),T}$ | | 100 | | ns | $C_L$ = 47pF; $R_L$ = 60Ω; |
| Propagation delay TxD HIGH to bus recessive | $t_{d(H),T}$ | | 100 | | ns | $C_L$ = 47pF; $R_L$ = 60Ω; |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | | 50 | | ns | $C_L$ = 47pF; $R_L$ = 60 Ω; $C_{RxD}$ = 20pF |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | | 50 | | ns | $C_L$ = 47pF; $R_L$ = 60Ω; $C_{RxD}$ = 20pF |

# 4 Diagrams
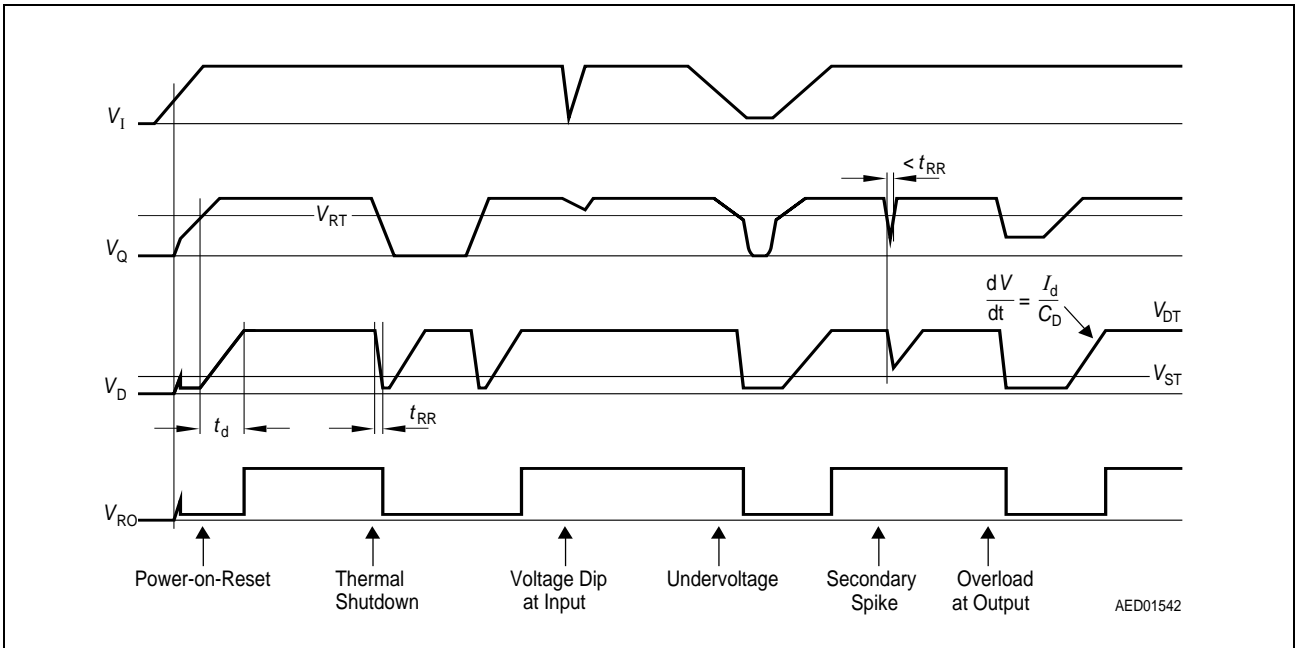


**Figure 3: reset timing diagram**
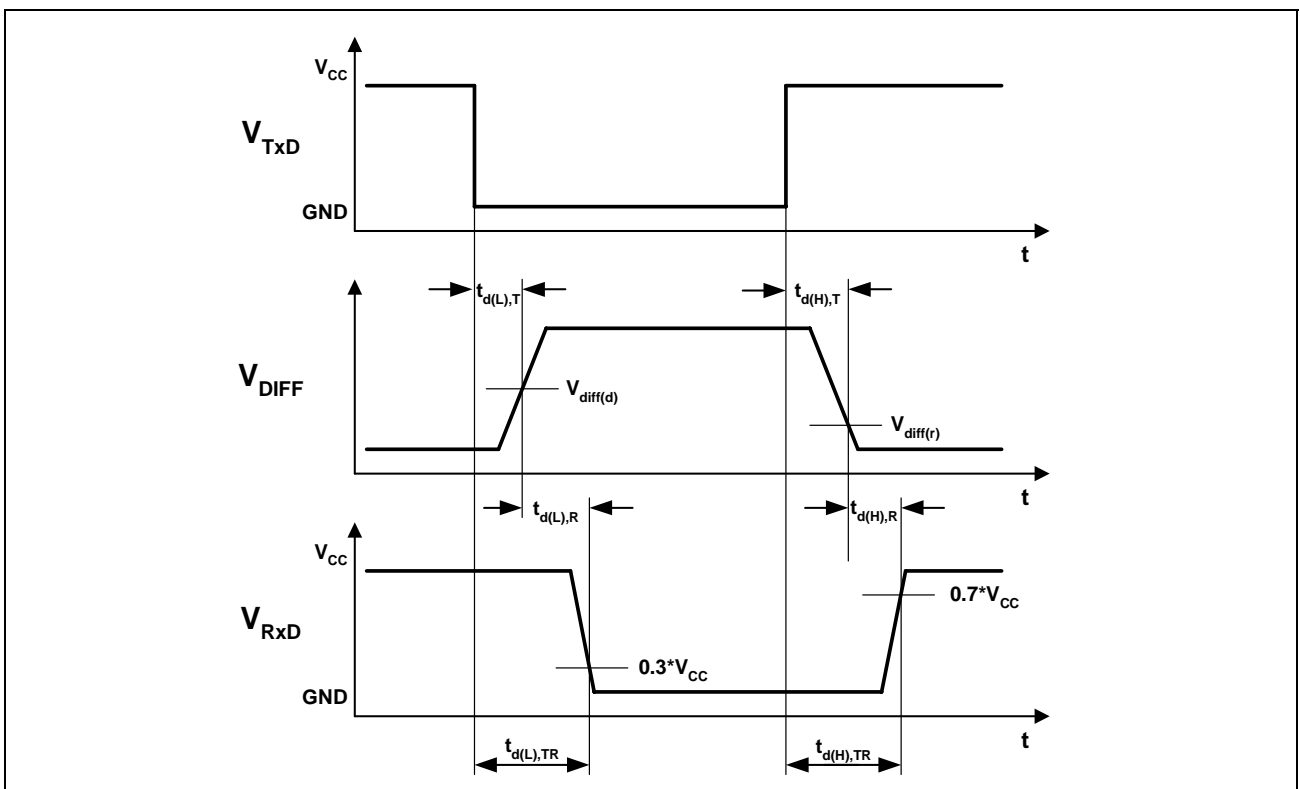


**Figure 4: Timing diagrams for dynamic characteristics**

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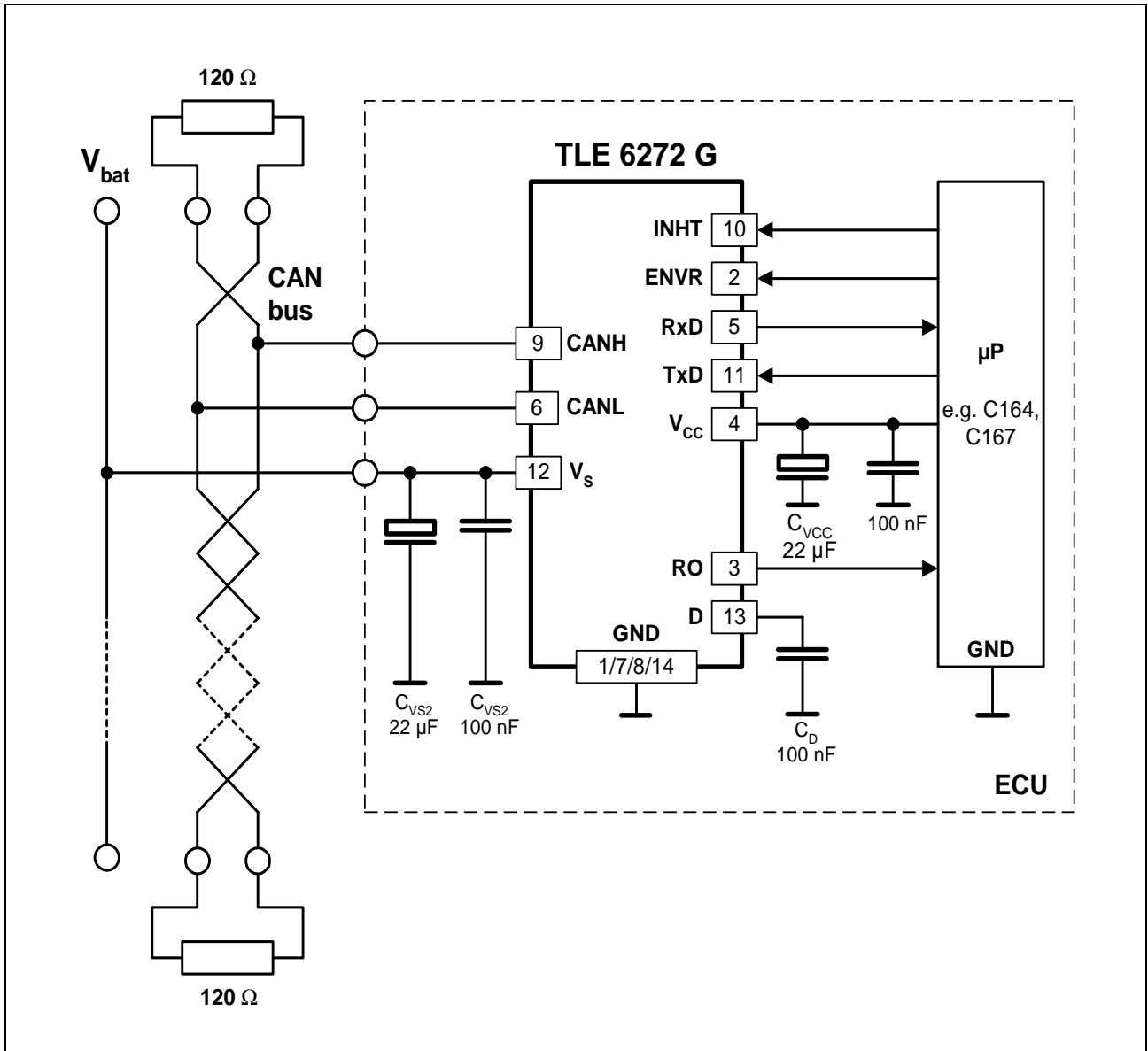
# 5    Application



**Figure 5**
**Application Circuit**

## 6 Package Outlines

**P-DSO-14-14**
(Plastic Dual Small Outline Package)



0.33 ±0.08 x45°

4 -0.2 1)

0.1 MIN.

(1.5)

1.75 MAX.

0.2 +0.05 -0.01

8° MAX.

1.27

0.41 +0.1 -0.06

⌖ 0.2 Ⓜ A C  14x

◠ 0.1

C

0.64 ±0.25

6 ±0.2

14    8

1    7

8.75 -0.2 1)

A
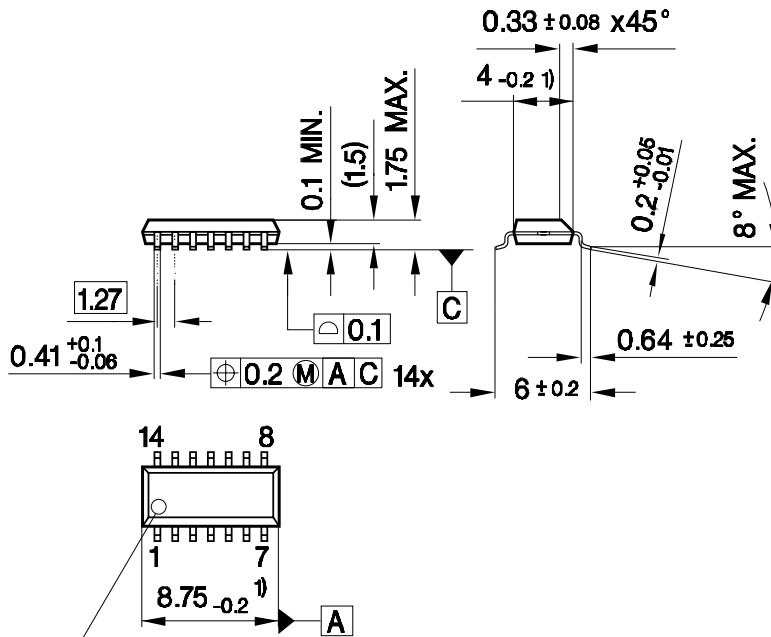
Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information".

SMD = Surface MountedDevice

Dimensions in mm