

# Am2916A

Quad Three-State Bus Transceiver with Interface Logic

## DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Two-port input to D-type register on driver
- Three-state bus driver output can sink 48mA at 0.5V max.
- Internal 4-bit odd parity checker/generator
- Receiver output latch can sink 12mA
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

## GENERAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ( $\overline{BE}$ ) is used to force the driver outputs to the high-impedance state. When  $\overline{BE}$  is HIGH, the driver is disabled.

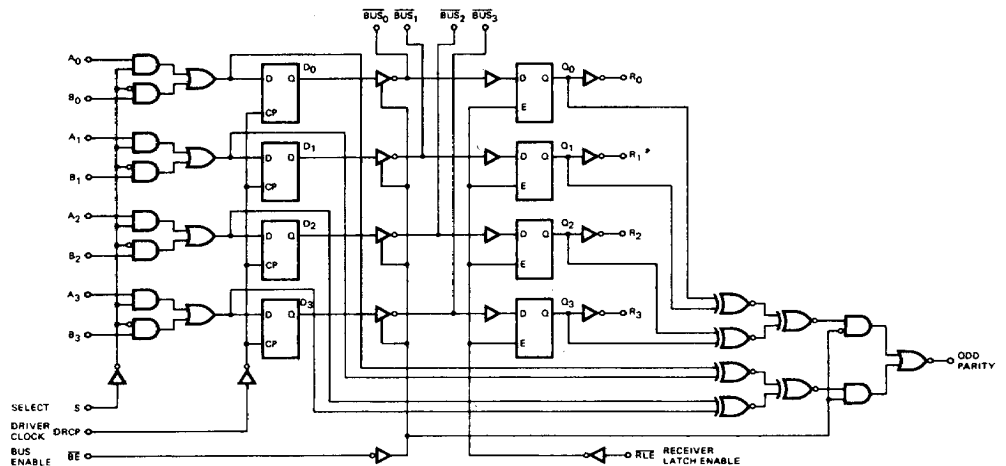
The input register consists of four D-type flip-flops with a buffered common clock and two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the  $A_i$  data is stored in the register and when S is HIGH, the  $B_i$  data is stored.

The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (RLE) input. When the RLE input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the RLE input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ( $\overline{BE}$ ) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When  $\overline{BE}$  is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, odd parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

## BLOCK DIAGRAM

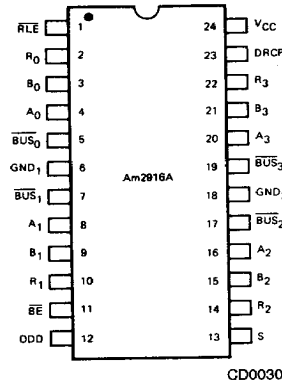


BD001600

05402A

### CONNECTION DIAGRAM Top View

D-24-1

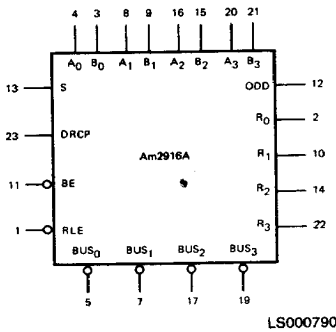


CD003020

Note: Pin 1 is marked for orientation

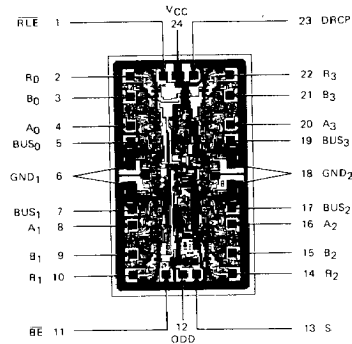
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### LOGIC SYMBOL



LS000790

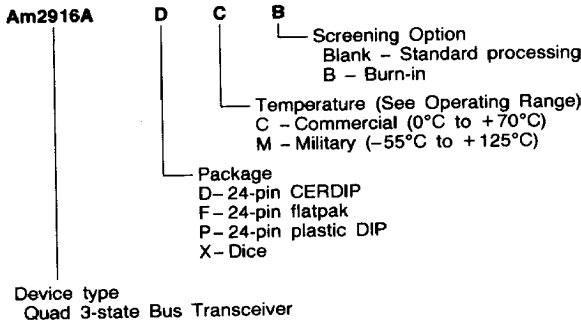
### METALLIZATION AND PAD LAYOUT



DIE SIZE .074" x .130"

### ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am2916A	PC DC, DCB, DM, DMB FM, FMB XC, XM

**Valid Combinations**  
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

Pin No.	Name	I/O	Description
4, 8, 16, 20	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub>	I	The "A" word data input into the two input multiplexer of the driver register.
3, 9, 15, 21	B <sub>0</sub> , B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub>	I	The "B" word data input into the two input multiplexers of the driver register.
13	S	I	Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.
23	DRCP	I	Driver Clock Pulse. Clock pulse for the driver register.
11	BE	I	Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high-impedance state.
5, 7, 17, 19	BUS <sub>0</sub> , BUS <sub>1</sub> , BUS <sub>2</sub> , BUS <sub>3</sub>	I/O	The four driver outputs and receiver inputs (data is inverted).
2, 10, 14, 22	R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub>	O	The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.
1	RLE	O	Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.
12	ODD	O	Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

## FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUTS			FUNCTION
S	A <sub>i</sub>	B <sub>i</sub>	DRCP	BE	RLE	D <sub>i</sub>	Q <sub>i</sub>	BUS <sub>i</sub>	R <sub>i</sub>	ODD		
X	X	X	X	H	X	X	X	Z	X	PQ	Driver output disable	
X	X	X	X		X	X	X	X	X	PD	Driver output enable	
X	X	X	X	H	L	X	L	L	H	H	Driver output disable and receive data via Bus input	
X	X	X	X	H	L	X	H	H	L	H		
X	X	X	X	X	H	X	NC	X	NC	X	Latch received data	
L	L	X	1	X	X	L	X	X	X	X	Load driver register	
L	H	X	1	X	X	H	X	X	X	X		
H	X	L	1	X	X	L	X	X	X	X		
H	X	H	1	X	X	H	X	X	X	X		
X	X	X	L	X	X	NC	X	X	X	X	No driver clock restrictions	
X	X	X	H	X	X	NC	X	X	X	X		
X	X	X	X	L	X	L	X	H	X	H	Drive Bus	
X	X	X	X	L	X	H	X	L	X	H		

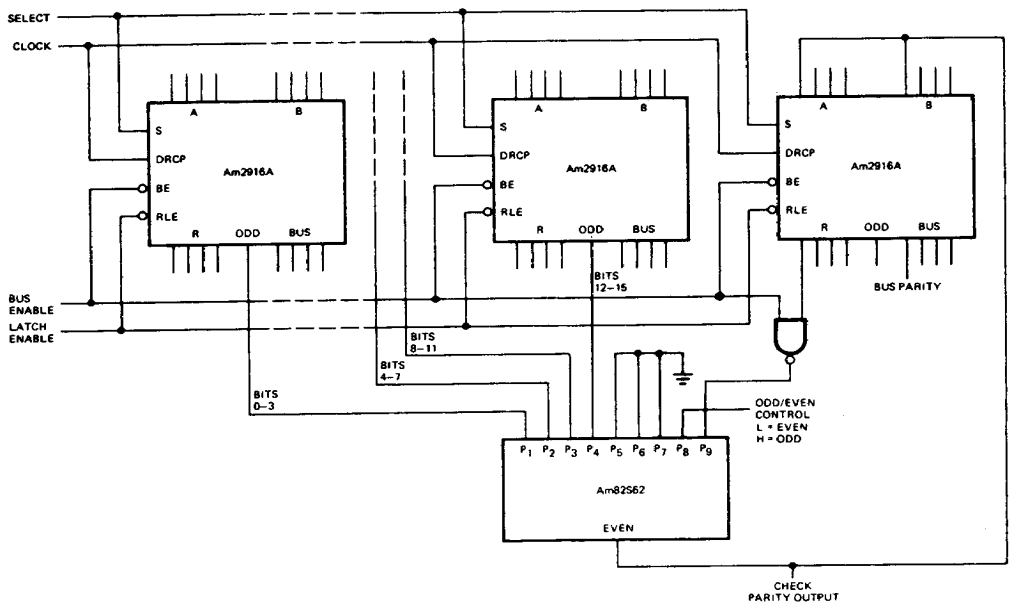
H = HIGH      Z = HIGH Impedance      X = Don't care      i = 0, 1, 2, 3  
L = LOW      NC = No change      1 = LOW to HIGH transition  
PQ=Parity of Q latches  
PD=Parity of D flip-flops

## PARITY OUTPUT FUNCTION TABLE

BE	ODD PARITY OUTPUT
L	ODD = I <sub>0</sub> ⊕ I <sub>1</sub> ⊕ I <sub>2</sub> ⊕ I <sub>3</sub>
H	ODD = Q <sub>0</sub> ⊕ Q <sub>1</sub> ⊕ Q <sub>2</sub> ⊕ Q <sub>3</sub>

I<sub>i</sub> = Selected input A<sub>i</sub> or B<sub>i</sub>

### APPLICATIONS



AF000990

Generating or checking parity for 16 data bits.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65°C to +150°C
(Ambient) Temperature Under Bias .....	-55°C to +125°C
Supply Voltage to Ground Potential Continuous .....	-0.5V to +7.0V
DC Voltage Applied to Outputs For High Output State .....	-0.5V to $V_{CC}$ max
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current, Into Outputs (Except Bus) .....	30mA
DC Output Current, Into Bus .....	100mA
DC Input Current .....	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES****Commercial (C) Devices**

Temperature .....	0°C to +70°C
Supply Voltage .....	+4.75V to +5.25V

**Military (M) Devices**

Temperature .....	-55°C to +125°C
Supply Voltage .....	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified

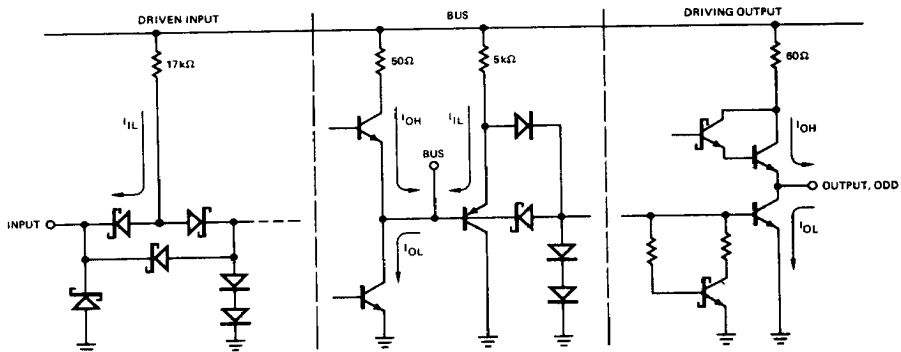
Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units	
$V_{OH}$	Receiver Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IL}$ or $V_{IH}$	MIL: $I_{OH} = -1.0\text{mA}$	2.4	3.4	Volts	
			COM'L: $I_{OH} = -2.6\text{mA}$	2.4	3.4		
		$V_{CC} = 5.0\text{V}$ , $I_{OH} = -100\mu\text{A}$		3.5			
$V_{OH}$	Parity Output HIGH Voltage	$V_{CC} = \text{MIN}$ , $I_{OH} = -660\mu\text{A}$ $V_{IN} = V_{IH}$ or $V_{IL}$	MIL	2.5	3.4	Volts	
			COM'L	2.7	3.4		
$V_{OL}$	Output LOW Voltage (Except Bus)	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IL}$ or $V_{IH}$	$I_{OL} = 4.0\text{mA}$	0.27	0.4	Volts	
			$I_{OL} = 8.0\text{mA}$		0.32		0.45
			$I_{OL} = 12\text{mA}$		0.37		0.5
$V_{IH}$	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs	2.0			Volts	
$V_{IL}$	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL		0.7	Volts	
			COM'L				0.8
$V_I$	Input Clamp Voltage (Except Bus)	$V_{CC} = \text{MIN}$ , $I_{IN} = -18\text{mA}$			-1.2	Volts	
$I_{IL}$	Input LOW Current (Except Bus)	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4\text{V}$	BE, RLE		-0.72	mA	
			All other inputs		-0.36		
$I_{IH}$	Input HIGH Current (Except Bus)	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7\text{V}$			20	$\mu\text{A}$	
$I_I$	Input HIGH Current (Except Bus)	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0\text{V}$			100	$\mu\text{A}$	
$I_{SC}$	Output Short Circuit Current (Except Bus)	$V_{CC} = \text{MAX}$	RECEIVER	-30	-130	mA	
			PARITY	-20	-100		
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX}$ , All inputs = GND		75	110	mA	

- Notes:
1. Typical limits are at  $V_{CC} = 5.0\text{V}$ , 25°C ambient and maximum loading.
  2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
  3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

**BUS INPUT/OUTPUT CHARACTERISTICS** over operating temperature range

Parameters	Description	Test Conditions (Note 1)		Min	Typ	Max.	Units
VOL	Bus Output LOW Voltage	V <sub>CC</sub> = MIN	I <sub>OL</sub> = 24mA			0.4	Volts
			I <sub>OL</sub> = 48mA			0.5	
VOH	Bus Output HIGH Voltage	V <sub>CC</sub> = MIN	COM'L, I <sub>OH</sub> = -20mA MIL, I <sub>OH</sub> = -15mA	2.4			Volts
I <sub>O</sub>	Bus Leakage Current (High Impedance)	V <sub>CC</sub> = MAX Bus enable = 2.4V	V <sub>O</sub> = 0.4V			-200	μA
			V <sub>O</sub> = 2.4V			50	
			V <sub>O</sub> = 4.5V			100	
I <sub>OFF</sub>	Bus Leakage Current (Power OFF)	V <sub>O</sub> = 4.5V V <sub>CC</sub> = 0V				100	μA
V <sub>IH</sub>	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V <sub>IL</sub>	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I <sub>SC</sub>	Bus Output Short Circuit Current	V <sub>CC</sub> = MAX V <sub>O</sub> = 0V		-50	-120	-225	mA

**INPUT/OUTPUT CURRENT INTERFACE CONDITIONS**



IC000460

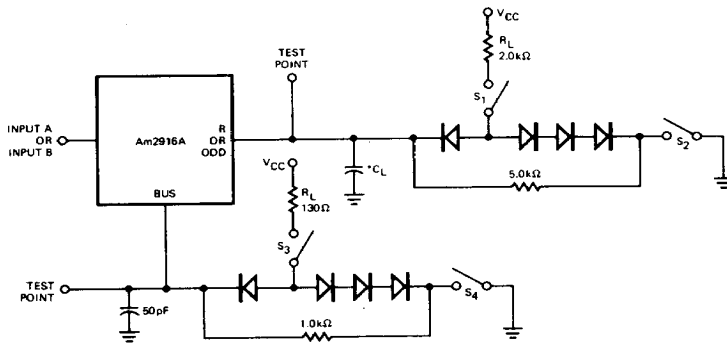
Note: Actual current flow direction shown.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions	COMMERCIAL			MILITARY			Units
			Am2916A			Am2916A			
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
$t_{PHL}$	Driver Clock (DRCP) to Bus	$C_L$ (BUS) = 50 pF $R_L$ (BUS) = 130 $\Omega$		21	32		21	36	ns
$t_{PLH}$				21	32		21	36	
$t_{ZH}, t_{ZL}$	Bus Enable ( $\overline{BE}$ ) to Bus			13	23		13	26	ns
$t_{HZ}, t_{LZ}$				13	18		13	21	
$t_s$	Data Inputs (A or B)			12			15		ns
$t_h$				6.0			8.0		
$t_s$	Select Inputs (S)			25			28		ns
$t_h$				6.0			8.0		
$t_{pw}$	Clock Pulse Width (HIGH)			17			20		ns
$t_{PLH}$	Bus to Receiver Output (Latch Enabled)				18	30		18	33
$t_{PHL}$				18	27		18	30	
$t_{PLH}$	Latch Enable to Receiver Output			21	30		21	33	ns
$t_{PHL}$				21	27		21	30	
$t_s$	Bus to Latch Enable ( $\overline{LE}$ )		13			15		ns	
$t_h$			4.0			6.0			
$t_{PLH}$	A or B Data to Odd Parity Output (Driver Enabled)			32	42		32	46	ns
$t_{PHL}$				26	36		26	40	
$t_{PLH}$	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	32		21	36	ns
$t_{PHL}$				21	32		21	36	
$t_{PLH}$	Latch Enable ( $\overline{LE}$ ) to Odd Parity Output			21	32		21	36	ns
$t_{PHL}$				21	32		21	36	

- Notes:
1. Typical limits are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading.
  2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
  3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

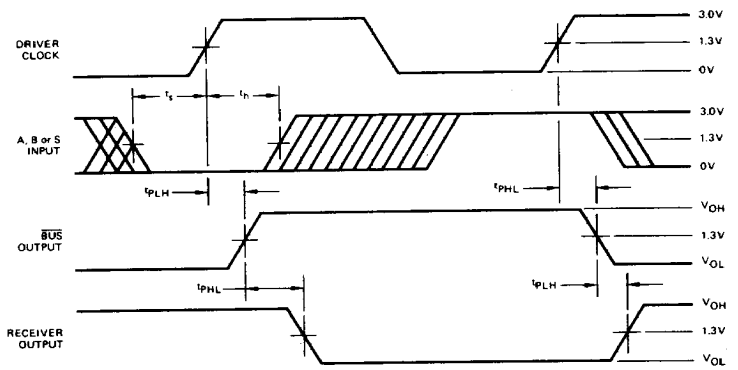
### SWITCHING TEST CIRCUIT



TC000890

\* $C_L$  = 15pF for t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>ZL</sub>, t<sub>ZH</sub>  
 $C_L$  = 5pF for t<sub>HZ</sub>, t<sub>LZ</sub>

### SWITCHING WAVEFORMS



WF002281

Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.