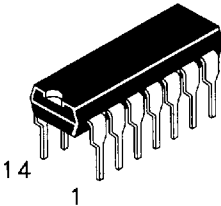


Hex Inverter with Open-Drain Outputs

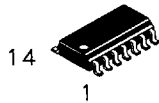
This device contains six independent gates, each of which performs the logic INVERT function. The open-drain outputs require external pull-up resistors for proper logical operation. They may be connected to other open-drain outputs to implement active-high wired-AND functions,

- **Output Drive Capability:** 10 LSTTL Loads
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range:** 2 to 6 V
- **Low Input Current:** 1 μ A
- **DC, AC parameters guaranteed from -55°C to 125°C**

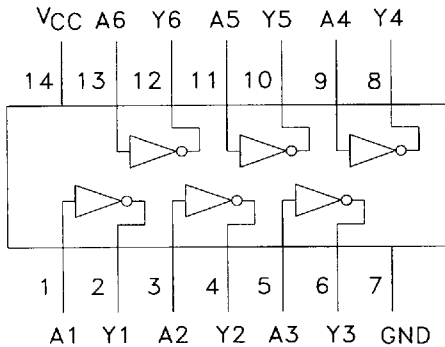
DV74HC05A



N Suffix
Plastic DIP
AVG-001 Case



D Suffix
Plastic SOP
AVG-002 Case



TRUTH TABLE
Y = A

Inputs	Outputs
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	± 20	mA
I _{OUT}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic DIP SOP Package	750 500	mW
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1mm from Case for 10 Seconds (Plastic DIP or Sop Package)	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Ambient Temperature	-55	+125	°C
t _r , t _f	Input Rise and Fall Time	0	1000	ns
	V _{CC} =2.0V	0	500	
	V _{CC} =4.0V	0	400	
	V _{CC} =6.0V	0	400	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} V	Guaranteed Limits			Unit
				25°C to -55°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or = V _{CC} - 0.1 V I _{OUT} = 0 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or = V _{CC} - 0.1 V I _{OUT} = 0 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (Per Package)	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	1	10	40	μA
I _{oz}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA

AC ELECTRICAL CHARACTERISTICS over full operating conditions (CL=50pF, Input t_f=tr=6ns, RL=1kΩ)

Symbol	Parameter	V _{CC} V	Guaranteed Limits			Unit
			25°C to -55°C	≤85°C	≤125°C	
t _{PLZ} , t _{PZL}	Maximum Propagation Delay Time, Input A or B To Output Y	2.0 4.5 6.0	125 24 20	150 30 26	180 36 31	ns
t _{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{IN}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption PD = CPD VCC²f + ICC VCC	Typical @ 25°C, VCC = 5 V		pF
		8		

SWITCHING WAVEFORMS (Input Threshold Voltage, V_T=50% V_{CC}, V_H=V_{CC})

