Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver with LSTTL-Compatible Inputs

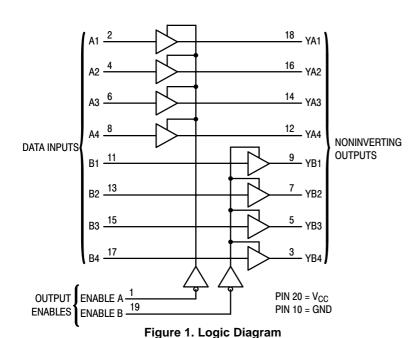
High-Performance Silicon-Gate CMOS

The MC74HCT244A is identical in pinout to the LS244. This device may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs. The HCT244A is an octal noninverting buffer line driver line receiver designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. The device has non–inverted outputs and two active–low output enables.

The HCT244A is the non-inverting version of the HCT240. See also HCT241.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 112 FETs or 28 Equivalent Gates
- Pb-Free Packages are Available





ON Semiconductor®

http://onsemi.com



PDIP-20 N SUFFIX CASE 738



SOIC-20W DW SUFFIX CASE 751D



TSSOP-20 DT SUFFIX CASE 948E



SOEIAJ-20 M SUFFIX CASE 967

PIN ASSIGNMENT

ENABLE A	1●	20] v _{cc}
A1 [2	19	ENABLE B
YB4 [3	18] YA1
A2 [4	17] B4
YB3 [5	16] YA2
A3 [6	15] B3
YB2 [7	14] YA3
A4 [8	13] B2
YB1 [9	12] YA4
GND [10	11] B1

FUNCTION TABLE

Inputs		Outputs			
Enable A, Enable B	A, B	YA, YB			
L	L	L			
L	Н	H			
Н	Χ	Z			
Z = high impe	Z = high impedance, X = don't care				

ORDERING AND MARKING INFORMATION

See detailed ordering, shipping, and marking information in the package dimensions section on page 5 of this data sheet.

1

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I _{in}	DC Input Current, per Pin	± 20	mA
l _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and Vout should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC}. Unused inputs must always be

tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

- SOIC Package: 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C
 For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	imit	
Symbol	Parameter	Test Conditions	V _{CC}	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	4.5 5.5	2 2	2 2	2 2	V
V _{IL}	Maximum Low–Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu\text{A}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 6 \text{ mA}$	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu\text{A}$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 6 \text{ mA}$	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μΑ
I _{OZ}	Maximum Three–State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} ; V _{out} = V _{CC} or GND	5.5	± 0.5	± 5.0	± 10	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	4	40	160	μΑ
ΔI_{CC}	Additional Quiescent Supply	V _{in} = 2.4 V, Any One Input		≥ -55 °C	25°C to	125°C	
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0 \mu A$	5.5	2.9	2	.4	mA

^{1.} Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

2. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

Plastic DIP: - 10 mW/°C from 65° to 125°C †Derating -

AC ELECTRICAL CHARACTERISTICS (V $_{CC}$ = 5.0 V \pm 10%, C_{L} = 50 pF, Input t_{r} = t_{f} = 6 ns)

		Guaranteed Limit			
Symbol	Parameter	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	26	33	39	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	22	28	33	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	55	pF

^{*}Used to determine the no–load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

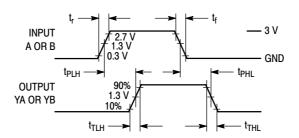


Figure 2.

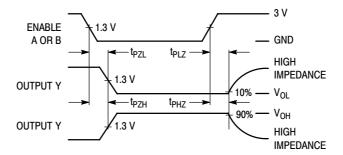
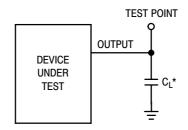


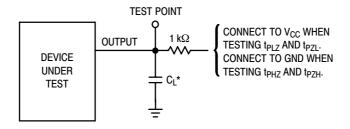
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

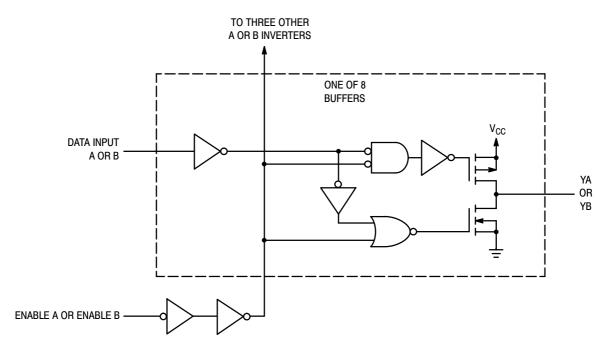
Figure 4.



*Includes all probe and jig capacitance

Figure 5.

LOGIC DETAIL

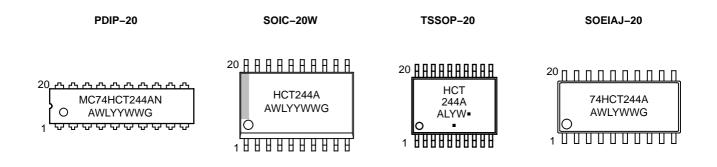


ORDERING INFORMATION

Device	Package	Shipping [†]	
MC74HCT244AN	PDIP-20		
MC74HCT244ANG	PDIP-20 (Pb-Free)	18 Units / Rail	
MC74HCT244ADW	SOIC-20		
MC74HCT244ADWG	SOIC-20 (Pb-Free)	38 Units / Rail	
MC74HCT244ADWR2	SOIC-20		
MC74HCT244ADWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel	
MC74HCT244ADTR2	TSSOP-20*	0500 / Tara 9 Paul	
MC74HCT244ADTR2G	TSSOP-20*	2500 / Tape & Reel	
MC74HCT244AF	SOEIAJ-20		
MC74HCT244AFG	SOEIAJ-20 (Pb-Free)	40 Units / Rail	
MC74HCT244AFEL	SOEIAJ-20		
MC74HCT244AFELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



A = Assembly Location

WL, L = Wafer Lot YY, Y = Year

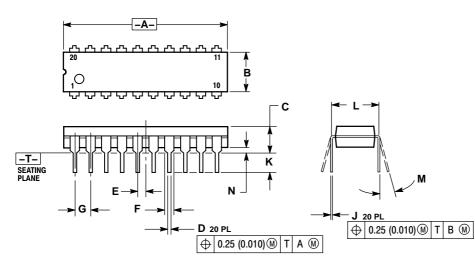
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

^{*}These packages are inherently Pb-Free.

PACKAGE DIMENSIONS

PDIP-20 **N SUFFIX** PLASTIC DIP PACKAGE CASE 738-03 ISSUE E

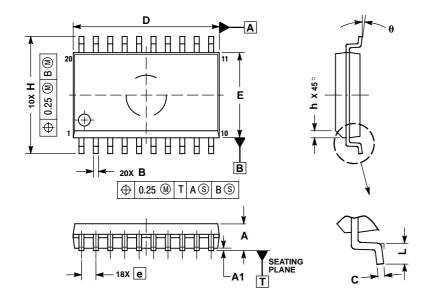


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION LTO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLACULE.

 - FLASH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	1.010	1.070	25.66	27.17
В	0.240	0.260	6.10	6.60
С	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
Е	0.050	BSC	1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100	0.100 BSC		BSC
7	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300	BSC	7.62	BSC
M	0 °	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOIC-20W **DW SUFFIX** CASE 751D-05 ISSUE G

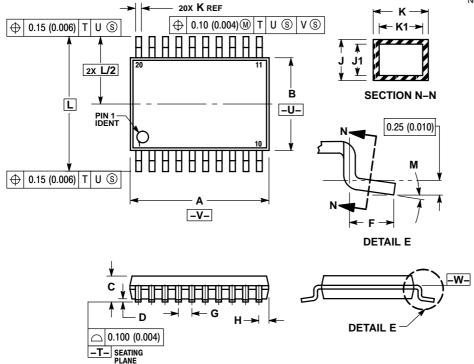


- NOTES:
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.35	2.65		
A1	0.10	0.25		
В	0.35	0.49		
С	0.23	0.32		
D	12.65	12.95		
E	7.40	7.60		
е	1.27	BSC		
Н	10.05	10.55		
h	0.25	0.75		
L	0.50	0.90		
Δ	n o	70		

PACKAGE DIMENSIONS

TSSOP-20 **DT SUFFIX** CASE 948E-02 **ISSUE C**

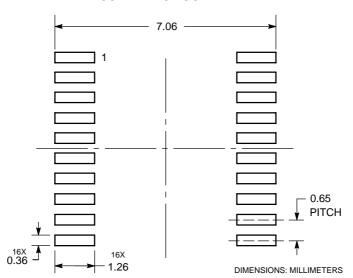


- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION:
 MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE
 MOLD FLASH, PROTRUSIONS OR GATE
 BURRS. MOLD FLASH OR GATE BURRS
 SHALL NOT EXCEED 0,15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 - INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION
 SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 - SHALL NOT EXCEED 0.25 (0.010) PER S 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
 - DIMENSION AT MAXIMUM MATERIAL
 CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE
 PETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

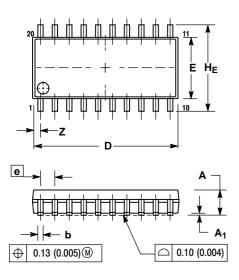
SOLDERING FOOTPRINT*

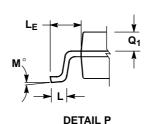


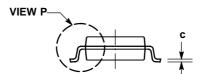
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOEIAJ-20 **F SUFFIX** CASE 967-01 **ISSUE A**







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (0.006) PEH SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION.
 DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A ₁	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.15	0.25	0.006	0.010	
D	12.35	12.80	0.486	0.504	
Ε	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050	BSC	
HE	7.40	8.20	0.291	0.323	
L	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10°	0 °	10°	
Q ₁	0.70	0.90	0.028	0.035	
Z		0.81		0.032	

ON Semiconductor and up are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice ON Semiconductor and war registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights or the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized large steps SCILLC is an Equal to the desiring or manufacture of the party of t associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA **Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81–3–5773–3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative