19-1310; Rev 0; 10/97

MAXIM

5-Tap Silicon Delay Line

General Description

The MXD1000 silicon delay line offers five equally spaced taps with delays ranging from 4ns to 500ns and a nominal accuracy of ±2ns or ±5%, whichever is greater. Relative to hybrid solutions, this device offers enhanced performance and higher reliability, and reduces overall cost. Each tap can drive up to ten 74LS loads.

The MXD1000 is available in multiple versions, each offering a different combination of delay times. It comes in the space-saving 8-pin µMAX package, as well as an 8-pin SO or DIP, allowing full compatibility with the DS1000 and other delay line products.

Features

- **Improved Second Source to DS1000**
- **Available in Space-Saving 8-Pin µMAX Package**
- **20mA Supply Current (vs. Dallas' 35mA)**
- **Low Cost**
- **Delay Tolerance of ±2ns or ±5%, whichever is Greater**
- **TTL/CMOS-Compatible Logic**
- **Leading- and Trailing-Edge Accuracy**
- **Custom Delays Available**

Applications

Clock Synchronization

Digital Systems

Functional Diagram appears at end of data sheet.

Ordering Information

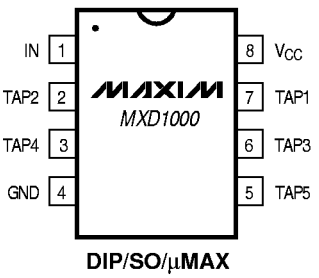
PART	TEMP. RANGE	PIN-PACKAGE
MXD1000C/D__	0°C to +70°C	Dice*
MXD1000PA__	-40°C to +85°C	8 Plastic DIP
MXD1000PD__	-40°C to +85°C	14 Plastic DIP
MXD1000SA__	-40°C to +85°C	8 SO
MXD1000SE__	-40°C to +85°C	16 Narrow SO
MXD1000UA__	-40°C to +85°C	8 µMAX

**Dice are tested at T_A = +25°C.*

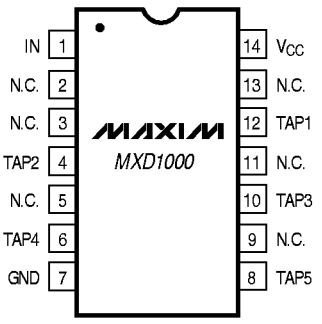
Note: *To complete the ordering information, fill in the blank with the part number extension from the Part Number and Delay Times table (located at the end of this data sheet) to indicate the desired delay per output.*

Pin Configurations

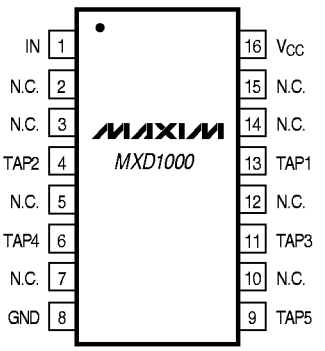
TOP VIEW



DIP/SO/µMAX



DIP



SO

5-Tap Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to +6V
All Other Pins.....-0.5V to (V_{CC} + 0.5V)
Short-Circuit Output Current (1sec).....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.0mW/°C above +70°C) ...800mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) 696mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 3)	4.75	5.00	5.25	V
Input Voltage High	V_{IH}	(Note 3)	2.2			V
Input Voltage Low	V_{IL}	(Note 3)			0.8	V
Input Leakage Current	I_L	$0V \le V_{IN} \le V_{CC}$	-1		1	µA
Active Current	I_{CC}	V_{CC} = 5.25V, period = minimum (Notes 4, 5)		20	75	mA
Output Current High	I_{OH}	V_{CC} = 4.75V, V_{OH} = 4.0V			-1	mA
Output Current Low	I_{OL}	V_{CC} = 4.75V, V_{OL} = 0.5V	12			mA
Input Capacitance	C_{IN}	T_A = +25°C (Note 6)		5	10	pF

TIMING CHARACTERISTICS

(V_{CC} = +5.0V ±5%, T_A = +25°C, unless otherwise noted.)

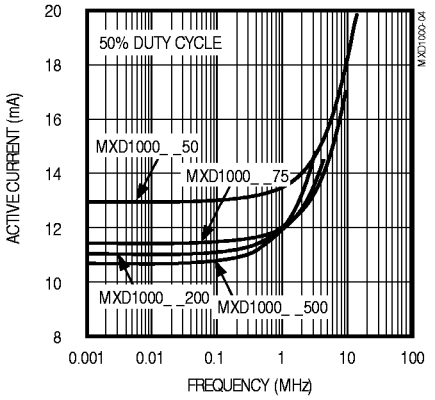
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 7)	40% of TAP5 t_{PLH}			ns
Input-to-Tap Delay (leading edge)	t_{PLH}	(Notes 1, 8–12)		See *Part Number and Delay Times* table		ns
Input-to-Tap Delay (trailing edge)	t_{PHL}	(Notes 1, 8–12)		See *Part Number and Delay Times* table		ns
Power-Up Time	t_{PU}				100	ms
Period		(Note 7)	4(t_{WI})			ns

Note 1: Contact factory for ordering information.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.
Note 3: All voltages referenced to GND.
Note 4: Measured with output open.
Note 5: I_{CC} is a function of frequency and TAP5 delay. Only an MXD1000__25 operating with a 40ns period and V_{CC} = +5.25V will have an I_{CC} = 75mA. For example, an MXD1000__100 will never exceed 30mA. See Supply Current vs. Input Frequency in *Typical Operating Characteristics*.
Note 6: Guaranteed by design.
Note 7: Pulse width and/or period specifications may be exceeded, but accuracy is application sensitive (i.e., layout, decoupling, etc.). The device will remain functional with pulse widths down to 20% of TAP5 delay, and input periods as short as 2(t_{WI}).
Note 8: Typical initial tolerances are ± with respect to the nominal value at +25°C and V_{CC} = 5V.
Note 9: Typical temperature tolerance is ± with respect to the initial delay value over a temperature range of -40°C to +85°C.
Note 10: The delay will also vary with supply voltage, typically by less than 4% over the supply range of V_{CC} = +4.75V to +5.25V.
Note 11: All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP1 slows down, all other taps will also slow down; i.e., TAP3 can never be faster than TAP2.

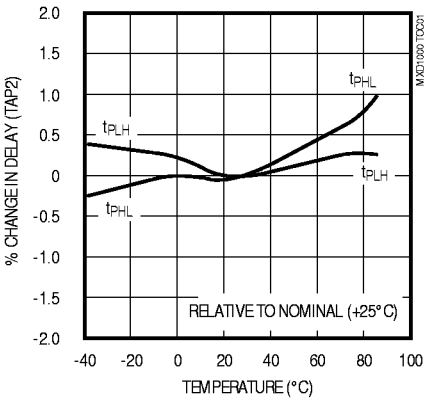
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

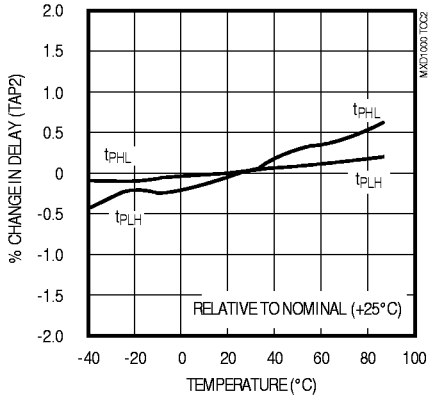
ACTIVE CURRENT vs. FREQUENCY



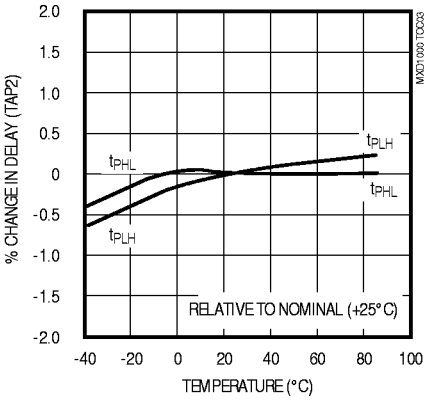
MXD1000_ _75 PERCENT CHANGE IN DELAY vs. TEMPERATURE



MXD1000_ _100 TO MXD1000_ _200 PERCENT CHANGE IN DELAY vs. TEMPERATURE



MXD1000_ _250 TO MXD1000_ _500 PERCENT CHANGE IN DELAY vs. TEMPERATURE



5-Tap Silicon Delay Line

Pin Description

PIN			NAME	FUNCTION
8-PIN DIP/SO/µMAX	14-PIN DIP	16-PIN SO		
1	1	1	IN	Signal Input
2	4	4	TAP2	40% of specified maximum delay
3	6	6	TAP4	80% of specified maximum delay
4	7	8	GND	Device Ground
5	8	9	TAP5	100% of maximum specified delay
6	10	11	TAP3	60% of specified maximum delay
7	12	13	TAP1	20% of specified maximum delay
8	14	16	V_{CC}	Power-Supply Input
—	2, 3, 5, 9, 11, 13	2, 3, 5, 7, 10, 12, 14, 15	N.C.	No Connection. Not internally connected.

Note: *Maximum delay is determined by the part number extension. See the Part Number and Delay Times table for more information.*

Definitions of Terms

Period: The time elapsed between the first pulse's leading edge and the following pulse's leading edge.

Pulse Width (t_{WI}): The time elapsed on the pulse between the 1.5V level on the leading edge and the 1.5V level on the trailing edge, or vice-versa.

Input Rise Time (t_{RISE}): The time elapsed between the 20% and 80% points on the input pulse's leading edge.

Input Fall Time (t_{FALL}): The time elapsed between the 80% and 20% points on the input pulse's trailing edge.

Time Delay, Rising (t_{PLH}): The time elapsed between the 1.5V level on the input pulse's leading edge and the corresponding output pulse's leading edge.

Time Delay, Falling (t_{PHL}): The time elapsed between the 1.5V level on the input pulse's trailing edge and the corresponding output pulse's trailing edge.

Test Conditions

Ambient Temperature:	+25°C ±3°C
Supply Voltage (V_{CC}):	+5V ±0.1V
Input Pulse:	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Times:	3.0ns max
Pulse Width:	500ns max (1ns for -500)
Period:	1µs (2ns for -500)

Each output is loaded with a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edges. The time delay due to the 74F04 is subtracted from the measured delay.

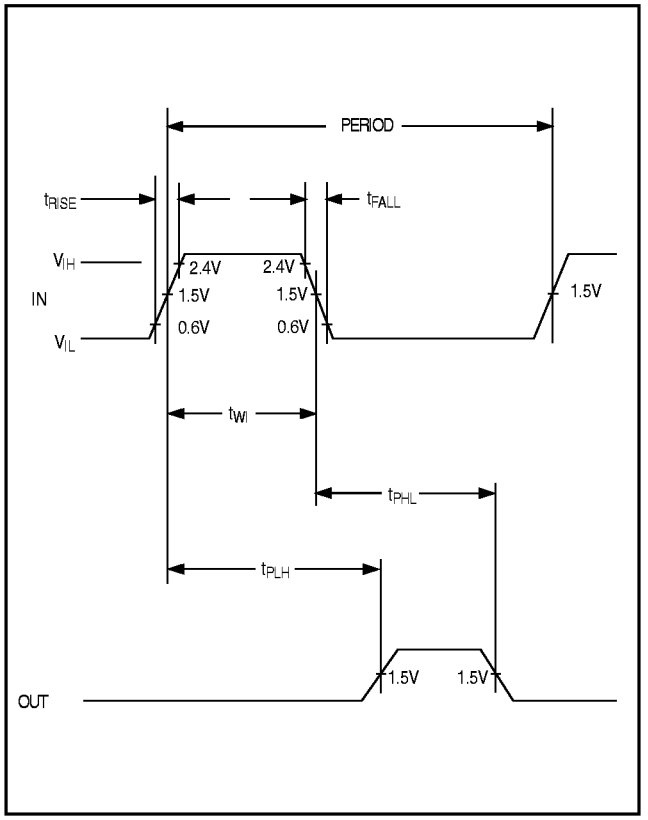


Figure 1. Timing Diagram

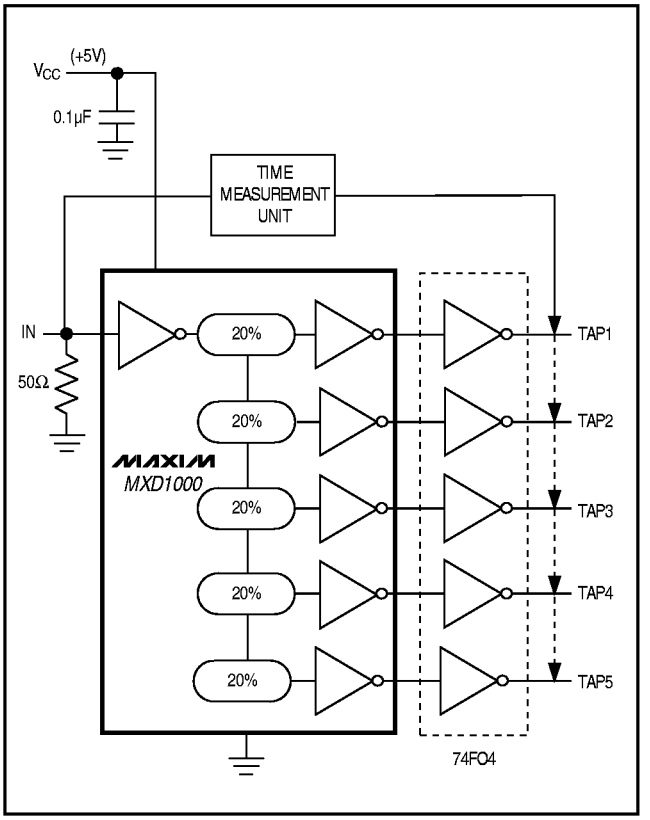


Figure 2. Test Circuit

Applications Information

Supply and Temperature Effects on Delay

Variations in supply voltage may affect the MXD1000's fixed tap delays. Supply voltages beyond the specified range may result with larger variations. The devices are internally compensated to reduce the effects of temperature variations. Although these devices might vary with supply and temperature, the delays vary unilaterally, which suggests that TAP3 can never be faster than TAP2.

Capacitance and Loading Effects on Delay

The output load can affect the tap delays. Larger capacitances tend to lengthen the rising and falling edges, thus increasing the tap delays. As the taps are loaded with other logic devices, the increased load will increase the tap delays.

Board Layout Considerations/Decoupling

The device should be driven with a source that can deliver the required current for proper operation. A 0.1µF ceramic bypassing capacitor could be used. The board should be designed to reduce stray capacitance.

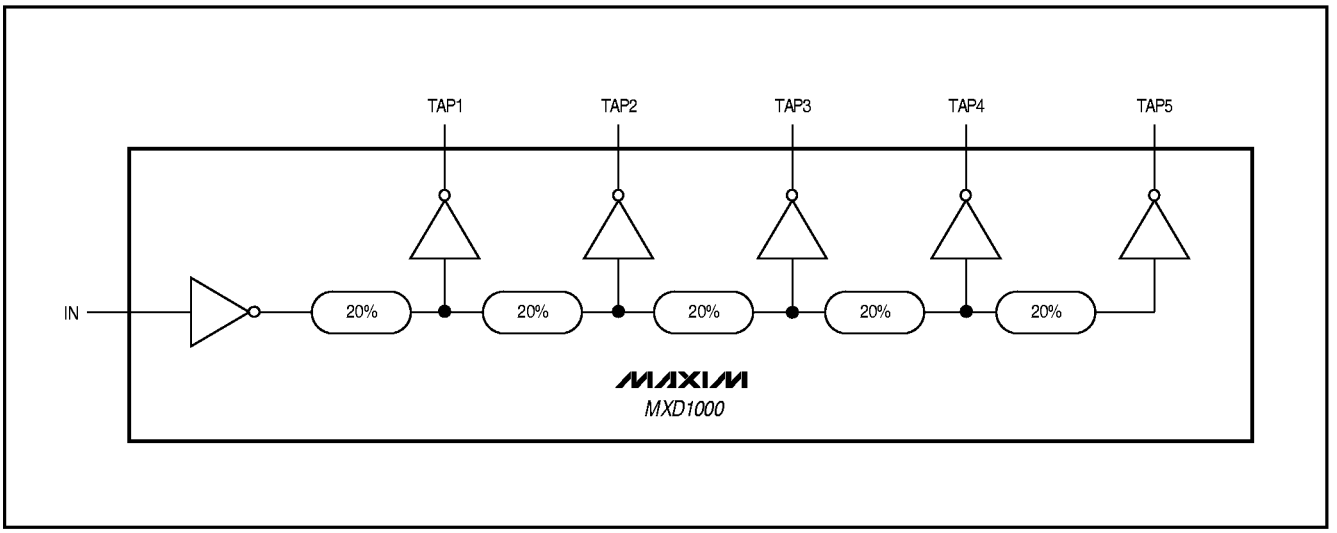
5-Tap Silicon Delay Line

Part Number and Delay Times

Part Number Extension (MXD1000__)	TAP1			TAP2			TAP3			TAP4			TAP5		
	Nom. Delay (ns)	Tolerance (ns)		Nom. Delay (ns)	Tolerance (ns)		Nom. Delay (ns)	Tolerance (ns)		Nom. Delay (ns)	Tolerance (ns)		Nom. Delay (ns)	Tolerance (ns)	
		Init.	Temp.		Init.	Temp.		Init.	Temp.		Init.	Temp.		Init.	Temp.
20 (Note 1)	4	2	1	8	2	1	12	2	1	16	2	1	20	2	1
25 (Note 1)	5	2	1	10	2	1	15	2	1	20	2	1	25	2	1
30 (Note 1)	6	2	1	12	2	1	18	2	1	24	2	1	30	2	1
35	7	2	1	14	2	1	21	2	1	28	2	1	35	2	1.1
40	8	2	1	16	2	1	24	2	1	32	2	1	40	2	1.2
45	9	2	1	18	2	1	27	2	1	36	2	1.1	45	2.3	1.4
50	10	2	1	20	2	1	30	2	1	40	2	1.2	50	2.5	1.5
60	12	2	1	24	2	1	36	2	1.1	48	2.4	1.5	60	3	1.8
75	15	2	1	30	2	1	45	2.3	1.4	60	3	1.8	75	3.8	2.3
100	20	2	1	40	2	1.2	60	3	1.8	80	4	2.4	100	5	3
125	25	2	1	50	2.5	1.5	75	3.8	2.3	100	5	3	125	6.3	3.8
150	30	2	1	60	3	1.8	90	4.5	2.7	120	6	3.6	150	7.5	4.5
175	35	2	1.1	70	3.5	2.1	105	5.3	3.2	140	7	4.2	175	8.8	5.3
200	40	2	1.2	80	4	2.4	120	6	3.6	160	8	4.8	200	10	6
250	50	2.5	1.5	100	5	3	150	7.5	4.5	200	10	6	250	12.5	7.5
500	100	5	3	200	10	6	300	15	9	400	20	12	500	25	15

Note 1: Contact factory for ordering information.

Functional Diagram

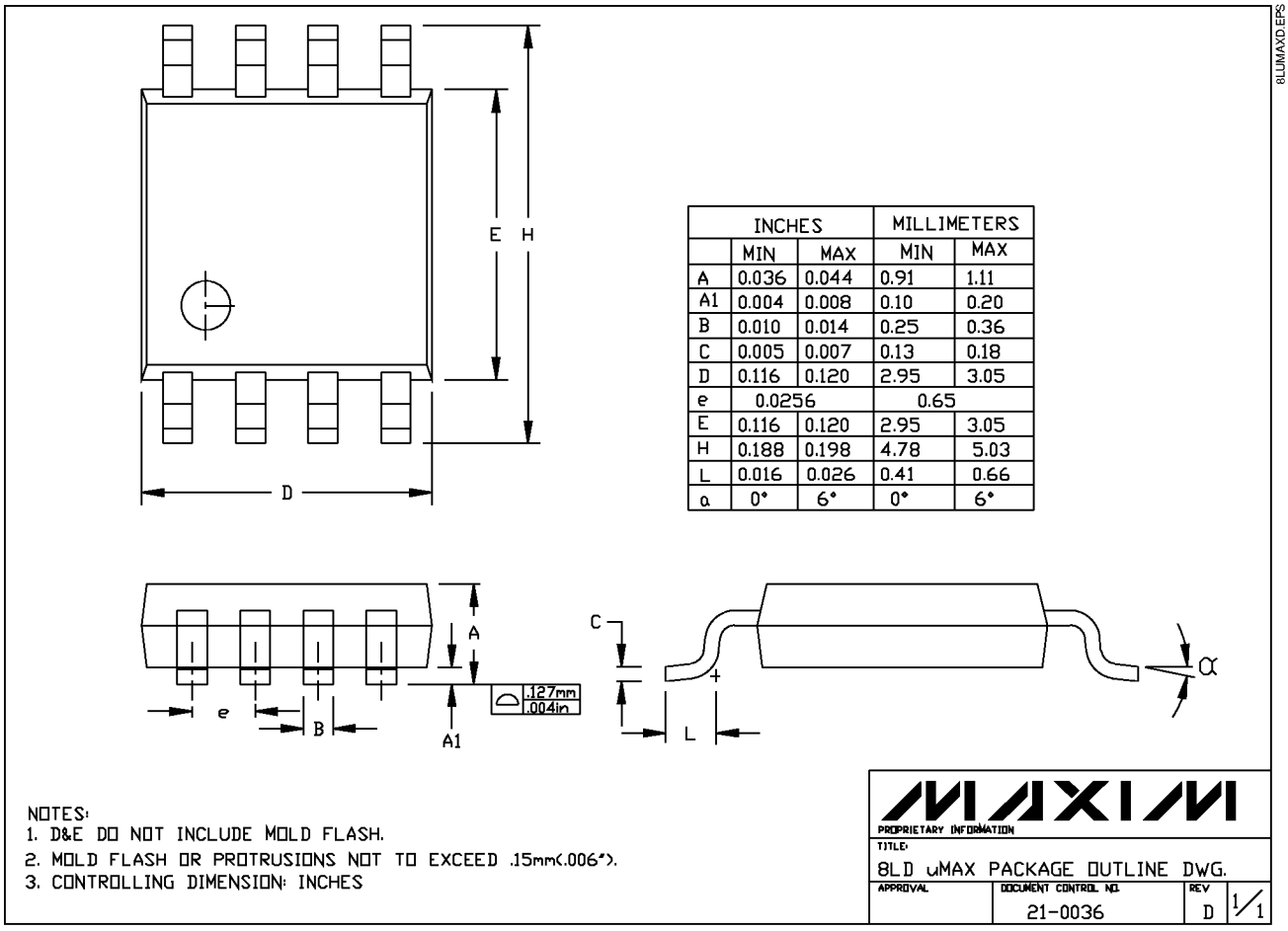


Chip Information

TRANSISTOR COUNT: 824

5-Tap Silicon Delay Line

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

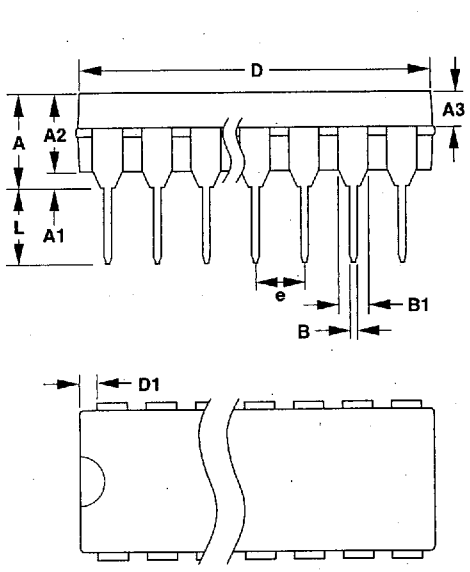
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION

TITLE:
8LD uMAX PACKAGE OUTLINE DWG.

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	D	1/1

This section contains physical dimensions for all packages currently supplied by Maxim.

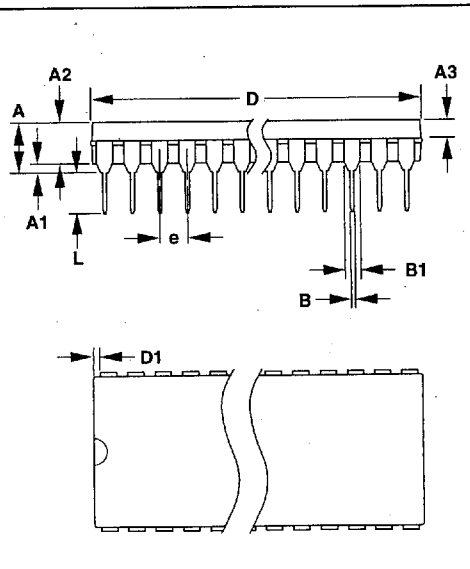


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



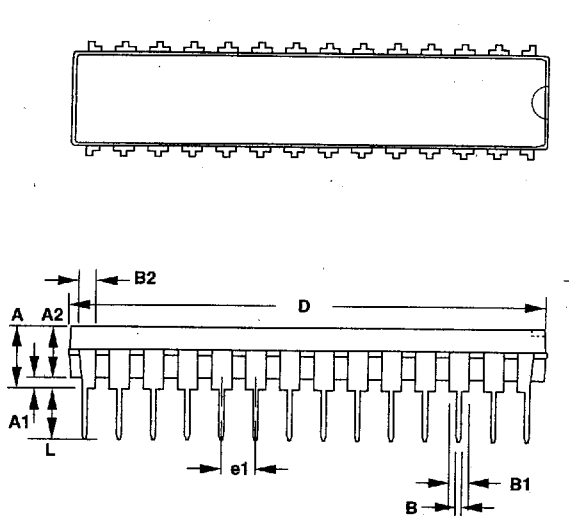
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	24	1.230	1.270	31.24	32.26
P	D	28	1.430	1.470	36.32	37.34
P	D	40	2.025	2.075	51.44	52.71

21-0044A

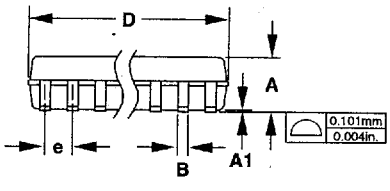
A

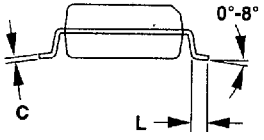


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.180	–	4.572
A1	0.020	–	0.508	–
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
L	0.115	0.150	2.921	3.810
α	0°	15°	0°	15°

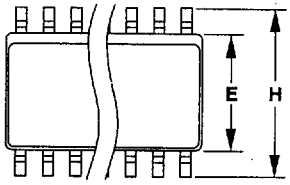
21-0400A

Narrow Plastic DIP
28-PIN PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



Narrow SO
SMALL-OUTLINE
PACKAGE
(0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A