

# 1 PRODUCT OVERVIEW

## SAM87RI PRODUCT FAMILY

Samsung's SAM87Ri family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A address/data bus architecture and a large number of bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

## S3C9432/C9434 MICROCONTROLLER

The S3C9432/C9434 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87Ri CPU core. The S3C9432/C9434 is a versatile microcontroller, with its A/D converter, timer, PWM, and SIO it can be used in a wide range of general purpose applications.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The S3C9432/C9434 have 2K-bytes or 4K-bytes of program memory on-chip (ROM) and 112-bytes of general purpose register area RAM.

Using the SAM87Ri design approach, the following peripherals were integrated with the SAM87Ri core:

- Three configurable I/O ports (13 pins)
- Five interrupt sources with one vector and one interrupt level
- One 8-bit timer/counter with time interval mode
- Analog to digital converter with five input channels and 10-bit resolution
- One synchronous SIO module
- One 12-bit PWM output

The S3C9432/C9434 microcontroller is ideal for use in a wide range of electronic applications requiring simple timer/counter, PWM, ADC, and SIO. S3C9432/C9434 is available in a 20/18/16-pin DIP and a 20-pin SOP package.

## OTP

The S3P9434 is an OTP (One Time Programmable) version of the S3C9432/C9434 microcontroller. The S3P9434 has on-chip 4K-byte one-time-programmable EPROM instead of masked ROM. The S3P9434 is fully compatible with the S3C9432/C9434, in function, in D.C. electrical characteristics and in pin configuration.

## FEATURES

### CPU

- SAM87RI CPU core

### Memory

- 2/4K-byte internal program memory (ROM)
- 112-byte general purpose register area (RAM)

### Instruction Set

- 41 instructions
- The SAM87RI core provides all the SAM87 core instruction except the word-oriented instruction, multiplication, division, and some one-byte instruction.

### Instruction Execution Time

- 600 ns at 10 MHz  $f_{OSC}$  (minimum cycles)
- 375 ns at 16 MHz  $f_{OSC}$  (minimum cycles)

### Interrupts

- 5 interrupt sources with one vector and one level interrupt structure

### General I/O

- Two I/O ports (Total 13 pins)
- One output only port (port 2)
- Bit programmable ports

### Serial I/O

- One synchronus serial I/O module
- Selectable transmit and receive rates

### Built-in reset Circuit (LVD)

- Low voltage detector for safe reset

### Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter for the time interval mode

### PWM Module

- 12-bit PWM 1-ch (Max: 250 kHz)
- 6-bit base + 6-bit extension frame

### A/D Converter

- Five analog input pins
- 10-bit conversion resolution

### Buzzer Frequency Range

- 200 Hz to 20 kHz signal can be generated

### Oscillation Frequency

- 1 MHz to 16 MHz external crystal oscillator
- Maximum 16 MHz CPU clock
- 4 MHz RC oscillator

### Operating Temperature Range

- -40°C to +85°C

### Operating Voltage Range

- 3.0 V to 5.5 V

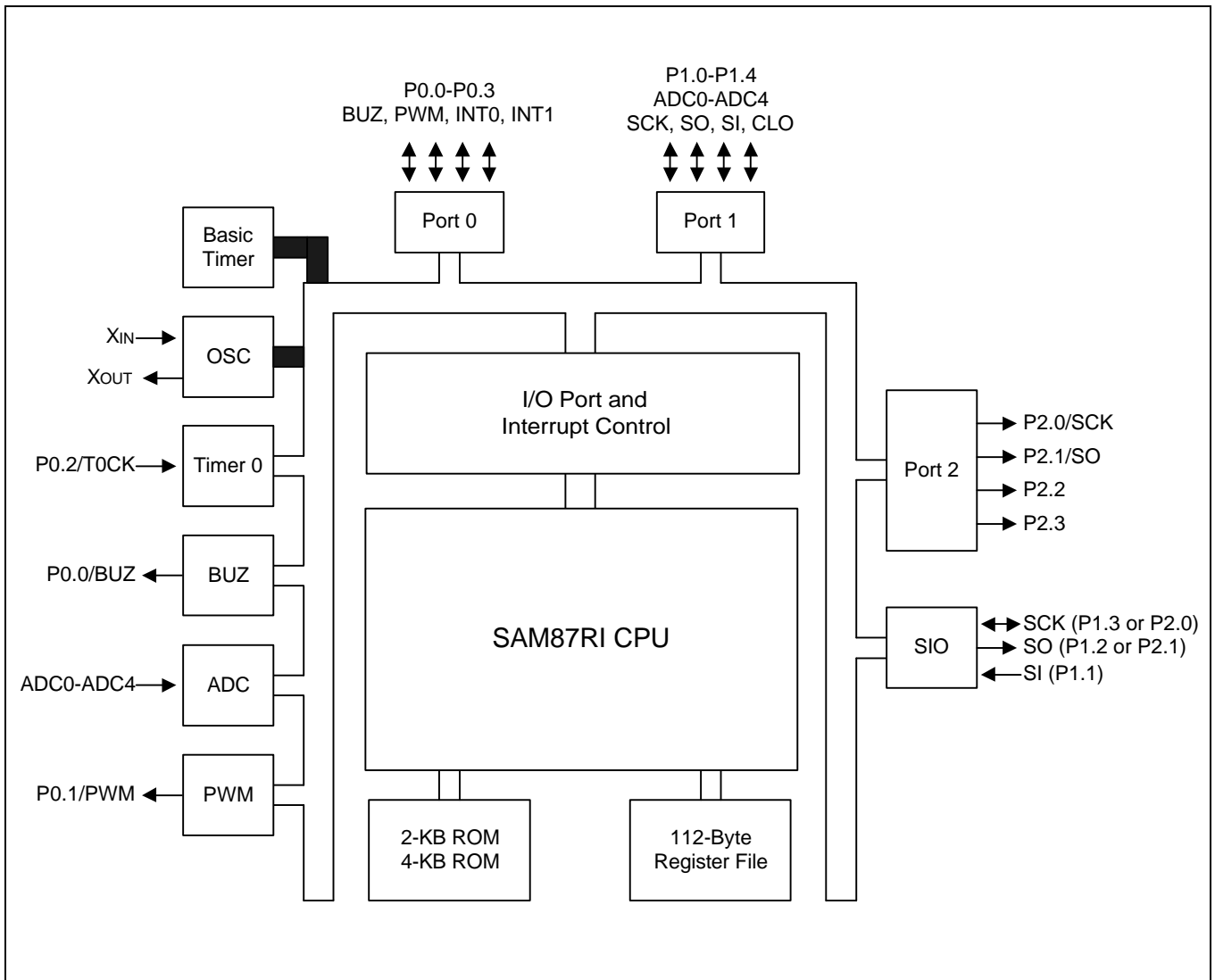
### OTP Interface Protocol Spec

- Serial OTP

### Package Types

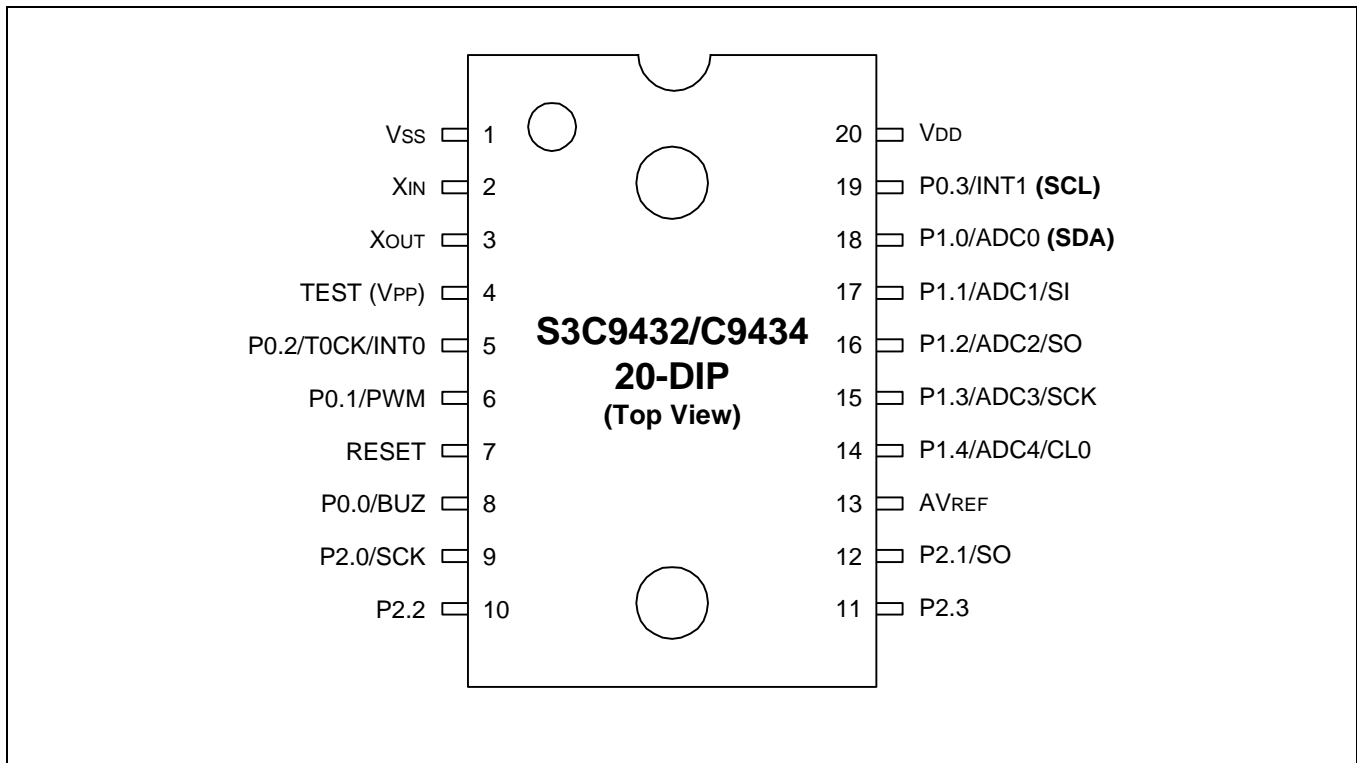
- 20-pin DIP-300
- 20-pin SOP-375
- 18-pin DIP-300
- 16-pin DIP-300

**BLOCK DIAGRAM**



**Figure 1-1. Block Diagram**

**PIN ASSIGNMENTS**



**Figure 1-2. Pin Assignment Diagram (20-Pin DIP Package)**

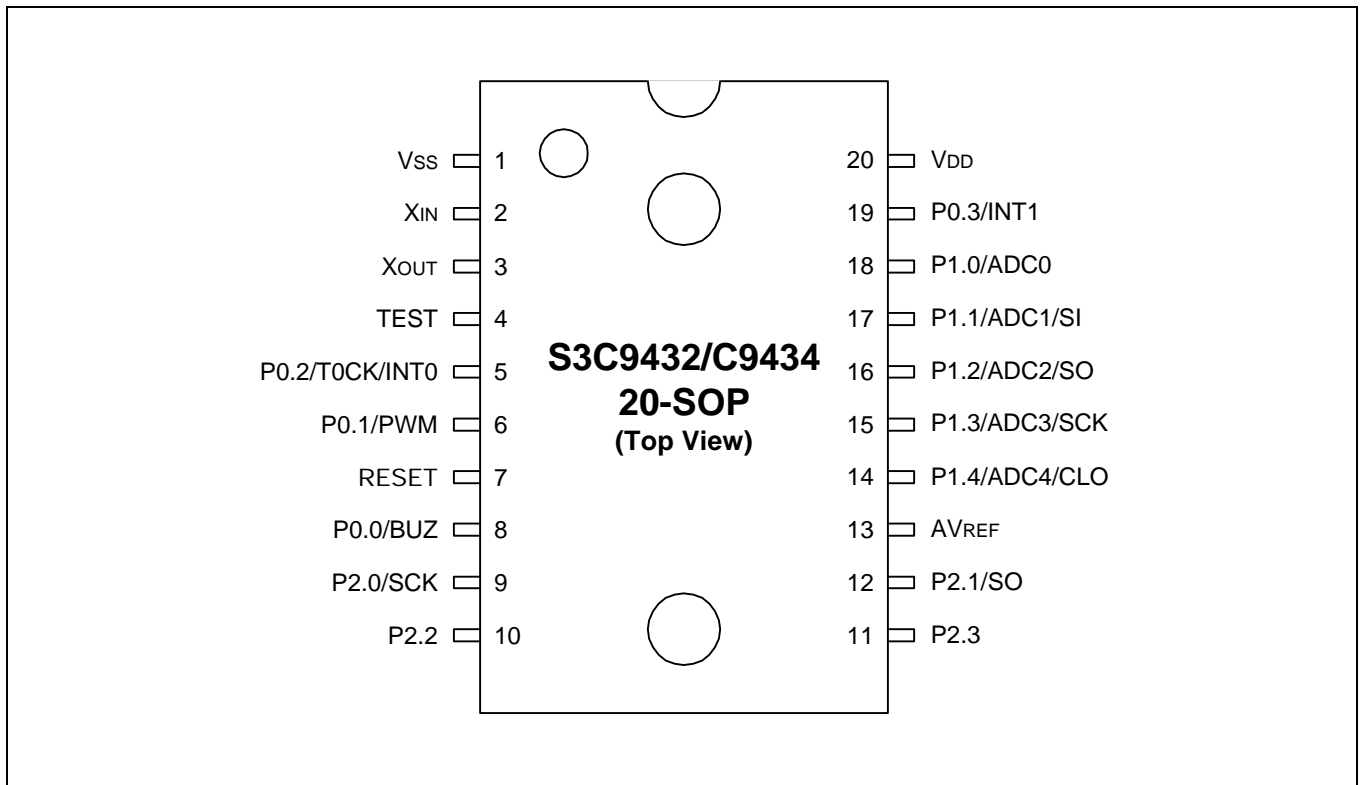


Figure 1-3. Pin Assignment Diagram (20-Pin SOP Package)

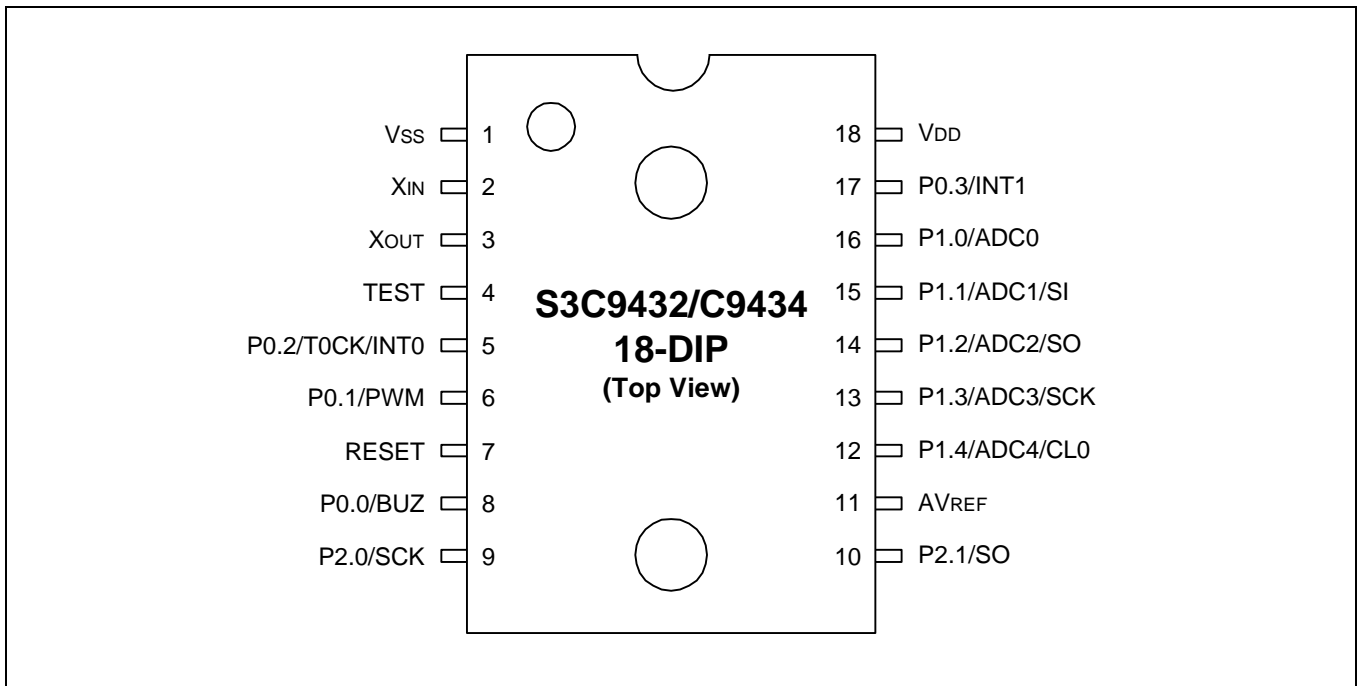


Figure 1-4. Pin Assignment Diagram (18-Pin DIP Package)

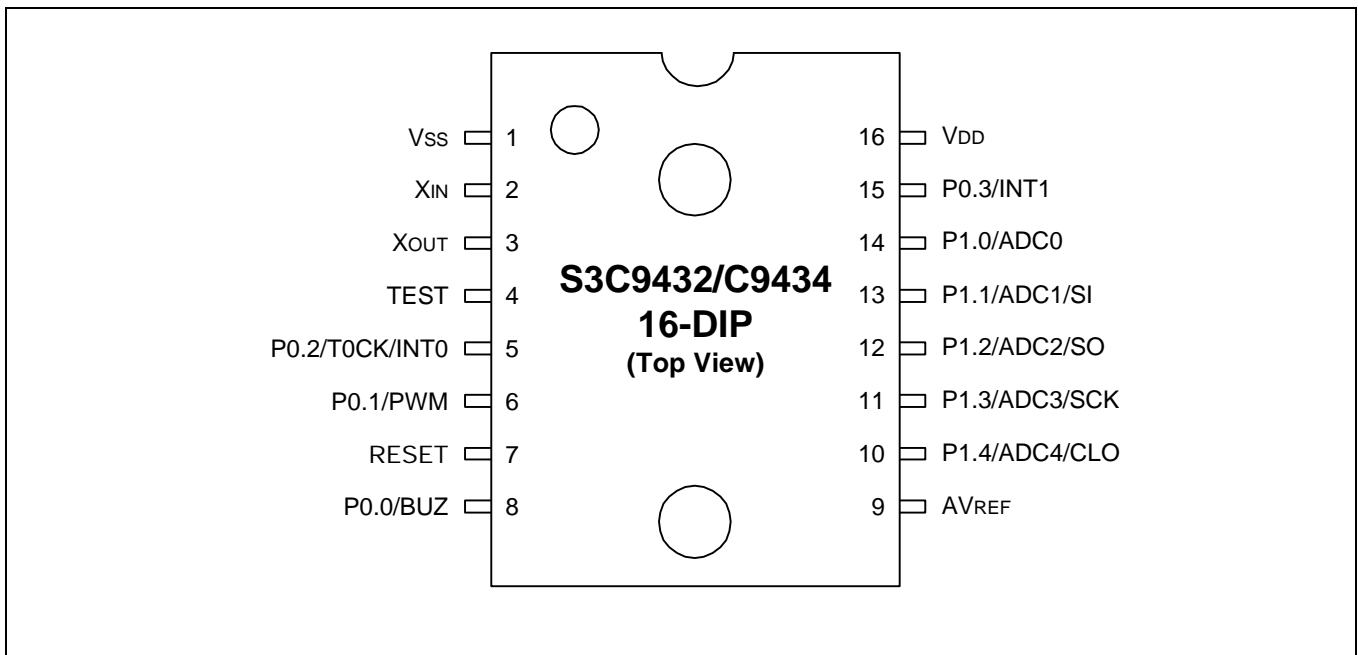


Figure 1-5. Pin Assignment Diagram (16-Pin DIP Package)

## PIN DESCRIPTIONS

Table 1-1. S3C9432/C9434 Pin Descriptions

| Pin Names                          | Pin Type | Pin Description  | Circuit Type | Share Pins                          |
|------------------------------------|----------|--|--------------|-------------------------------------|
| P0.0-P0.3                          | I/O      | Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software. Port 0 pins can also be used as alternative function. | E            | BUZ<br>PWM<br>INT0/T0CK<br>INT1     |
| P1.0-P1.4                          | I/O      | Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software. Port 1 pins can also be used as alternative function. | E-1          | ADC0-ADC4<br>SI<br>SO<br>SCK<br>CLO |
| P2.0-P2.3                          | O        | Push-pull or open-drain output port. Pull up resistors are assignable by software. Port 2.0-2.1 pins can also be used as alternative function.   | E-2          | SCK<br>SO                           |
| X <sub>IN</sub> , X <sub>OUT</sub> | –        | Crystal/ceramic, or RC oscillator signal for system clock.   | –            | –                                   |
| RESET                              | I        | System RESET signal input pin.   | B            | –                                   |
| TEST                               | I        | Test signal input pin (for factory use only: must be connected to V <sub>SS</sub> )  | –            | –                                   |
| V <sub>DD</sub> , V <sub>SS</sub>  | –        | Voltage input pin and ground   | –            | –                                   |
| AV <sub>REF</sub>                  | –        | A/D converter reference voltage input and ground   | –            | –                                   |
| AV <sub>SS</sub>                   |          | Bonded to V <sub>SS</sub> internally   |              |                                     |
| SCK                                | I/O      | Serial interface clock I/O   | E-1<br>E-2   | P1.3 or<br>P2.0                     |
| SO                                 | O        | Serial data output   | E-1<br>E-2   | P1.2 or<br>P2.1                     |
| SI                                 | I        | Serial data input  | E-1          | P1.1                                |
| CLO                                | O        | System clock output port   | E-1          | P1.4                                |
| BUZ                                | O        | 200 Hz- 20 kHz frequency output for buzzer sound   | E            | P0.0                                |
| PWM                                | O        | 12-bit PWM output  | E            | P0.1                                |
| INT0-INT1                          | I        | External interrupt input port  | E            | P0.2<br>P0.3                        |
| T0CK                               | I        | Timer 0 external clock input   | E            | P0.2                                |
| ADC0-ADC4                          | I        | A/D converter input  | E-1          | P1.0-P1.4                           |

PIN CIRCUITS

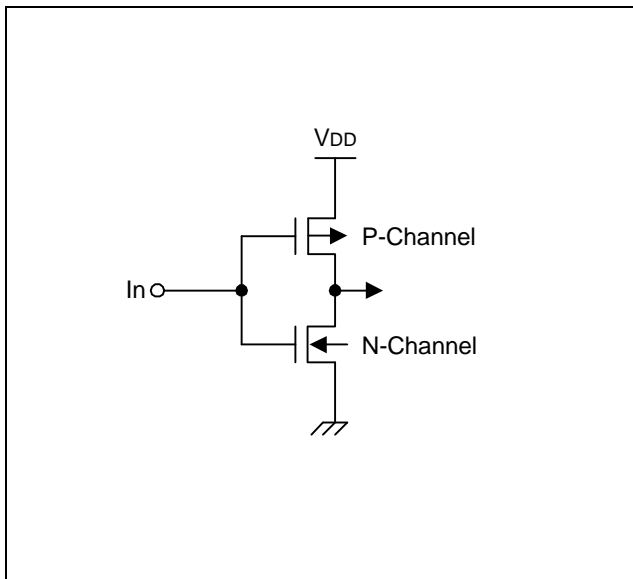


Figure 1-6. Pin Circuit Type A

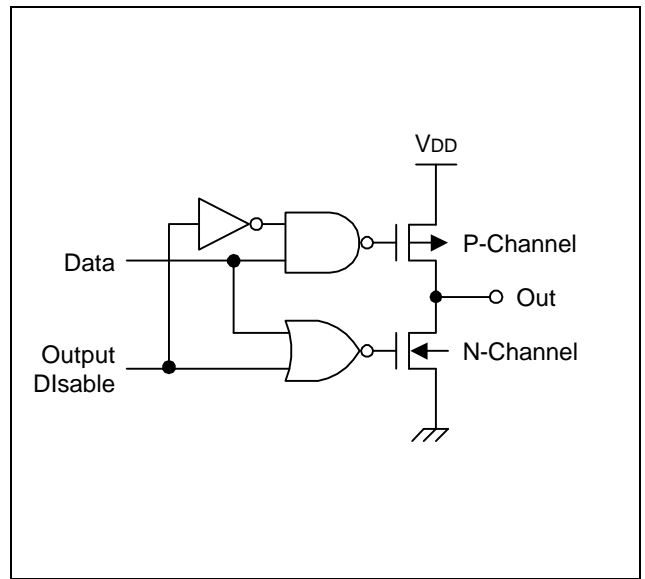


Figure 1-8. Pin Circuit Type C

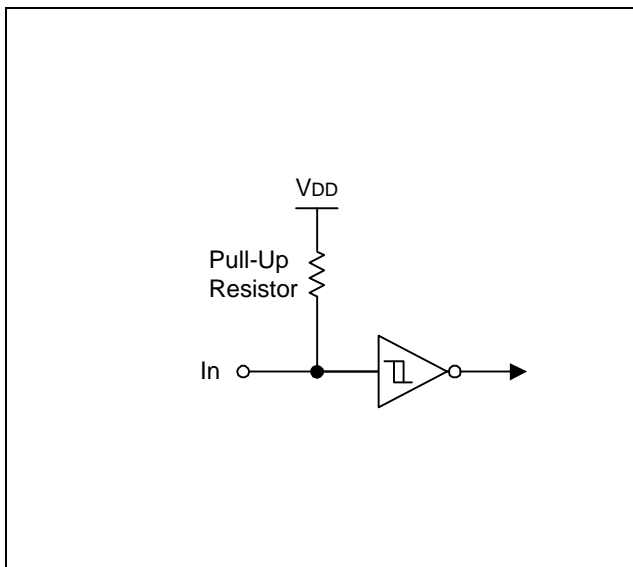


Figure 1-7. Pin Circuit Type B

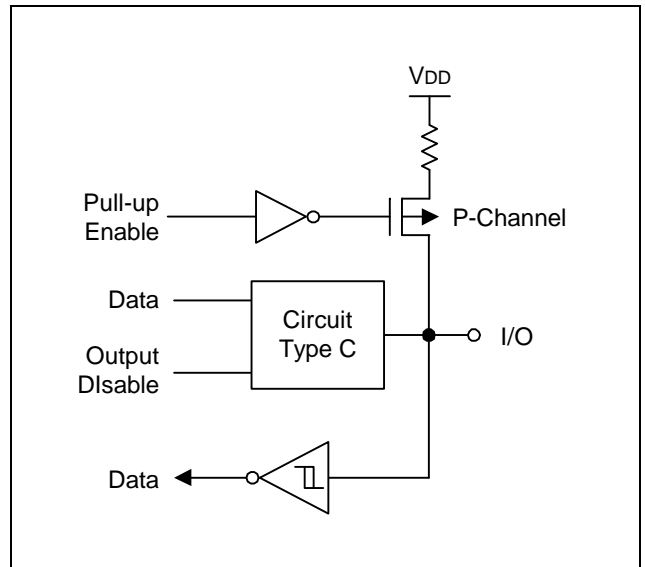


Figure 1-9. Pin Circuit Type D



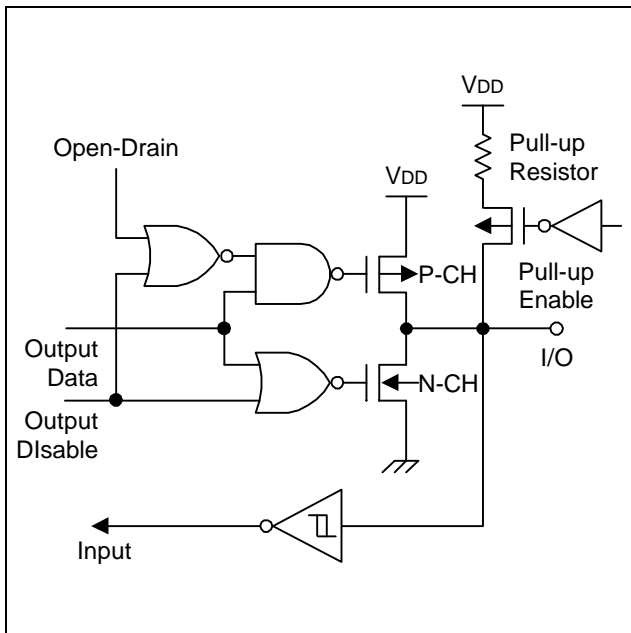


Figure 1-10. Pin Circuit Type E

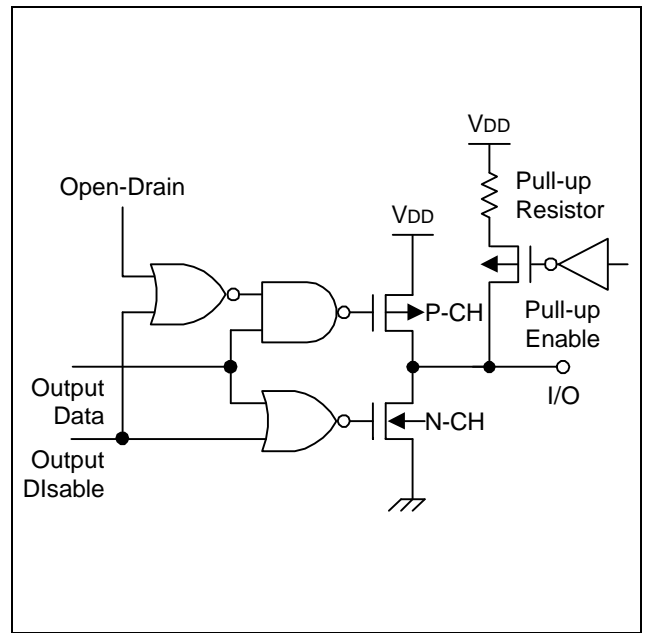


Figure 1-12. Pin Circuit Type E-2

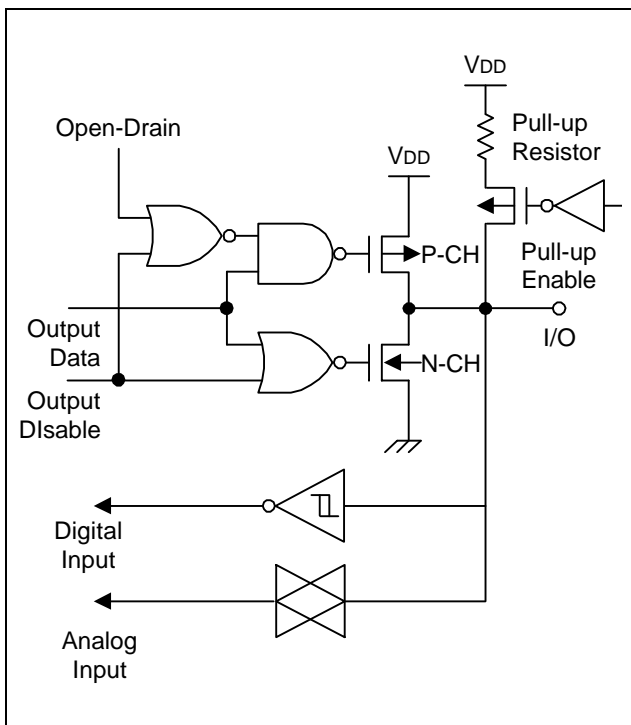


Figure 1-11. Pin Circuit Type E-1

# 14 ELECTRICAL DATA

## OVERVIEW

In this section, the following S3C9432/C9434 electrical characteristics are presented in tables and graphs:

- Absolute maximum ratings
- D.C. electrical characteristics
- A.C. electrical characteristics
- Input Timing Measurement Points
- Oscillator characteristics
- Oscillation stabilization time
- Operating Voltage Range
- Schmitt trigger input characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by a RESET
- A/D converter electrical characteristics
- LVD circuit characteristics
- LVD reset Timing
- Serial I/O timing characteristics
- Serial data transfer timing

Table 14-1. Absolute Maximum Ratings

 $(T_A = 25^\circ\text{C})$ 

| Parameter             | Symbol    | Conditions          | Rating                  | Unit             |
|-----------------------|-----------|---------------------|-------------------------|------------------|
| Supply voltage        | $V_{DD}$  | –                   | - 0.3 to + 6.5          | V                |
| Input voltage         | $V_I$     | All input ports     | - 0.3 to $V_{DD} + 0.3$ | V                |
| Output voltage        | $V_O$     | All output ports    | - 0.3 to $V_{DD} + 0.3$ | V                |
| Output current high   | $I_{OH}$  | One I/O pin active  | - 25                    | mA               |
|                       |           | All I/O pins active | - 80                    |                  |
| Output current low    | $I_{OL}$  | One I/O pin active  | + 30                    | mA               |
|                       |           | All I/O pins active | + 150                   |                  |
| Operating temperature | $T_A$     | –                   | - 40 to + 85            | $^\circ\text{C}$ |
| Storage temperature   | $T_{STG}$ | –                   | - 65 to + 150           | $^\circ\text{C}$ |

Table 14-2. DC Electrical Characteristics

 $(T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  to  $5.5\text{ V}$ )

| Parameter           | Symbol    | Conditions                                  | Min                              | Typ            | Max            | Unit         |   |
|---------------------|-----------|---|----------------------------------|----------------|----------------|--------------|---|
| Input high voltage  | $V_{IH1}$ | Ports 0, 1, and RESET                       | $V_{DD} = 3.0$ to $5.5\text{ V}$ | $0.8 V_{DD}$   | –              | $V_{DD}$     | V |
|                     | $V_{IH2}$ | $X_{IN}$ and $X_{OUT}$                      |                                  | $V_{DD} - 0.1$ |                |              |   |
| Input low voltage   | $V_{IL1}$ | Ports 0, 1, and RESET                       | $V_{DD} = 3.0$ to $5.5\text{ V}$ | –              | –              | $0.2 V_{DD}$ | V |
|                     | $V_{IL2}$ | $X_{IN}$ and $X_{OUT}$                      |                                  |                |                | 0.1          |   |
| Output high voltage | $V_{OH}$  | $I_{OH} = -10\text{ mA}$<br>ports 0, 1, 2   | $V_{DD} = 4.5$ to $5.5\text{ V}$ | $V_{DD} - 1.5$ | $V_{DD} - 0.4$ | –            | V |
| Output low voltage  | $V_{OL}$  | $I_{OL} = 25\text{ mA}$<br>port 0, 1, and 2 | $V_{DD} = 4.5$ to $5.5\text{ V}$ | –              | 0.4            | 2.0          | V |

Table 14-2. DC Electrical Characteristics (Continued)

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.0 V to 5.5 V)

| Parameter                   | Symbol            | Conditions                                    | Min                                | Typ | Max | Unit |    |
|-----------------------------|-------------------|---|------------------------------------|-----|-----|------|----|
| Input high leakage current  | I <sub>LIH1</sub> | All inputs except I <sub>LIH2</sub>           | V <sub>IN</sub> = V <sub>DD</sub>  | -   | -   | 1    | uA |
|                             | I <sub>LIH2</sub> | X <sub>IN</sub> , X <sub>OUT</sub>            | V <sub>IN</sub> = V <sub>DD</sub>  |     |     | 20   |    |
| Input low leakage current   | I <sub>LIL1</sub> | All inputs except I <sub>LIL2</sub> and RESET | V <sub>IN</sub> = 0 V              | -   | -   | -1   | uA |
|                             | I <sub>LIL2</sub> | X <sub>IN</sub> , X <sub>OUT</sub>            | V <sub>IN</sub> = 0 V              |     |     | -20  |    |
| Output high leakage current | I <sub>LOH</sub>  | All outputs                                   | V <sub>OUT</sub> = V <sub>DD</sub> | -   | -   | 2    | uA |
| Output low leakage current  | I <sub>LOL</sub>  | All outputs                                   | V <sub>OUT</sub> = 0 V             | -   | -   | -2   | uA |
| Pull-up resistors           | R <sub>P</sub>    | V <sub>IN</sub> = 0 V<br>Ports 0-2            | V <sub>DD</sub> = 5 V              | 30  | 47  | 70   | kΩ |
|                             |                   | RESET   | V <sub>DD</sub> = 5 V              | 100 | 200 | 350  |    |
| Supply current              | I <sub>DD1</sub>  | Run mode<br>16 MHz CPU clock                  | V <sub>DD</sub> = 5V ± 10%         | -   | 11  | 20   | mA |
|                             |                   | 8 MHz CPU clock                               | V <sub>DD</sub> = 3.3 V            |     | 3   | 6    |    |
|                             | I <sub>DD2</sub>  | Idle mode<br>16 MHz CPU clock                 | V <sub>DD</sub> = 5V ± 10%         | -   | 5   | 8    |    |
|                             |                   | 8 MHz CPU clock                               | V <sub>DD</sub> = 3.3 V            |     | 0.7 | 2.5  |    |
|                             | I <sub>DD3</sub>  | Stop mode                                     | V <sub>DD</sub> = 5V ± 10%         | -   | 65  | 100  |    |
| V <sub>DD</sub> = 3.3 V     |                   |   |                                    | 45  | 80  |      |    |

**NOTE:** D.C electrical values for supply current (I<sub>DD1</sub> to I<sub>DD3</sub>) do not include current drawn through internal pull-up resistors, output port drive current and ADC module.

Table 14-3. AC Electrical Characteristics

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.0 V to 5.5 V)

| Parameter                       | Symbol                                   | Conditions                               | Min | Typ | Max | Unit |
|---------------------------------|--|--|-----|-----|-----|------|
| Interrupt input high, low width | t <sub>INTH</sub> ,<br>t <sub>INTL</sub> | INT0, INT1<br>V <sub>DD</sub> = 5V ± 10% | –   | 200 | –   | ns   |
| RESET input low width           | t <sub>RSL</sub>                         | Input<br>V <sub>DD</sub> = 5V ± 10%      | –   | 1   | –   | us   |

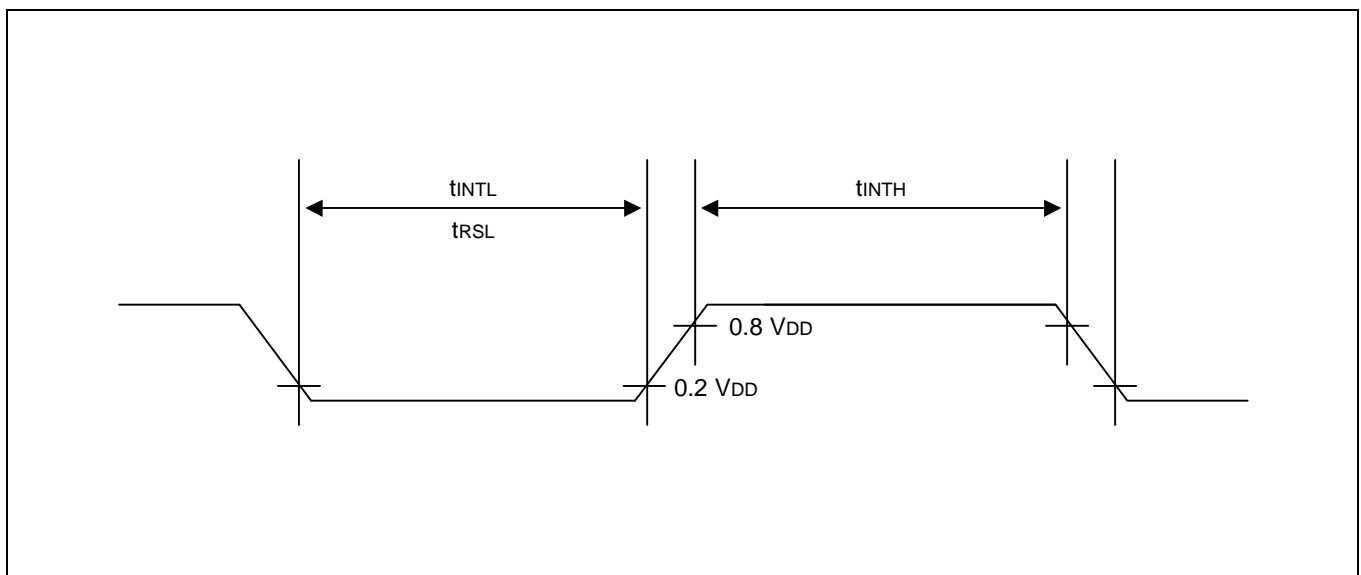


Figure 14-1. Input Timing Measurement Points

Table 14-4. Oscillator Characteristics

(T<sub>A</sub> = -40°C to +85°C)

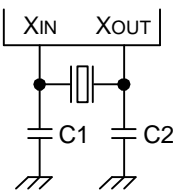
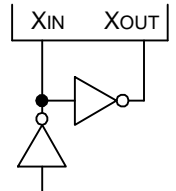
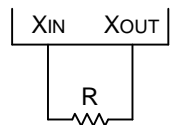
| Oscillator              | Clock Circuit   | Test Condition   | Min    | Typ    | Max     | Unit |
|-------------------------|---|--|--------|--------|---------|------|
| Main crystal or ceramic |  | V <sub>DD</sub> = 4.5 to 5.5 V<br>V <sub>DD</sub> = 3.0 to 4.5 V     | 1<br>1 | –<br>– | 16<br>8 | MHz  |
| External clock          |  | V <sub>DD</sub> = 4.5 to 5.5 V<br>V <sub>DD</sub> = 3.0 to 4.5 V     | 1<br>1 | –<br>– | 16<br>8 |      |
| RC oscillator           |  | V <sub>DD</sub> = 5 V, R = 10 KΩ<br>V <sub>DD</sub> = 3 V, R = 22 KΩ | –<br>– | 4<br>2 | –<br>–  |      |

Table 14-5. Oscillation Stabilization Time

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.0 V to 5.5 V)

| Oscillator                         | Test Condition  | Min | Typ                               | Max | Unit |
|------------------------------------|---|-----|-----------------------------------|-----|------|
| Main crystal                       | f <sub>OSC</sub> > 1.0 MHz  | –   | –                                 | 20  | ms   |
| Main ceramic                       | Oscillation stabilization occurs when V <sub>DD</sub> is equal to the minimum oscillator voltage range. | –   | –                                 | 10  |      |
| External clock (main system)       | X <sub>IN</sub> input high and low width (t <sub>XH</sub> , t <sub>XL</sub> )                           | 25  | –                                 | 500 | ns   |
| Oscillator stabilization wait time | t <sub>WAIT</sub> when released by a reset <sup>(1)</sup>   | –   | 2 <sup>16</sup> /f <sub>OSC</sub> | –   | ms   |
|                                    | t <sub>WAIT</sub> when released by an interrupt <sup>(2)</sup>  | –   | –                                 | –   |      |

**NOTES:**

- f<sub>OSC</sub> is the oscillator frequency.
- The duration of the oscillator stabilization wait time, t<sub>WAIT</sub>, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

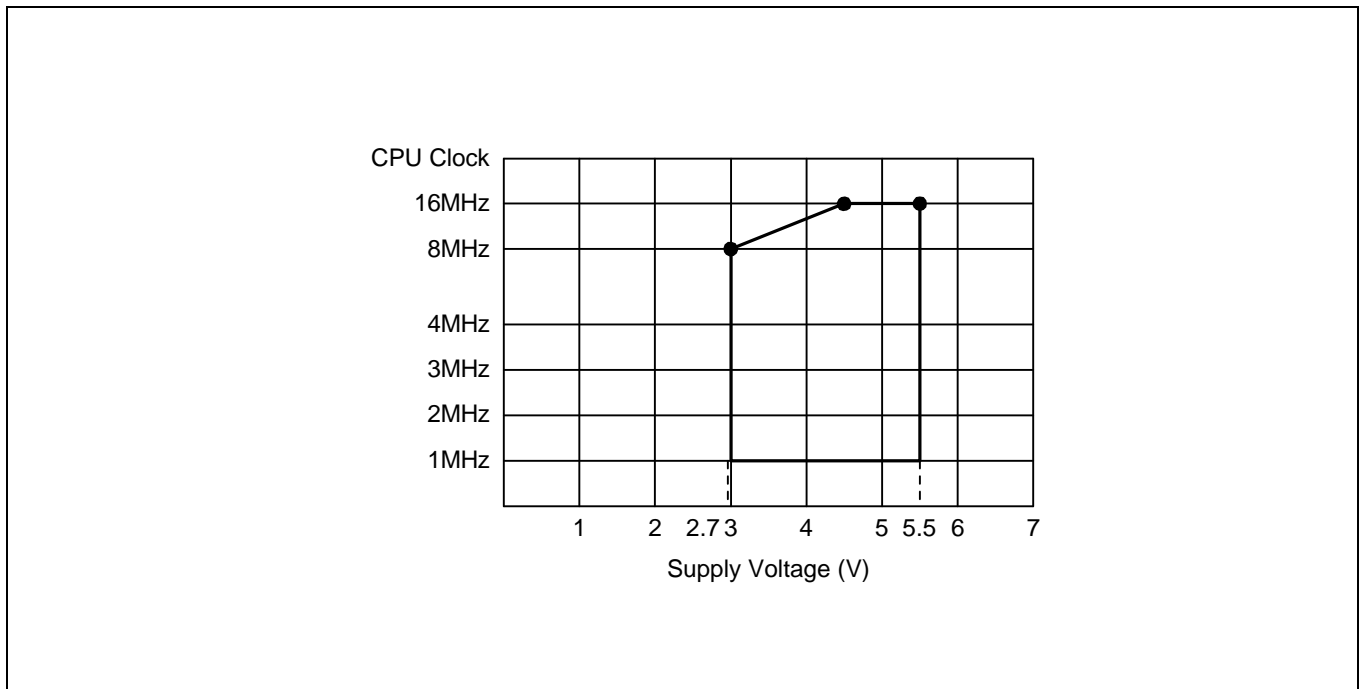


Figure 14-2. Operating Voltage Range

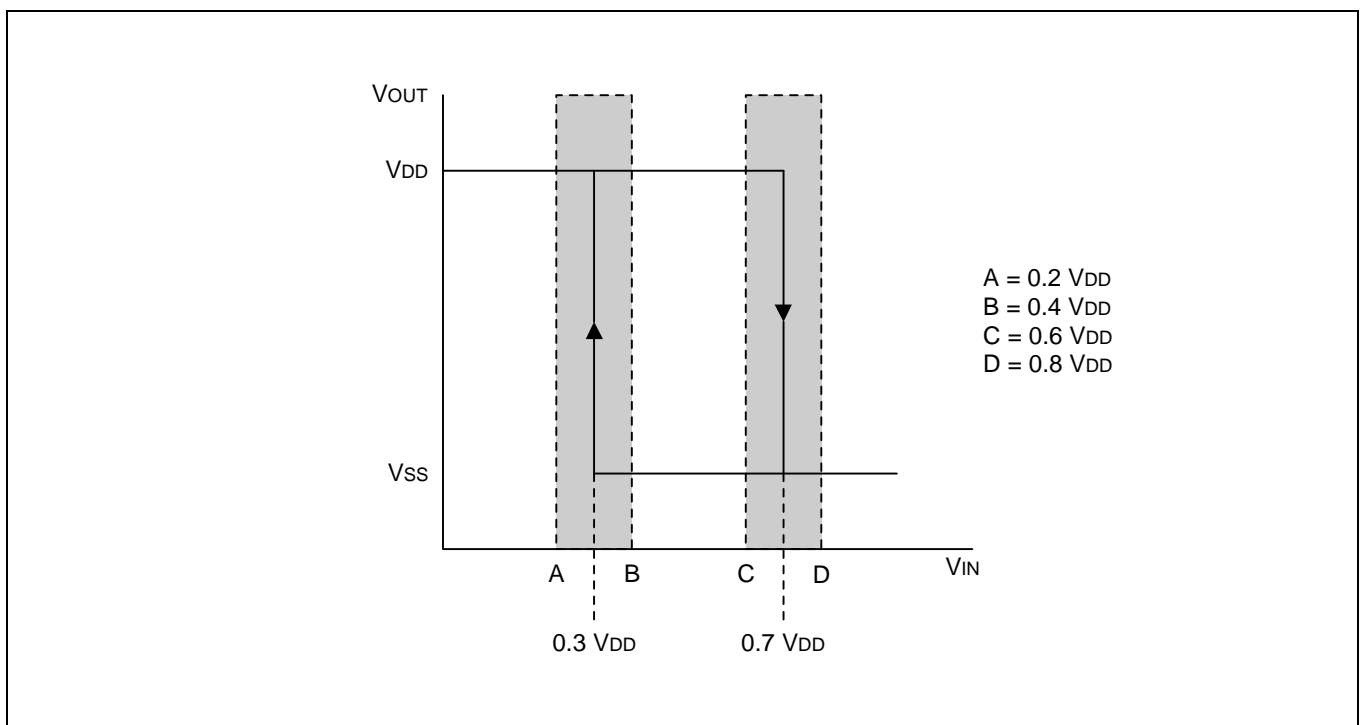


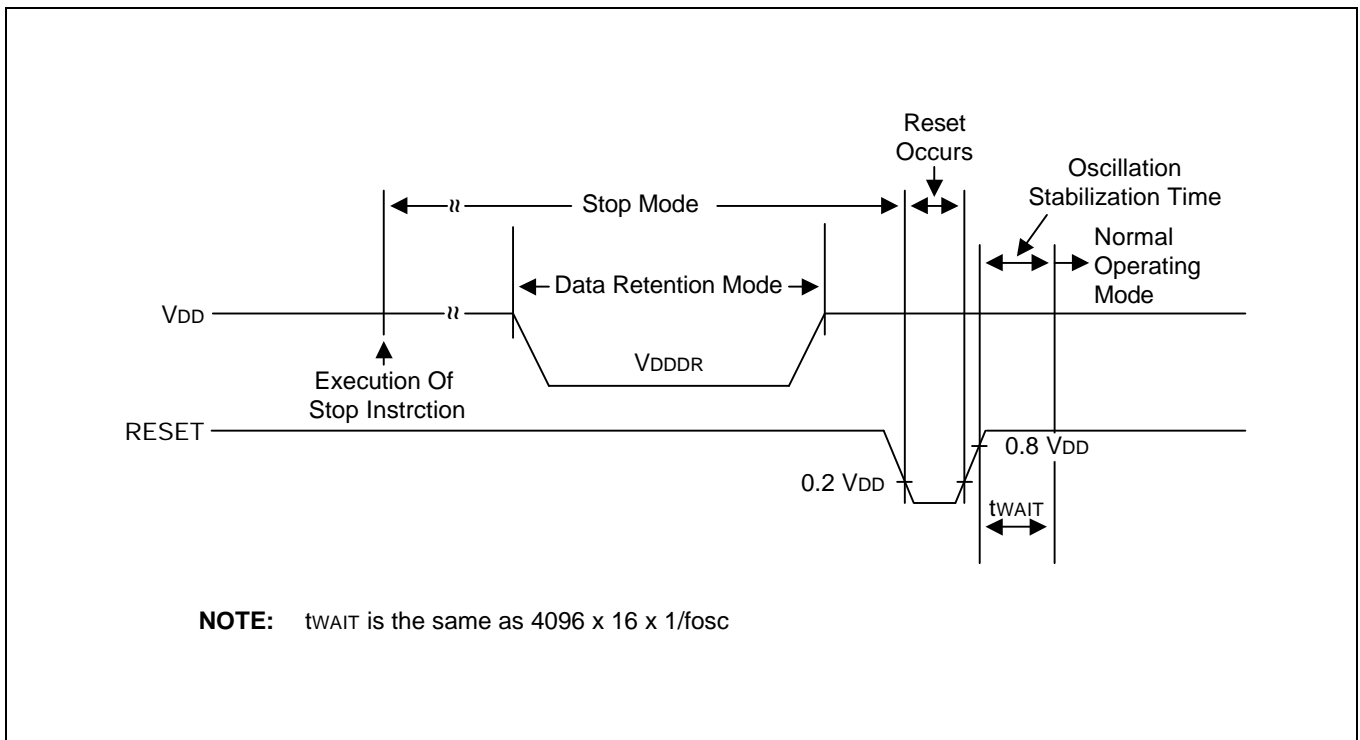
Figure 14-3. Schmitt Trigger Input Characteristics Diagram

**Table 14-6. Data Retention Supply Voltage in Stop Mode**

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  to  $5.5\text{ V}$ )

| Parameter                     | Symbol     | Conditions                           | Min | Typ | Max | Unit          |
|-------------------------------|------------|--------------------------------------|-----|-----|-----|---------------|
| Data retention supply voltage | $V_{DDDR}$ | Stop mode                            | 2.0 | –   | 5.5 | V             |
| Data retention supply current | $I_{DDDR}$ | Stop mode; $V_{DDDR} = 2.0\text{ V}$ | –   | 0.1 | 5   | $\mu\text{A}$ |

**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.



**Figure 14-4. Stop Mode Release Timing When Initiated by a RESET**



Table 14-7. A/D Converter Electrical Characteristics

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.0 V to 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter                    | Symbol            | Test Conditions  | Min              | Typ                    | Max                   | Unit |
|------------------------------|-------------------|--|------------------|------------------------|-----------------------|------|
| Total accuracy               | –                 | V <sub>DD</sub> = 5.12 V<br>CPU clock = 10 MHz<br>AV <sub>REF</sub> = 5.12 V<br>AV <sub>SS</sub> = 0 V | –                | –                      | ± 3                   | LSB  |
| Integral linearity error     | ILE               | –  | –                | –                      | ± 2                   |      |
| Differential linearity error | DLE               | –  | –                | –                      | ± 1                   |      |
| Offset error of top          | EOT               | –  | –                | ± 1                    | ± 3                   |      |
| Offset error of bottom       | EOB               | –  | –                | ± 1                    | ± 2                   |      |
| Conversion time (1)          | t <sub>CON</sub>  | f <sub>OSC</sub> = 10 MHz  | –                | 50x4/ f <sub>OSC</sub> | –                     | μs   |
| Analog input voltage         | V <sub>IAN</sub>  | –  | AV <sub>SS</sub> | –                      | AV <sub>REF</sub>     | V    |
| Analog input impedance       | R <sub>AN</sub>   | –  | 2                | –                      | –                     | MΩ   |
| ADC reference voltage        | AV <sub>REF</sub> | –  | 3.0              | –                      | V <sub>DD</sub>       | V    |
| ADC reference ground         | AV <sub>SS</sub>  | –  | V <sub>SS</sub>  | –                      | V <sub>SS</sub> + 0.3 | V    |
| Analog input current         | I <sub>ADIN</sub> | AV <sub>REF</sub> = V <sub>DD</sub> = 5 V  | –                | –                      | 10                    | μA   |
| Analog block current (2)     | I <sub>ADC</sub>  | AV <sub>REF</sub> = V <sub>DD</sub> = 5 V<br>conversion time = 20 μs                                   |                  | 1                      | 3                     | mA   |
|                              |                   | AV <sub>REF</sub> = V <sub>DD</sub> = 3 V<br>conversion time = 20 μs                                   |                  | 0.5                    | 1.5                   | mA   |
|                              |                   | AV <sub>REF</sub> = V <sub>DD</sub> = 5 V<br>when power down mode                                      |                  | 100                    | 500                   | nA   |

**NOTES:**

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I<sub>ADC</sub> is operating current during A/D conversion.

Table 14-8. LVD Circuit Characteristics

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 3.0 V to 5.5V)

| Parameter                                  | Symbol            | Conditions                   | Min | Typ | Max    | Unit |
|--|-------------------|------------------------------|-----|-----|--------|------|
| Power-on reset voltage high                | V <sub>DDH</sub>  |                              | 3.0 |     | 5.5    | V    |
| Power-on reset voltage low                 | V <sub>DDL</sub>  |                              | 0   | 2.6 | 3.0    | V    |
| Power supply voltage rise time             | t <sub>r</sub>    |                              | 10  |     | (note) | us   |
| Power supply voltage off time              | t <sub>off</sub>  |                              | 0.5 |     |        | sec  |
| Power-on reset circuit consumption current | I <sub>DDPR</sub> | V <sub>DD</sub> = 5 V ± 10 % |     | 65  | 100    | uA   |
|  |                   | V <sub>DD</sub> = 3 V        |     | 45  | 80     | uA   |

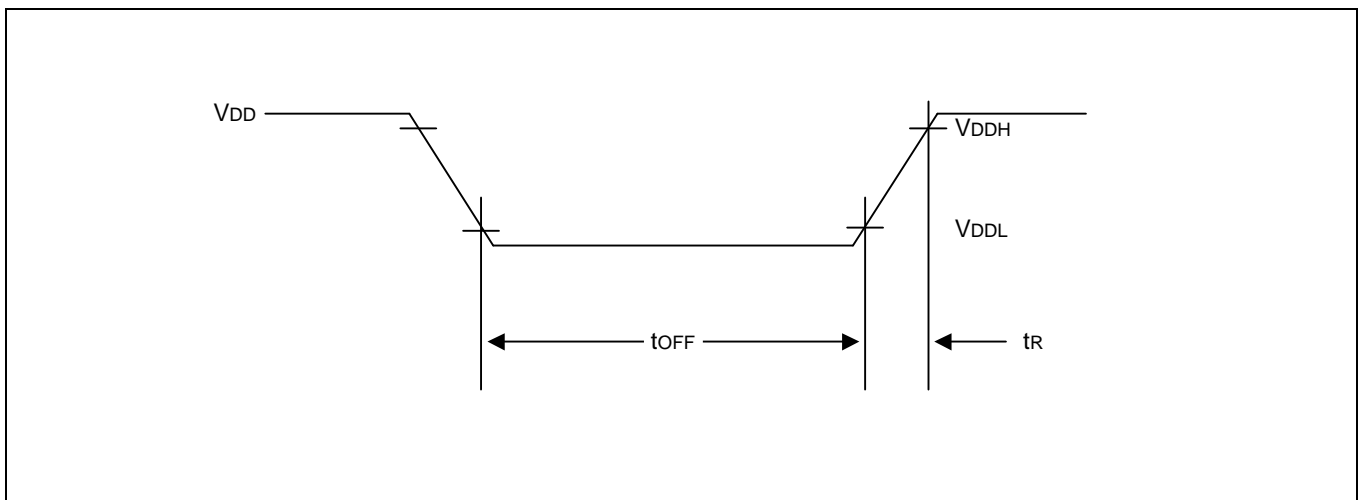
**NOTE:** Oscillation stabilization time = 2<sup>16</sup>/fx (= 6.55 ms at fx = 10 MHz)

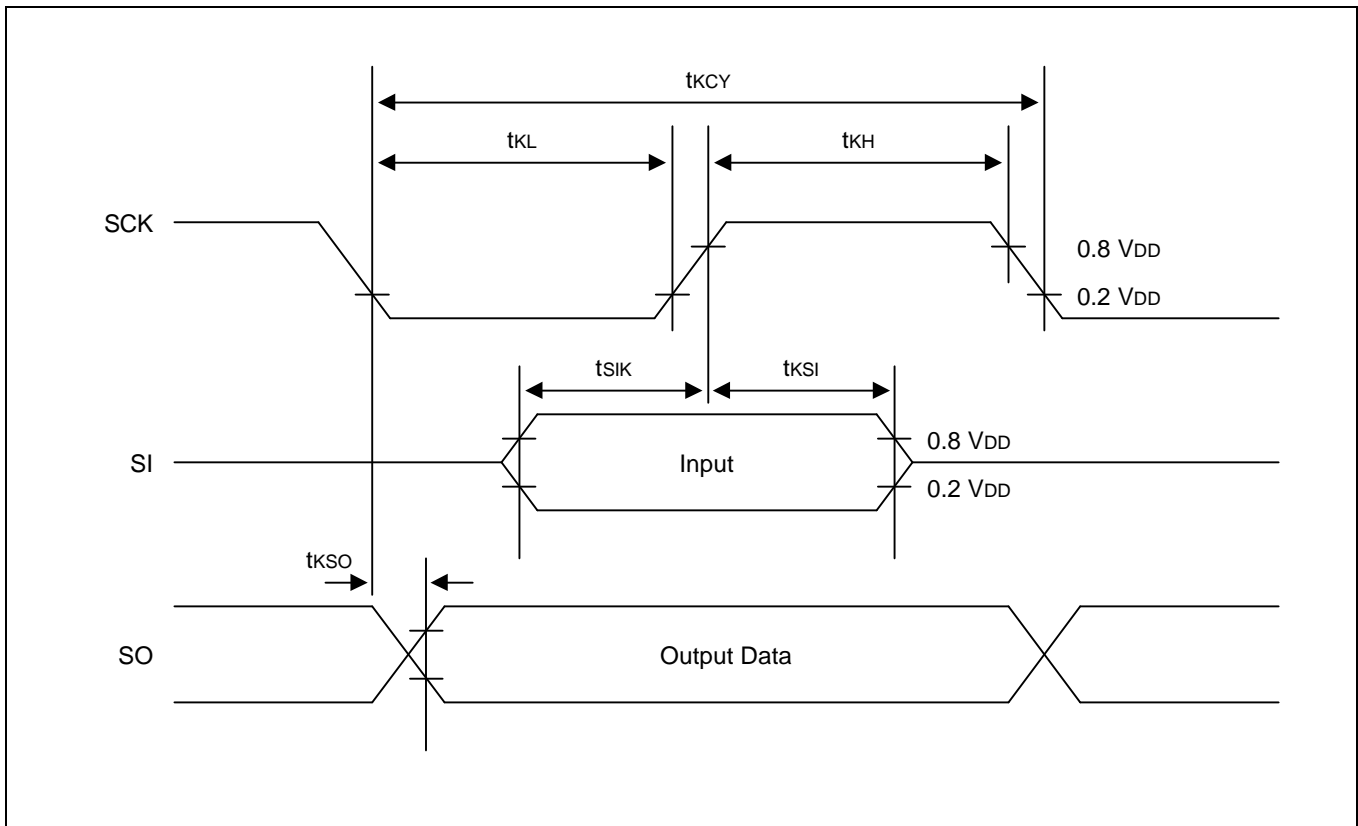
Figure 14-5. LVD Reset Timing

**Table 14-9. Serial I/O Timing Characteristics**

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  to  $5.5\text{ V}$ )

| Parameter                  | Symbol           | Conditions          | Min              | Typ | Max | Unit |
|----------------------------|------------------|---------------------|------------------|-----|-----|------|
| SCK Cycle Time             | $t_{CKY}$        | External SCK source | 1000             | -   | -   | ns   |
|                            |                  | Internal SCK source | 1000             |     |     |      |
| SCK High, Low Width        | $t_{KH}, t_{KL}$ | External SCK source | 500              | -   | -   |      |
|                            |                  | Internal SCK source | $t_{CKY}/2 - 50$ |     |     |      |
| SI Setup Time to SCK Low   | $t_{SIK}$        | External SCK source | 250              | -   | -   |      |
|                            |                  | Internal SCK source | 250              |     |     |      |
| SI Hold Time to SCK High   | $t_{KSI}$        | External SCK source | 400              | -   | -   |      |
|                            |                  | Internal SCK source | 400              |     |     |      |
| Output Delay for SCK to SO | $t_{KSO}$        | External SCK source | -                | -   | 300 |      |
|                            |                  | Internal SCK source | -                |     | 250 |      |

**NOTE:** "SCK" means serial I/O clock frequency, "SI" means serial data input, and "SO" means serial data output.



**Figure 14-6. Serial Data Transfer Timing**

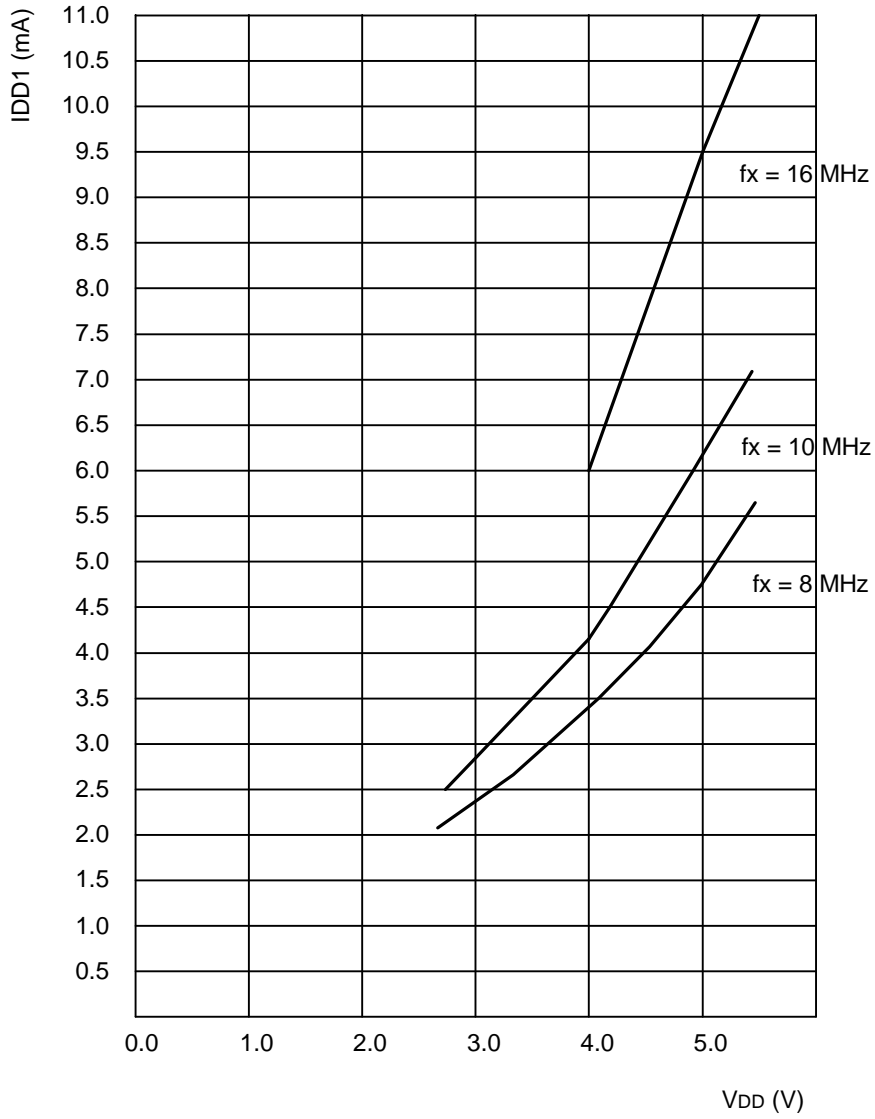
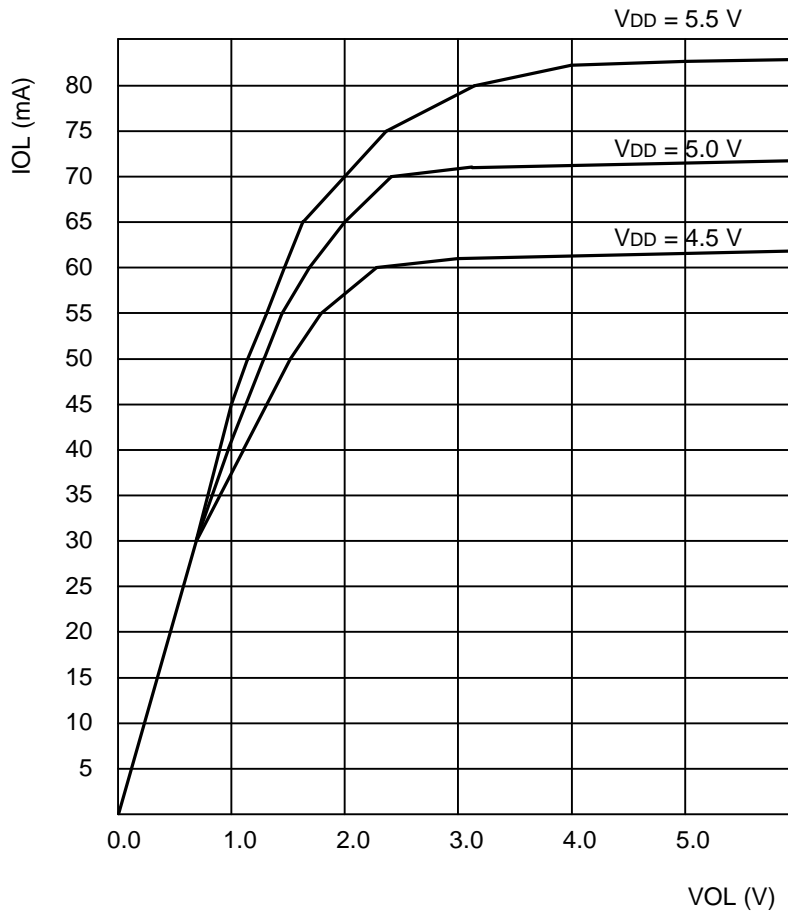


Figure 14-7.  $I_{DD1}$  vs  $V_{DD}$

Figure 14-8.  $I_{OL}$  vs  $V_{OL}$

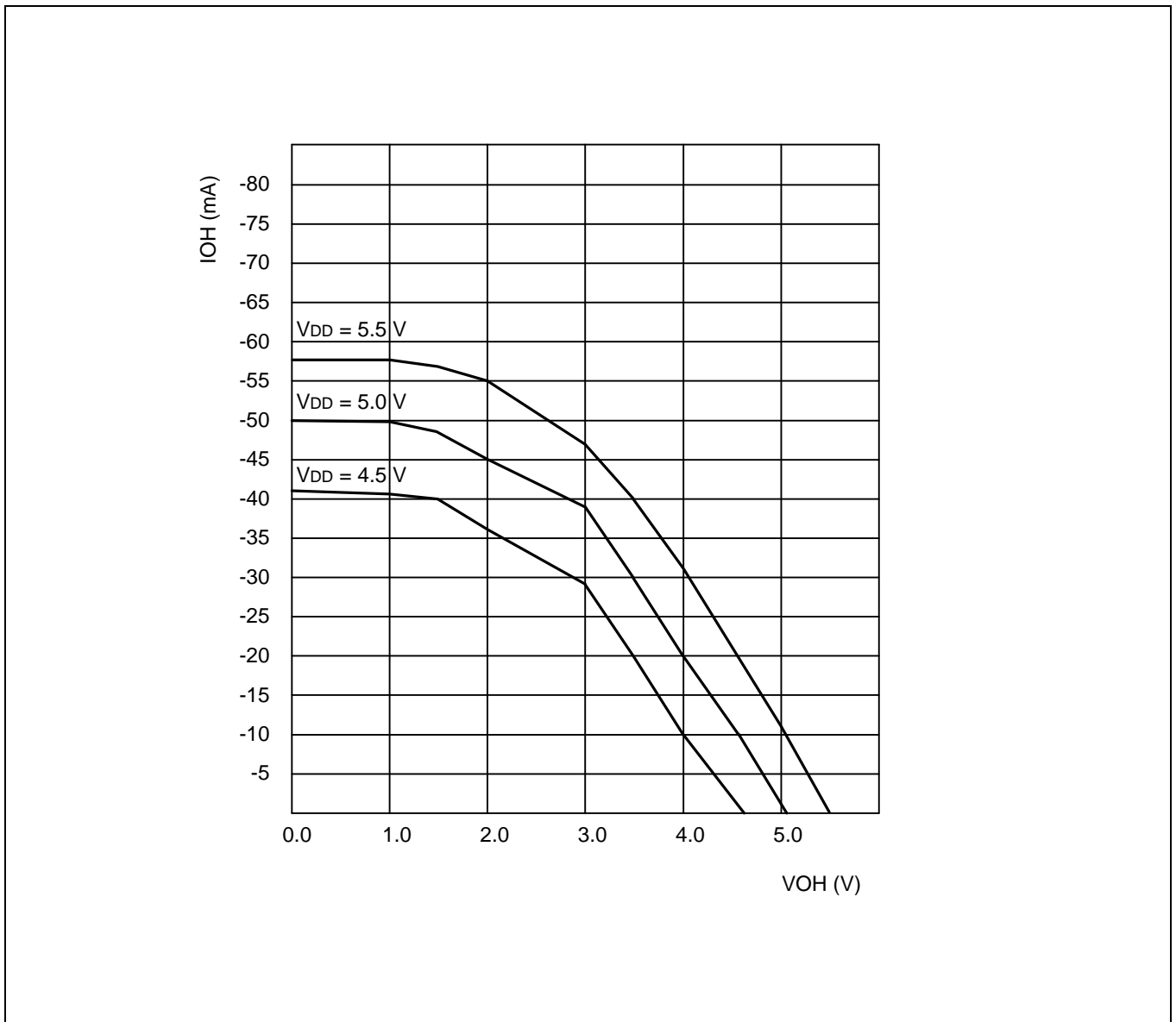


Figure 14-9.  $I_{OH}$  vs  $V_{OH}$

# 15 MECHANICAL DATA

## OVERVIEW

The S3C9432/C9434 is available in a 20-pin SDIP package (Samsung: 20-DIP-300A), a 20-pin SOP package (Samsung: 20-SOP-375), a 18-pin DIP package (Samsung: 18-DIP-300A). Package dimensions are shown in Figure 15-1, 15-2, and 15-3.

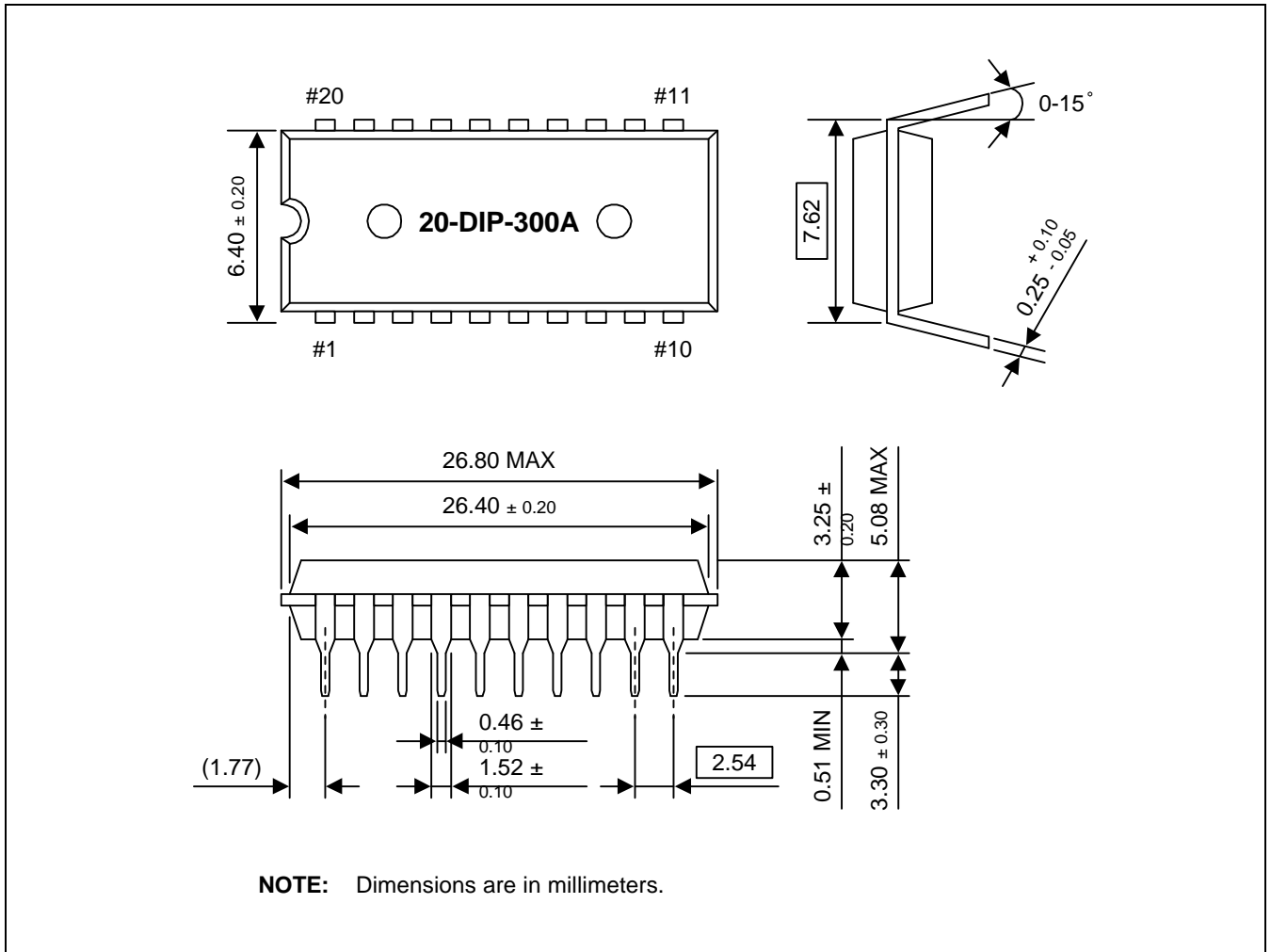


Figure 15-1. 20-DIP-300A Package Dimensions

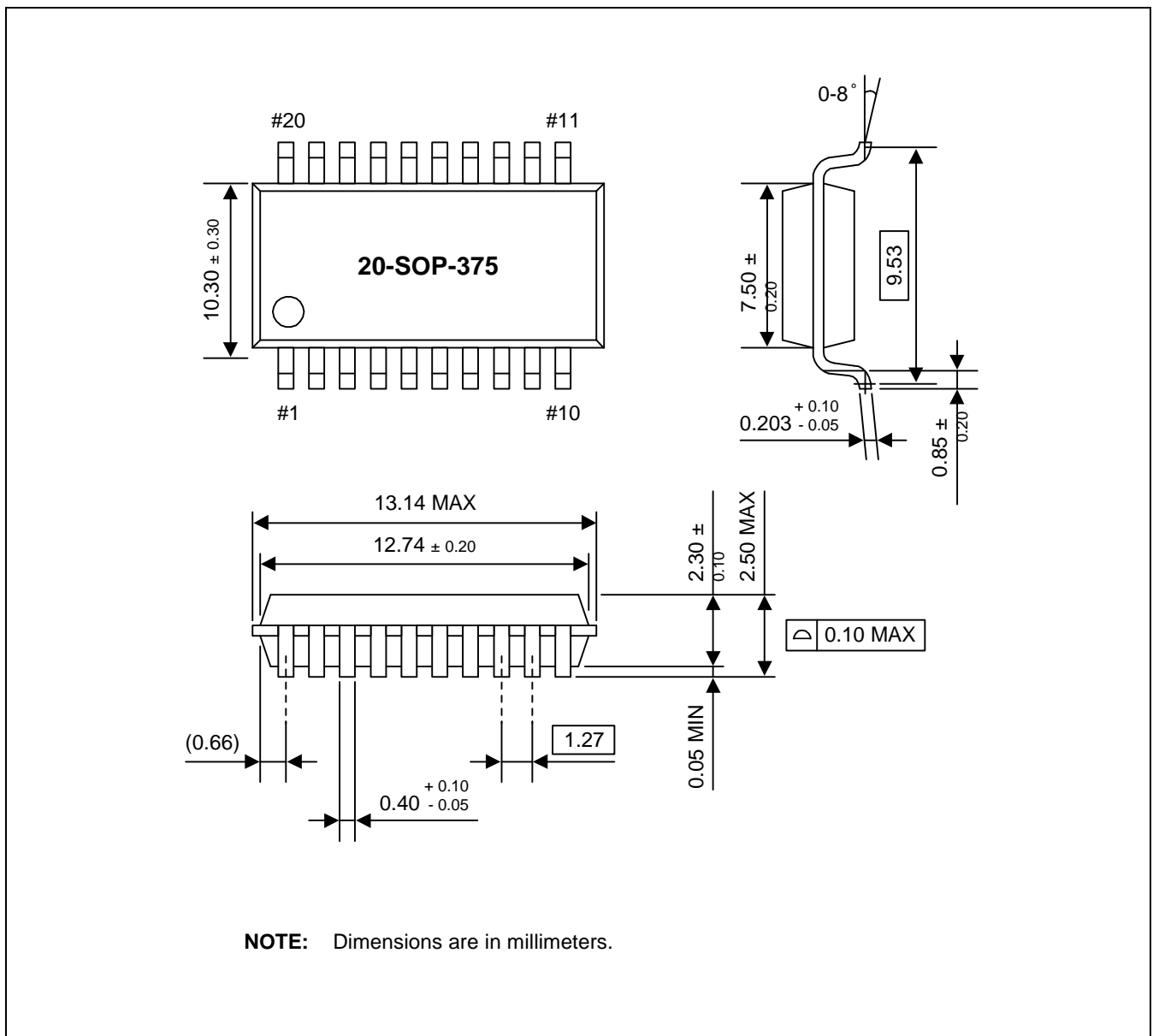


Figure 15-2. 20-SOP-375 Package Dimensions



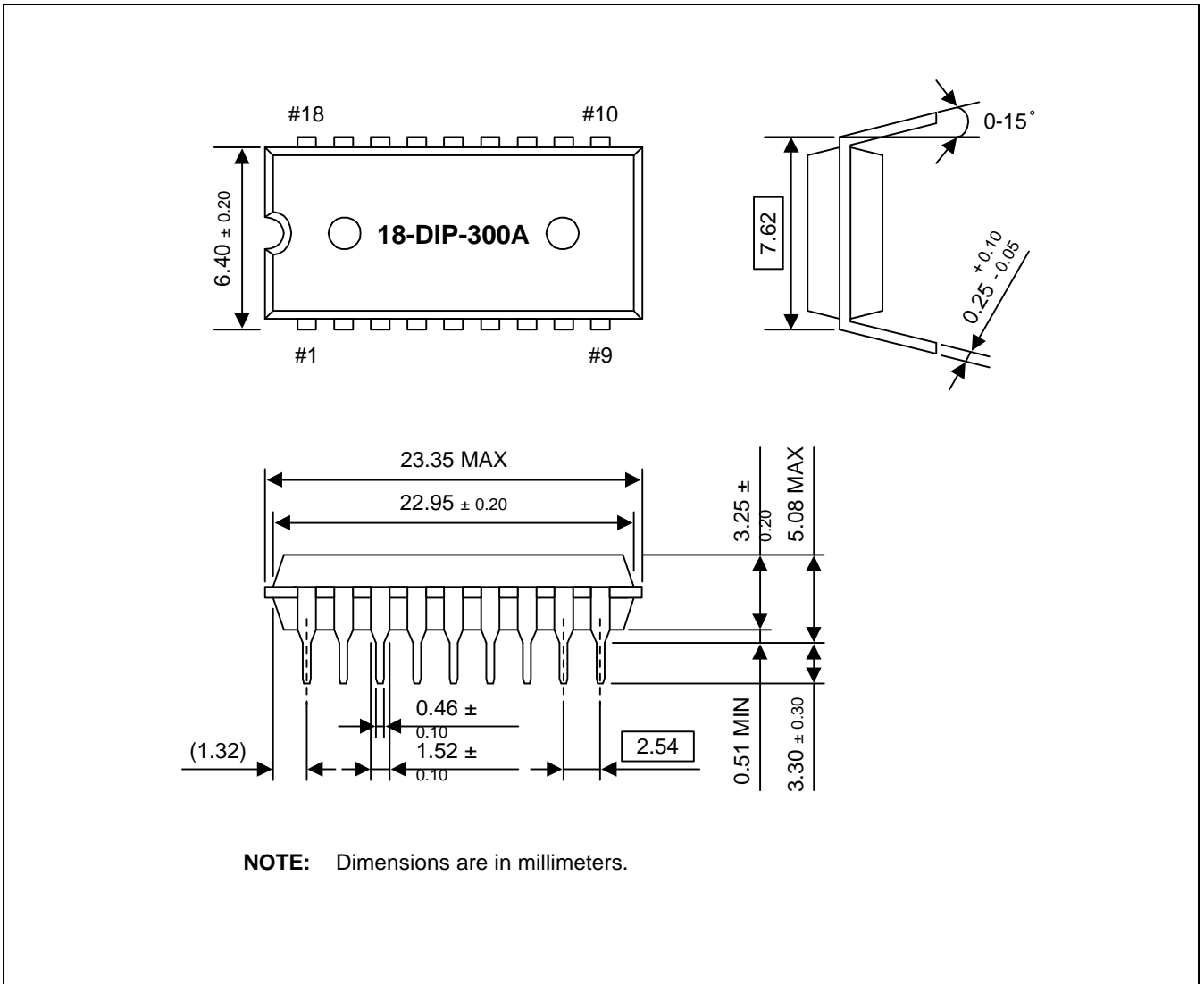


Figure 15-3. 18-DIP-300A Package Dimensions

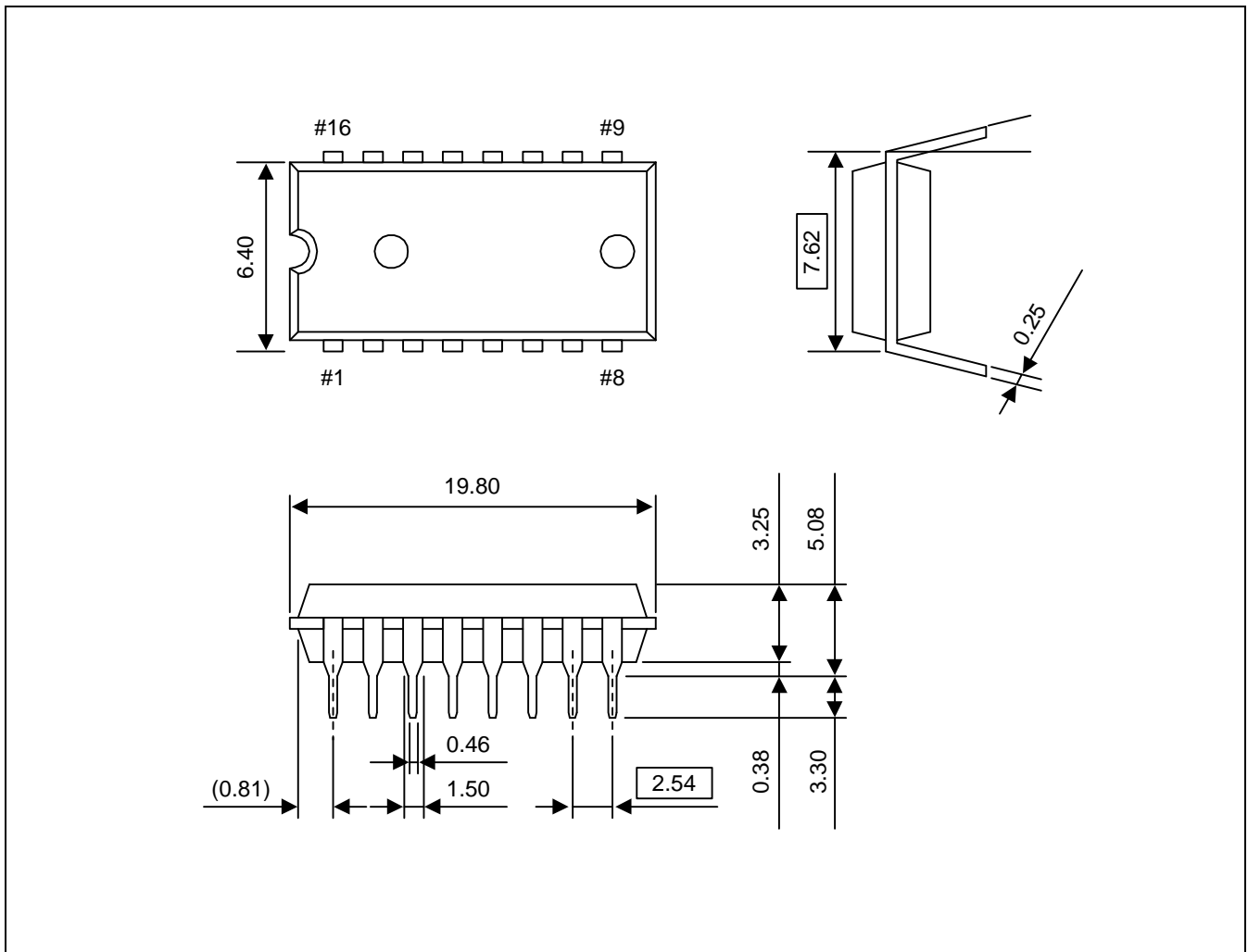


Figure 15-4. 16-DIP-300A Package Dimensions

# 16

## S3P9434 OTP

### OVERVIEW

The S3P9434 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C9432/C9434 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P9434 is fully compatible with the S3C9432/C9434, in function, in D.C. electrical characteristics, and in pin configuration. Because of its simple programming requirements, the S3P9434 is ideal for use as an evaluation chip for the S3C9432/C9434.

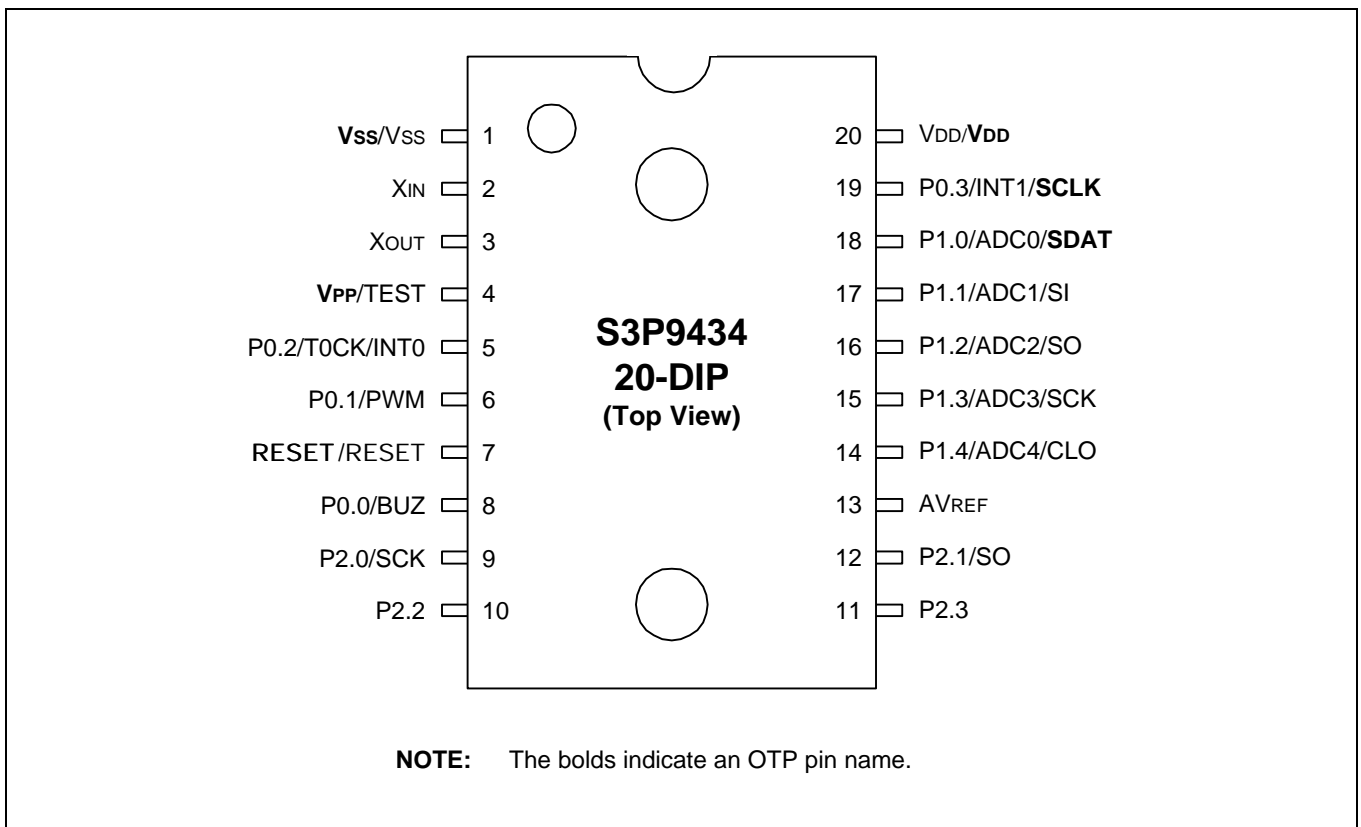


Figure 16-1. Pin Assignment Diagram (20-Pin DIP Package)

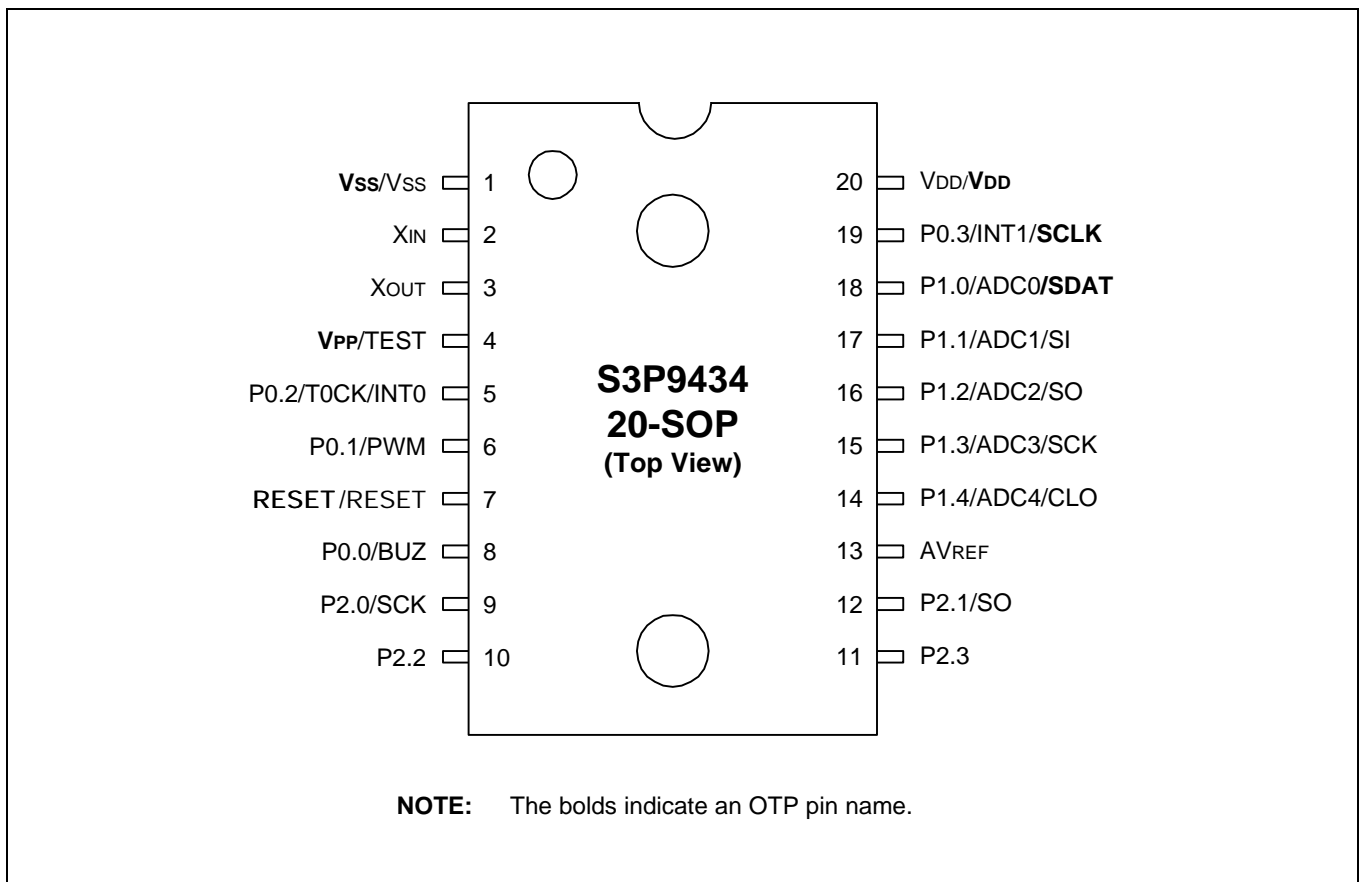


Figure 16-2. Pin Assignment Diagram (20-Pin SOP Package)

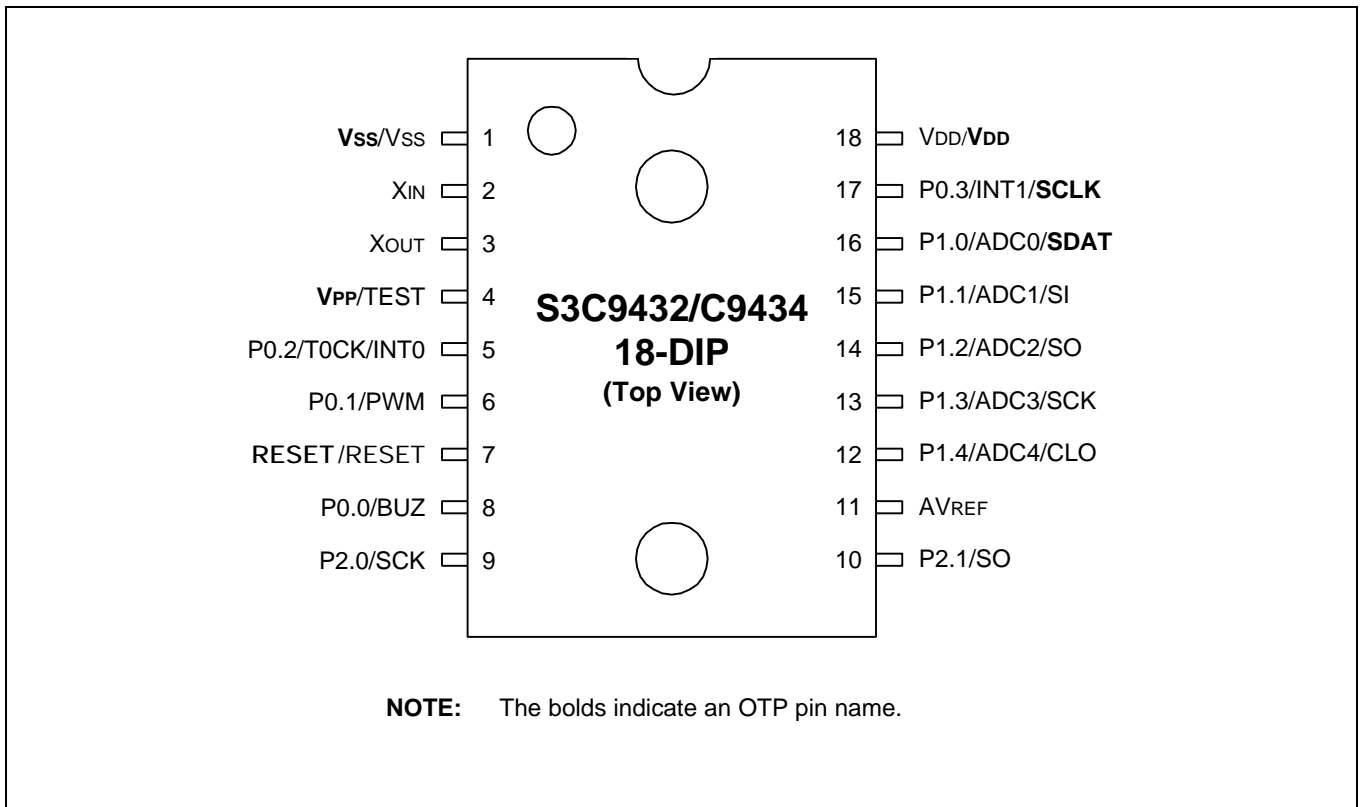


Figure 16-3. Pin Assignment Diagram (18-Pin DIP Package)

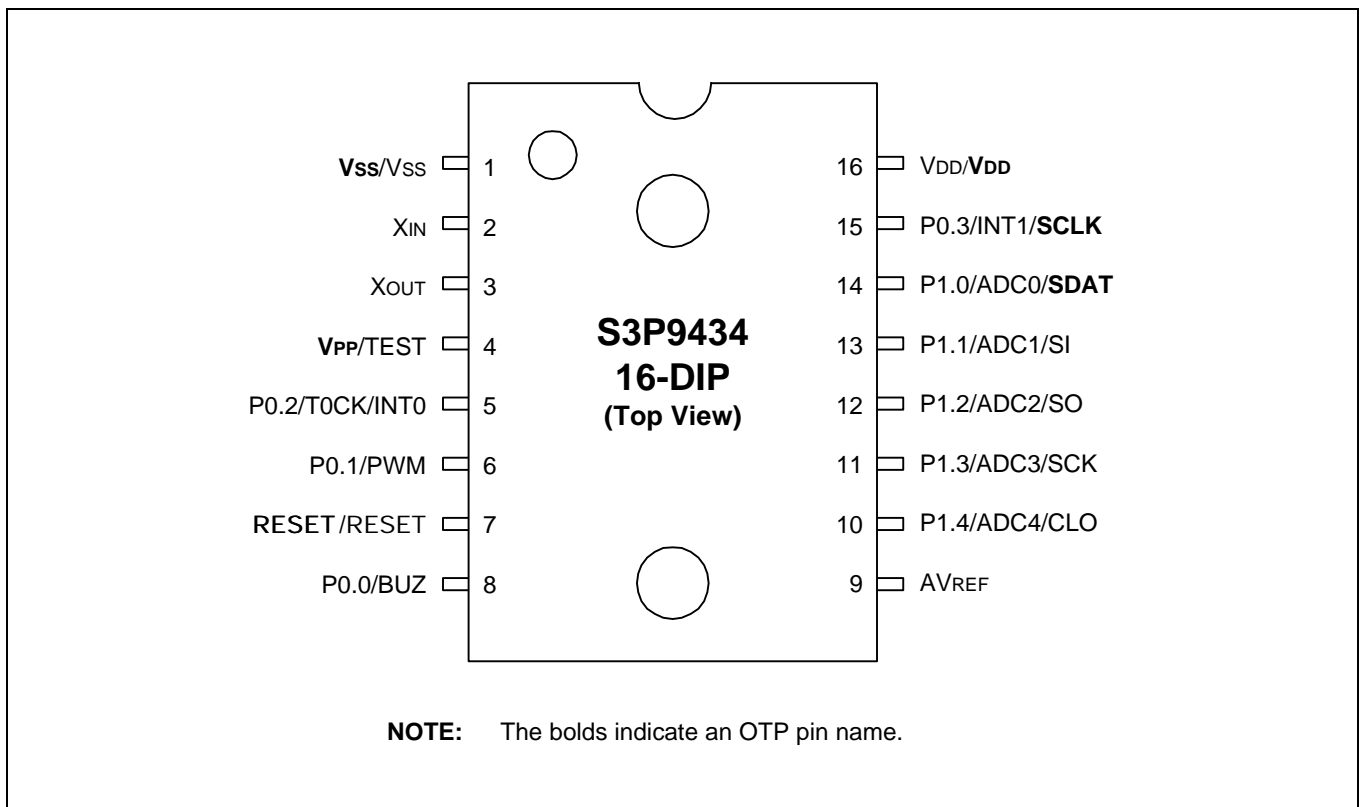


Figure 16-4. Pin Assingment Diagram (16-Pin DIP Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

| Main Chip<br>Pin Name            | During Programming               |  |     |   |
|----------------------------------|----------------------------------|--|-----|---|
|                                  | Pin Name                         | Pin No.  | I/O | Function  |
| P0.3                             | SDAT                             | 18 (20-pin)<br>16 (18-pin)                         | I/O | Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned   |
| P0.2                             | SCLK                             | 19 (20-pin)<br>17 (18-pin)                         | I   | Serial clock pin (input only pin)   |
| TEST                             | V <sub>PP</sub> (TEST)           | 4  | I   | Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) |
| RESET                            | RESET                            | 7  | I   | Chip Initialization   |
| V <sub>DD</sub> /V <sub>SS</sub> | V <sub>DD</sub> /V <sub>SS</sub> | 20 (20-pin), 18 (18-pin)<br>1 (20-pin), 1 (18-pin) | I   | Logic power supply pin.   |

NOTE: ( ) means the SOP OTP pin number.

Table 16-2. Comparison of S3P9434 and S3C9432/C9434 Features

| Characteristic                       | S3P9434  | S3C9432/C9434             |
|--------------------------------------|--|---------------------------|
| Program Memory                       | 4 Kbyte EPROM  | 2K/4K byte mask ROM       |
| Operating Voltage (V <sub>DD</sub> ) | 3.0 V to 5.5 V   | 3.0 V to 5.5 V            |
| OTP Programming Mode                 | V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5 V |                           |
| Pin Configuration                    | 20 DIP/20 SOP/18 DIP                                   |                           |
| EPROM Programmability                | User Program 1 time                                    | Programmed at the factory |

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub> (TEST) pin of the S3P9434, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

| V <sub>DD</sub> | V <sub>PP</sub> (TEST) | REG/MEM | ADDRESS (A15-A0) | R/W | MODE                  |
|-----------------|------------------------|---------|------------------|-----|-----------------------|
| 5 V             | 5 V                    | 0       | 0000H            | 1   | EPROM read            |
|                 | 12.5 V                 | 0       | 0000H            | 0   | EPROM program         |
|                 | 12.5 V                 | 0       | 0000H            | 1   | EPROM verify          |
|                 | 12.5 V                 | 1       | 0E3FH            | 0   | EPROM read protection |

NOTE: "0" means Low level; "1" means High level.