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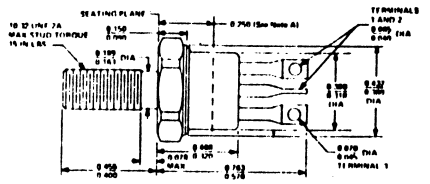
TYPES 2N5003, 2N5005, 2N5151, 2N5153
P-N-P SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use With 2N5002, 2N5004, 2N5152, 2N5154
- 15 mJ Reverse Energy Rating with I_C = 10 A and 4 V Reverse Bias

*mechanical data

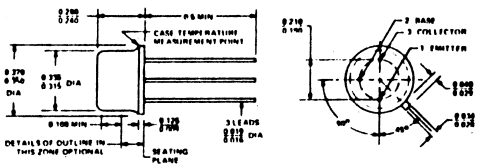
2N5003, 2N5005 — ALL TERMINALS ARE INSULATED FROM THE CASE



ALL JEDEC TO-59 DIMENSIONS AND NOTES ARE APPLICABLE

NOTES: A. Within this dimension, case diameter may vary.
B. Position of terminals with respect to the hexagon is not controlled.
C. The case temperature may be measured anywhere on the seating plane within 0.125 inch of the stud.
D. All dimensions are in inches unless otherwise specified.

2N5151, 2N5153 — THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



ALL JEDEC TO-39 DIMENSIONS AND NOTES ARE APPLICABLE

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5003 2N5005	2N5151 2N5153
Collector-Base Voltage	←—— −100 V* ——→	
Collector-Emitter Voltage (See Note 1)	←—— −80 V* ——→	
Emitter-Base Voltage	←—— −5.5 V* ——→	
Continuous Collector Current	−5 A*	−5 A*
Peak Collector Current (See Note 2)	−10 A*	−10 A
Continuous Base Current	−2 A*	−2.5 A*
Safe Operating Areas	See Figures 7* and 8	
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	50 W*	10 W*
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	33.3 W	6.7 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)		1 W*
Unclamped Inductive Load Energy (See Note 5)	←—— 15 mJ ——→	
Operating Collector Junction Temperature Range	−65°C to 200°C*	
Storage Temperature Range	−65°C to 200°C*	
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	←—— 300°C* ——→	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_w \leq 8.3$ ms, duty cycle $\leq 1\%$.
3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves, Figures 9 and 10.
4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/°C.
5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*†. L = 0.3 mH, R_{BB1} = 10 Ω, R_{BB2} = 100Ω, V_{BB1} = 10 V, V_{BB2} = 4 V, R_L = 0.1 Ω, V_{CC} = 10 V, I_{CM} = 10 A. Energy ≈ $I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

Quality Semi-Conductors