

OPERATION MODE

OPERATION MODE	\overline{CE}	\overline{OE}	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDS}

Note: x = don't care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V _{IN}	Input Voltage	- 0.3* to 7.0	V
V _{I/O}	Input and Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	0 to 70	°C

* - 3.0 V when measured at a pulse width of 50 ns (max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3*	-	0.8	V
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

* - 3.0 V when measured at a pulse width of 50 ns (max)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT		
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 1.0	μA		
I _{OH}	Output High Current	V _{OH} = 2.4 V	- 1.0	-	-	mA		
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.1	-	-	mA		
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}	-	-	± 1.0	μA		
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	Tcycle	min	-	-	80	mA
				1 μs	-	15	-	
I _{DDO2}	Operating Current	$\overline{CE} = 0.2$ V and R/W = V _{DD} - 0.2 V I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V	Tcycle	min	-	-	70	mA
				1 μs	-	10	-	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	-	-	3	mA		
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V V _{DD} = 2.0 to 5.5 V	-	-	60	μA		
			Ta = 25°C	-	4	8		
			Ta = 0° to 70°C	-	-	60		

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554001FL/FTL						UNIT
		-70L		-85L		-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	-	85	-	100	-	ns
t _{ACC}	Address Access Time	-	70	-	85	-	100	
t _{CO}	Chip Enable Access Time	-	70	-	85	-	100	
t _{OE}	Output Enable Access Time	-	35	-	45	-	50	
t _{COE}	Chip Enable Low to Output Active	10	-	10	-	10	-	
t _{OOE}	Output Enable Low to Output Active	5	-	5	-	5	-	
t _{OD}	Chip Enable Hige to Output High-Z	-	25	-	30	-	35	
t _{ODO}	Output Enable Hige to Output High-Z	-	25	-	30	-	35	
t _{OH}	Output Data Hold Time	10	-	10	-	10	-	

WRITE CYCLE

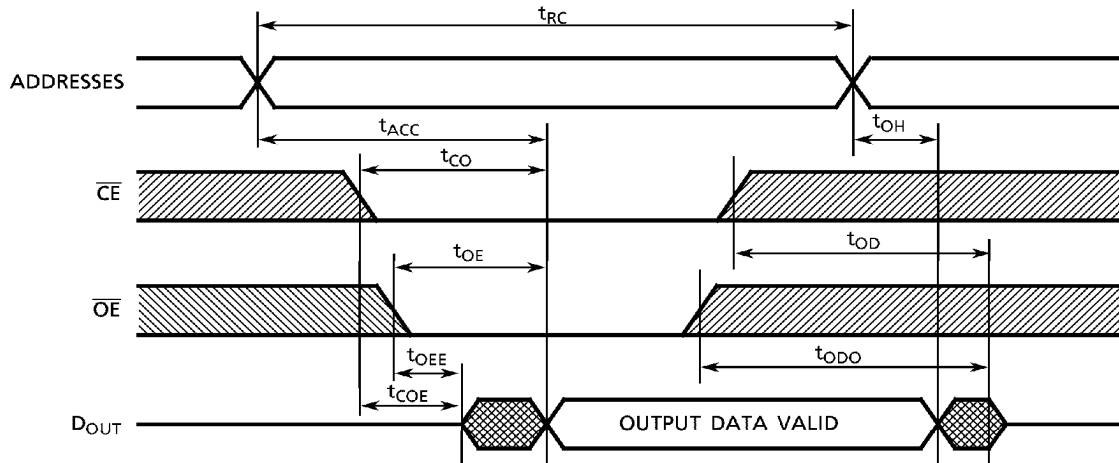
SYMBOL	PARAMETER	TC554001FL/FTL						UNIT
		-70L		-85L		-10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t _{WP}	Write Pulse Width	50	-	55	-	60	-	
t _{CW}	Chip Enable to End of Write	60	-	70	-	80	-	
t _{AS}	Address Setup Time	0	-	0	-	0	-	
t _{WR}	Write Recovery Time	0	-	0	-	0	-	
t _{ODW}	R/W Low to Output High-Z	-	25	-	30	-	35	
t _{OEW}	R/W High to Output Active	5	-	5	-	5	-	
t _{DS}	Data Setup Time	30	-	35	-	40	-	
t _{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

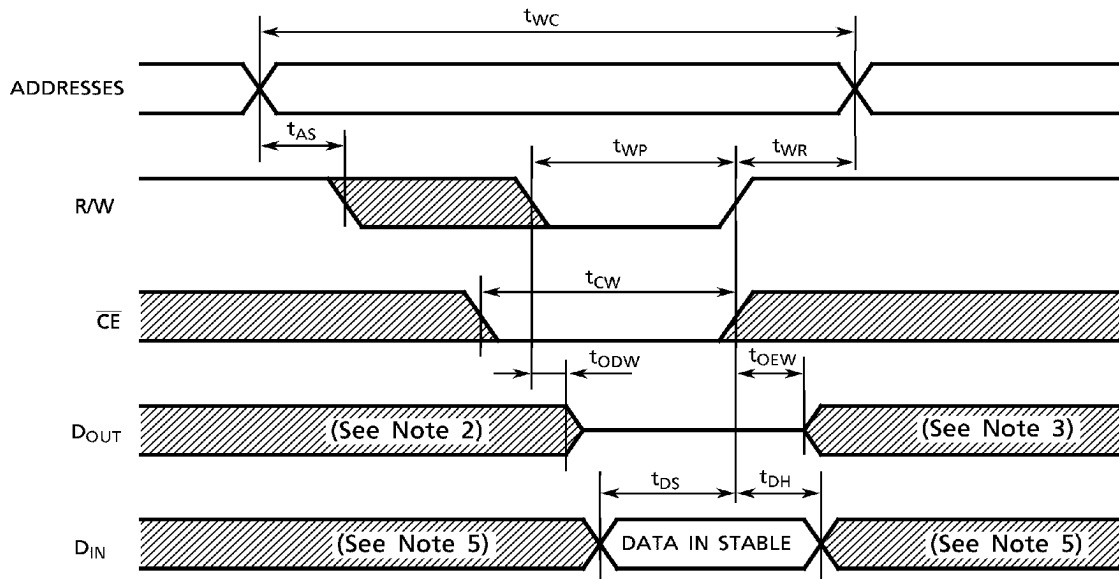
- Output Load : 30 pF + 1 TTL gate (-70L)
: 100 pF + 1 TTL gate (-85L, -10L)
- Input Pulse Level : 0.6 V, 2.4 V
- Timing Measurement V_{IN} : 1.5 V
Reference Level V_{OUT}: 1.5 V
- t_r, t_F : 5 ns

TIMING WAVEFORMS

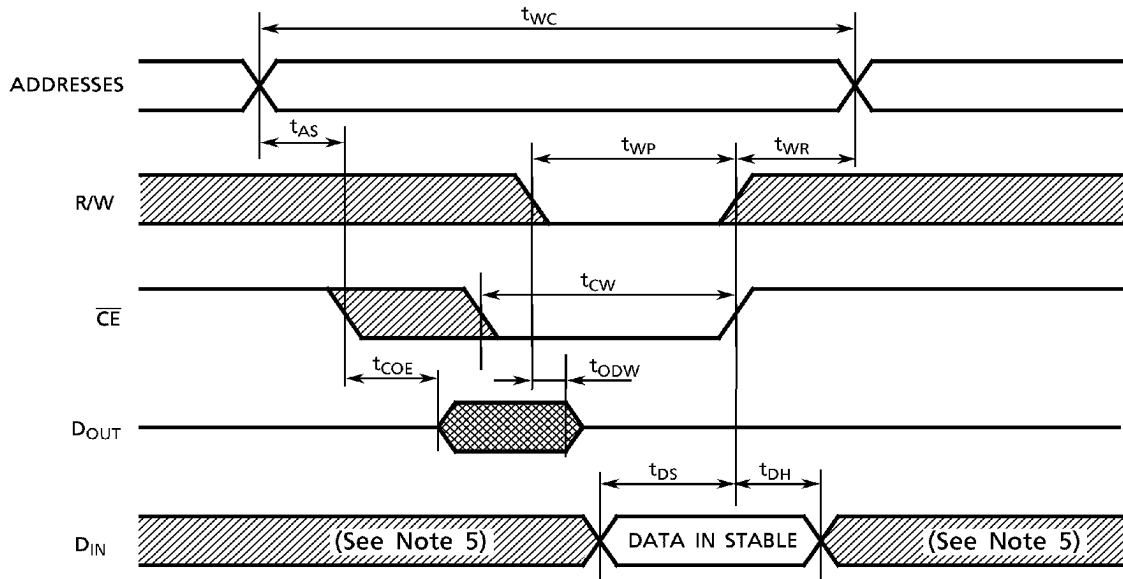
READ CYCLE (See Note 1)



WRITE CYCLE 1 (See Note 4) (R/W Controlled Write)



WRITE CYCLE 2 (See Note 4) ($\overline{\text{CE}}$ Controlled Write)



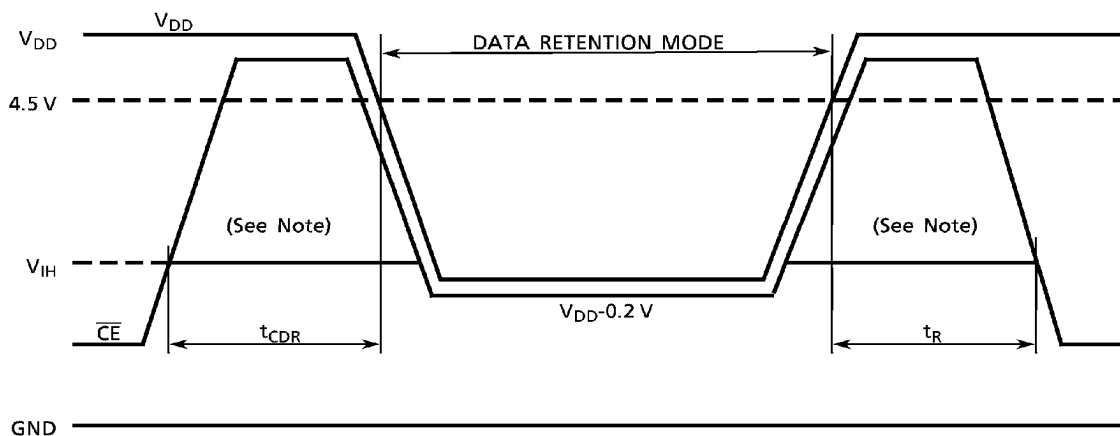
- (1) R/W is High for Read Cycle.
- (2) Assuming that $\overline{\text{CE}}$ Low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
- (3) Assuming that $\overline{\text{CE}}$ High transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
- (4) Assuming that $\overline{\text{OE}}$ is High for Write Cycle, Outputs are in high impedance state during this period.
- (5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	-	30*	μA
		V _{DH} = 5.5 V	-	60	
t _{CDR}	Chip Deselect to Data Retention Mode	0	-	-	nS
t _R	Recovery Time	5	-	-	mS

*) 6 μA (max) Ta = 0° to 40°C

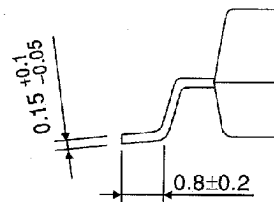
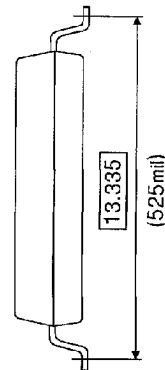
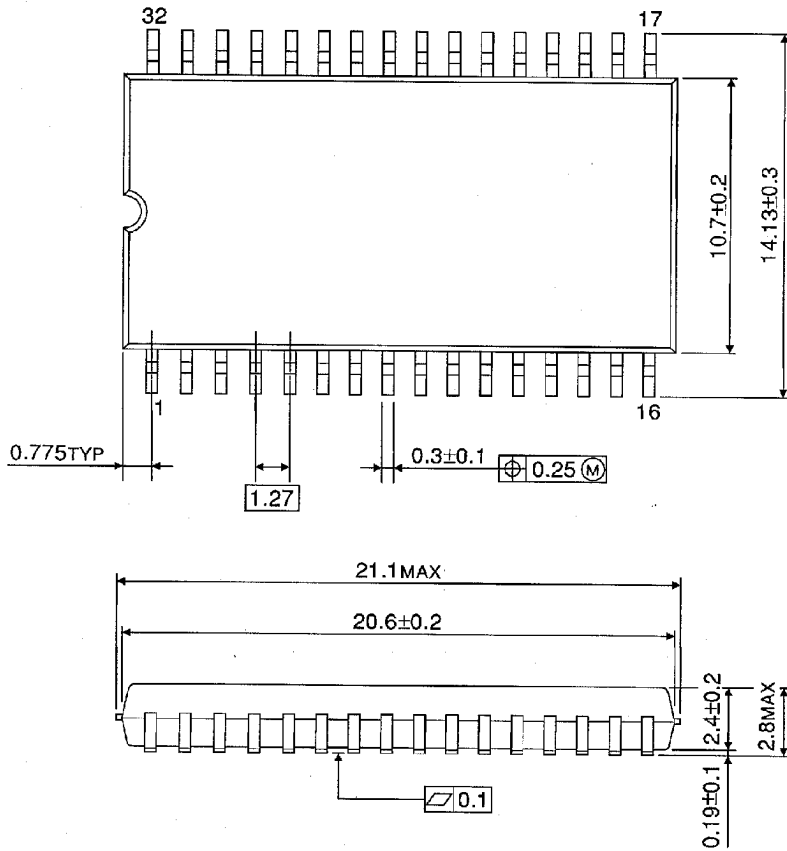
CE Controlled Data Retention Mode



Note: If the V_{IH} of CE is 2.2 V in operation, during the period that the V_{DD} voltage is going down from 4.5 to 2.4 V, I_{DDS1} current flows.

PACKAGE DIMENSIONS (SOP32-P-525)

Unit in mm

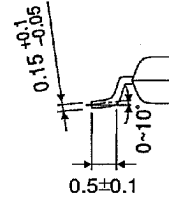
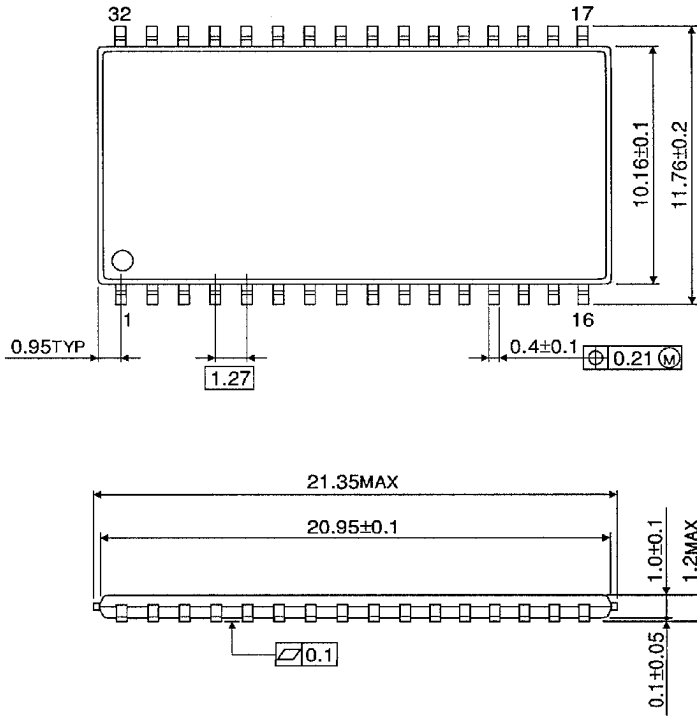


Weight: 1.14 g (typ)

TC554001FL-L-8
1996-09-02
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PACKAGE DIMENSIONS (TSOP32-P-400)

Unit in mm



Weight: 0.51 g (typ)

TC554001FL-L-9*
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