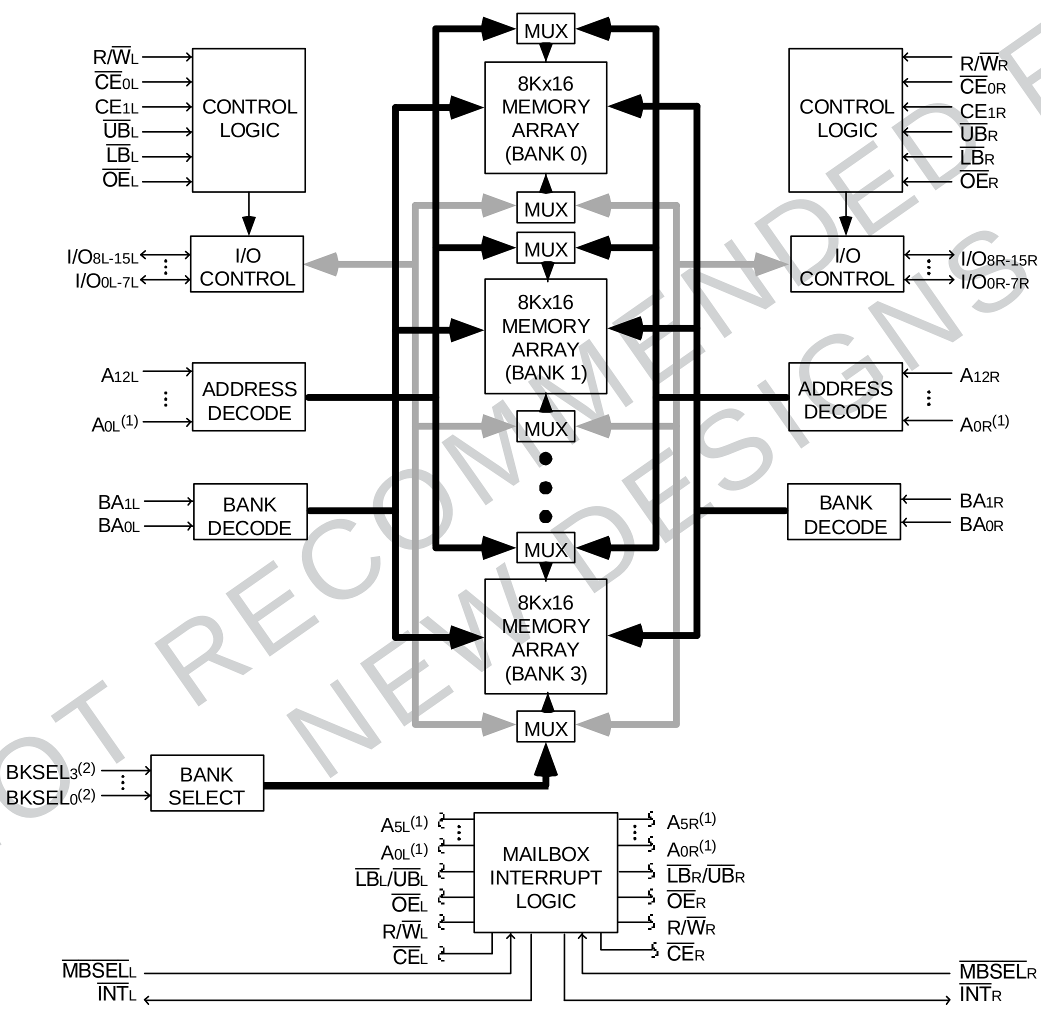
HIGH-SPEED 3.3V 32K x 16 BANK-SWITCHABLE DUAL-PORTED SRAM WITH EXTERNAL BANK SELECTS

IDT70V7278S/L

Features

- **32K x 16 Bank-Switchable Dual-Ported SRAM Architecture**
  - *Four independent 8K x 16 banks*
  - *512 kilobit of memory on chip*
- **Fast asynchronous address-to-data access time: 15ns**
- **User-controlled input pins included for bank selects**
- **Independent port controls with asynchronous address & data busses**
- **Four 16-bit mailboxes available to each port for inter-processor communications; interrupt option**
- **Interrupt flags with programmable masking**
- **Dual Chip Enables allow for depth expansion without external logic**
- **$\overline{UB}$ and $\overline{LB}$ are available for x8 or x16 bus matching**
- **LVTTL-compatible, single 3.3V (±5%) power supply**
- **Available in a 100-pin Thin Quad Flatpack**
- **Industrial temperature range (-40° to +85°C) is available for selected speeds**

Functional Block Diagram



NOTES:
1. The first six address pins for each port serve dual functions. When $\overline{MBSEL}$ = V_{IH}, the pins serve as memory address inputs. When $\overline{MBSEL}$ = V_{IL}, the pins serve as mailbox address inputs.
2. Each bank has an input pin assigned that allows the user to toggle the assignment of that bank between the two ports. Refer to Truth Table I for more details.

JUNE 2000

Description

The IDT70V7278 is a high-speed 32K x 16 (512K bit) Bank-Switchable Dual-Ported SRAM organized into four independent 8K x 16 banks. The device has two independent ports with separate controls, addresses, and I/O pins for each port, allowing each port to asynchronously access any 8K x 16 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via bank select pin inputs under the user's control. Mailboxes are provided to allow inter-processor communications. Interrupts are provided to indicate mailbox writes have occurred. An automatic power down feature controlled by the chip enables ($\overline{CE}_0$ and CE_1) permits the on-chip circuitry of each port to enter a very low standby power mode and allows fast depth expansion.

The IDT70V7278 offers a maximum address-to-data access time as fast as 15ns, and is packaged in a 100-pin Thin Quad Flatpack (TQFP).

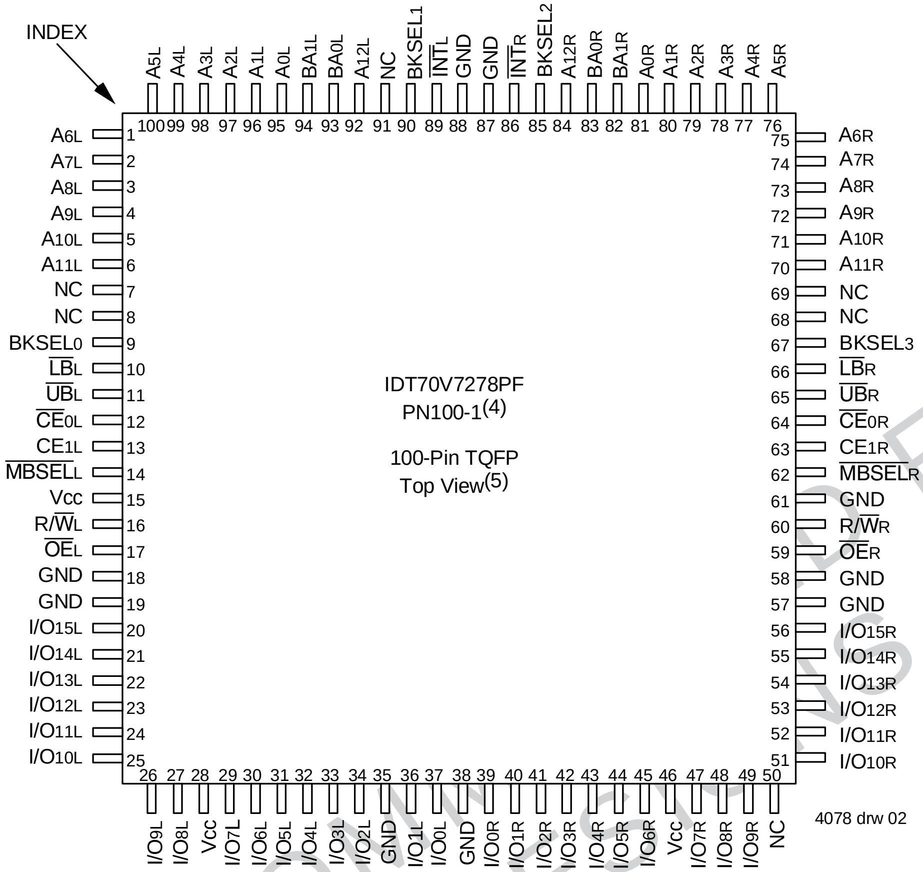
Functionality

The IDT70V7278 is a high-speed asynchronous 32K x 16 Bank-Switchable Dual-Ported SRAM, organized in four 8K x 16 banks. The two ports are permitted independent, simultaneous access into separate banks within the shared array. There are four user-controlled Bank Select input pins, and each of these pins is associated with a specific bank within the memory array. Access to a specific bank is gained by placing the associated Bank Select pin in the appropriate state: V_{IH} assigns the bank to the left port, and V_{IL} assigns the bank to the right port (See Truth Table IV). Once a bank is assigned to a particular port, the port has full access to read and write within that bank. Each port can be assigned as many banks within the array as needed, up to and including all four banks.

The IDT70V7278 provides mailboxes to allow inter-processor communications. Each port has four 16-bit mailbox registers available to which it can write and read and which the opposite port can read only. These mailboxes are external to the common SRAM array, and are accessed by setting $\overline{MBSEL} = V_{IL}$ while setting $\overline{CE} = V_{IH}$. Each mailbox has an associated interrupt: a port can generate an interrupt to the opposite port by writing to the upper byte of any one of its four 16-bit mailboxes. The interrupted port can clear the interrupt by reading the upper byte. This read will not alter the contents of the mailbox.

If desired, any source of interrupt can be independently masked via software. Two registers are provided to permit interpretation of interrupts: the Interrupt Cause Register and the Interrupt Status Register. The Interrupt Cause Register gives the user a snapshot of what has caused the interrupt to be generated - the specific mailbox written to. The information in this register provides post-mask signals: Interrupt sources that have been masked will not be updated. The Interrupt Status Register gives the user the status of all bits that could potentially cause an interrupt regardless of whether they have been masked. Truth Table V gives a detailed explanation of the use of these registers.

Pin Configurations(1,2,3)



NOTES:
1. All VCC pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

A_0 - A_{12}(1,6)	Address Inputs
BA_0 - BA_1(1)	Bank Address Inputs
$\overline{MBSEL}$(1)	Mailbox Access Control Gate
$\overline{BKSEL}_{0-3}$(2)	Bank Select Inputs
R/$\overline{W}$(1)	Read/Write Enable
$\overline{OE}$(1)	Output Enable
$\overline{CE}_0$, $\overline{CE}_1$(1)	Chip Enables
$\overline{UB}$, $\overline{LB}$(1)	I/O Byte Enables
I/O_0 - I/O_{15}(1)	Bidirectional Data Input/Output
$\overline{INT}$(1)	Interrupt Flag (Output)(3)
V_{CC}(4)	3.3VPower
GND(5)	Ground

4078 tbl 01

NOTES:
1. Duplicated per port.
2. Each bank has an input pin assigned that allows the user to toggle the assignment of that bank between the two ports. Refer to Truth Table IV for more details. When changing the bank assignment, accesses of the affected banks must be suspended. Accesses may continue uninterrupted in banks that are not being reallocated.
3. Generated upon mailbox access.
4. All Vcc pins must be connected to power supply.
5. All GND pins must be connected to ground supply.
6. The first six address pins (A_0-A_5) for each port serve dual functions. When MBSEL = V_{IH}, the pins serve as memory address inputs. When MBSEL = V_{IL}, the pins serve as mailbox address inputs (A_6-A_{12} ignored).

Truth Table I – Chip Enable[1,2,3,4]

$\overline{CE}$	$\overline{CE}_0$	CE_1	Mode
L	V_{IL}	V_{IH}	Port Selected (TTL Active)
	$\leq$ 0.2V	$\geq V_{CC}$ -0.2V	Port Selected (CMOS Active)
H	V_{IH}	X	Port Deselected (TTL Inactive)
	X	V_{IL}	Port Deselected (TTL Inactive)
	$\geq V_{CC}$ -0.2V	X	Port Deselected (CMOS Inactive)
	X	$\leq$0.2V	Port Deselected (CMOS Inactive)

4078 tbl 02

NOTES:
1. Chip Enable references are shown above with the actual $\overline{CE}_0$ and CE_1 levels, $\overline{CE}$ is a reference only.
2. Port "A" and "B" references are located where $\overline{CE}$ is used.
3. "H" = V_{IH} and "L" = V_{IL}.
4. $\overline{CE}$ and $\overline{MBSEL}$ cannot both be active at the same time.

Truth Table II – Non-Contention Read/Write Control

Inputs[1]						Outputs		Mode
$\overline{CE}$[2]	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{MBSEL}$	I/O_{8-15}	I/O_{0-7}	
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X[3]	X	X	H	H	X[3]	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	$DATA_{IN}$	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X[3]	X	H	X	X	X[3]	High-Z	High-Z	Outputs Disabled

4078 tbl 03

NOTES:
1. BA_{0L} - $BA_{1L} \neq BA_{0R}$ - BA_{1R}: cannot access same bank simultaneously from both ports.
2. Refer to Truth Table I.
3. $\overline{CE}$ and $\overline{MBSEL}$ cannot both be active at the same time.

Truth Table III – Mailbox Read/Write Control[1]

Inputs						Outputs		Mode
$\overline{CE}$[2]	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{MBSEL}$	I/O_{8-15}	I/O_{0-7}	
H	H	L	X[3]	X[3]	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data from Mailbox, ↓clears interrupt
H	H	L	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data from Mailbox, ↓clears interrupt
H	L	X	L[3]	L[3]	L	$DATA_{IN}$	$DATA_{IN}$	Write Data into Mailbox
L	X	X	X	X	L	—	—	Not Allowed

4078 tbl 04

NOTES:
1. There are four mailbox locations per port written to and read from all the I/O's (I/O_0-I/O_{15}). These four mailboxes are addressed by A_0-A_5. Refer to Truth Table V.
2. Refer to Truth Table I.
3. Each mailbox location contains a 16-bit word, controllable in bytes by setting input levels to $\overline{UB}$ and $\overline{LB}$ appropriately.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	50	mA

4078 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 5% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 5%.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 5%
Industrial	-40°C to +85°C	0V	3.3V ± 5%

4078 tbl 06

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.135	3.3	3.465	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.0	—	VCC +5%(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.8	V

4078 tbl 07

NOTES:
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 5%.

Capacitance(1)

(TA = +25°C, f = 1.0MHz) TQFP Package

Symbol	Parameter	Conditions(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT(3)	Output Capacitance	VOUT = 3dV	10	pF

4078 tbl 08

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.
3. COUT represents CI/O as well.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VCC = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	70V7278S		70V7278L		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current(1)	VCC = 3.465V, VIN = 0V to VCC	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, $\overline{MBSEL}$ = VIH, VOUT = 0V to VCC	—	10	—	5	µA
VOL	Output Low Voltage	IOL = +4mA	—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

4078 tbl 09

NOTE:
1. At Vcc ≤ 2.0V, input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,6) (V_{CC} = 3.3V ± 5%)

Symbol	Parameter	Test Condition	Version		70V7278X15 Com'l Only		70V7278X20 Com'l Only		70V7278X25 Com'l & Ind		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Disabled $\overline{MBSEL} = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	200 200	280 230	170 170	260 210	160 160	250 200	mA
			IND	S L	— —	— —	— —	— —	160 160	280 230	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $\overline{MBSEL}_R = \overline{MBSEL}_L = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	50 50	85 60	40 40	75 50	35 35	70 45	mA
			IND	S L	— —	— —	— —	— —	35 35	80 55	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"} = V_{IL}$ and $\overline{CE}_{"B"} = V_{IH}$(5) Active Port Outputs Disabled, $f=f_{MAX}$(3) $\overline{MBSEL}_R = \overline{MBSEL}_L = V_{IH}$	COM'L	S L	120 120	160 140	100 100	140 120	90 90	130 110	mA
			IND	S L	— —	— —	— —	— —	90 90	150 130	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0(4) $\overline{MBSEL}_R = \overline{MBSEL}_L \geq V_{CC} - 0.2V$	COM'L	S L	1.5 1.5	6 3	1.5 1.5	6 3	1.5 1.5	6 3	mA
			IND	S L	— —	— —	— —	— —	1.5 1.5	10 6	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq 0.2V$ and $\overline{CE}_{"B"} \geq V_{CC} - 0.2V$(5) $\overline{MBSEL}_R = \overline{MBSEL}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled $f = f_{MAX}$(3)	COM'L	S L	115 115	140 125	95 95	130 110	85 85	120 100	mA
			IND	S L	— —	— —	— —	— —	85 85	140 120	

4078 tbl 10

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Refer to Truth Table I.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

4078 tbl 11

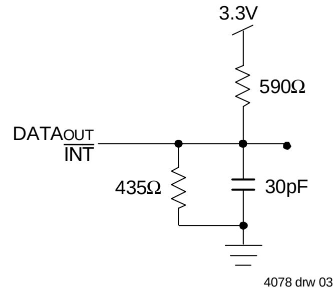


Figure 1. AC Output Test Load

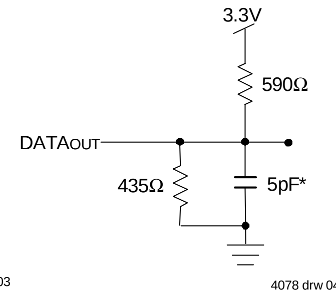


Figure 2. Output Test Load
(for tLZ, tHZ, tWZ, tOW)
*Including scope and jig.

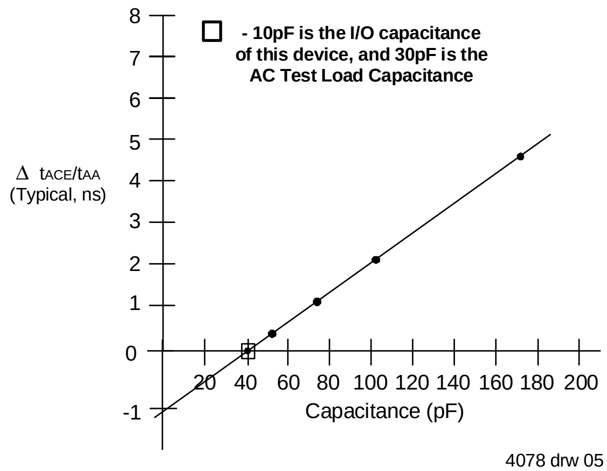


Figure 3. Lumped Capacitance Load Typical Derating Curve

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4]

Symbol	Parameter	70V7278X15 Com'l Only		70V7278X20 Com'l Only		70V7278X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time[3]	—	15	—	20	—	25	ns
t_{ABE}	Byte Enable Access Time[3]	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	9	—	10	—	11	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	8	—	9	—	10	ns
t_{PU}	Chip Enable to Power Up Time[2,5]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2,5]	—	15	—	20	—	25	ns
t_{MOP}	Mailbox Flag Update Pulse ($\overline{OE}$ or $\overline{MBSEL}$)	10	—	10	—	10	—	ns
t_{MAA}	Mailbox Address Access Time	—	15	—	20	—	25	ns

4078 tbl 12

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{MBSEL}$ = V_{IH}. To access mailbox, $\overline{CE}$= V_{IH} and $\overline{MBSEL}$ = V_{IL}.
4. 'X' in part numbers indicates power rating (S or L).
5. Refer to Truth Table I.

Assigning the Banks via the External Bank Selects

There are four bank select pins available on the IDT70V7278, and each of these pins is associated with a specific bank within the memory array. The pins are user-controlled inputs: access to a specific bank is assigned to a particular port by setting the input to the appropriate level. The process of assigning the banks is detailed in Truth Table IV. Once a bank is assigned to a port, the owning port has full access to read and write within that bank. The opposite port is unable to access that bank until the user reassigns the port. Access by a port to a bank which it does not control will have no effect if written, and if read unknown values on D_0-D_{15} will be returned. Each port can be assigned as many banks within the array as needed, up to and including all four banks.

The bank select pin inputs must be set at either V_{IH} or V_{IL} - these inputs are not tri-statable. When changing the bank assignments, accesses of the affected banks must be suspended. Accesses may continue uninterrupted in banks that are not being reallocated.

Truth Table IV – Memory Bank Assignment ($\overline{CE}$ = V_{IH})(2,3)

BKSEL0	BKSEL1	BKSEL2	BKSEL3	BANK AND DIRECTION(1)
H	X	X	X	BANK 0 LEFT
X	H	X	X	BANK 1 LEFT
X	X	H	X	BANK 2 LEFT
X	X	X	H	BANK 3 LEFT
L	X	X	X	BANK 0 RIGHT
X	L	X	X	BANK 1 RIGHT
X	X	L	X	BANK 2 RIGHT
X	X	X	L	BANK 3 RIGHT

4078 tbl 13

NOTES:
1. Bank 0 refers to the first 8Kx16 memory spaces, Bank 1 to the second 8Kx16 memory spaces, Bank 2 to the third 8Kx16 memory spaces, and Bank 3 to the fourth 8Kx16 memory spaces. 'LEFT' indicates the bank is assigned to the left port; 'RIGHT' indicates the bank is assigned to the right port. 0-4 banks may be assigned to either port.
2. The bank select pin inputs must be set at either V_{IH} or V_{IL} - these inputs are not tri-statable. When changing the bank assignments, accesses of the affected banks must be suspended. Accesses may continued uninterrupted in banks that are not being reallocated.
3. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = Don't Care.

Mailbox Interrupts and Interrupt Control Registers

If the user chooses the mailbox interrupt function, four mailbox locations are assigned to each port. These mailbox locations are external to the memory array. The mailboxes are accessed by taking $\overline{MBSEL}$ LOW while holding $\overline{CE}$ HIGH.

The mailboxes are 16 bits wide and controllable by byte: the message is user-defined since these are addressable SRAM locations. An interrupt is generated to the opposite port upon writing to the upper byte of any mailbox location. A port can read the message it has just written in order to verify it: this read will not alter the status of the interrupt sent to the opposite port. The interrupted port can clear the interrupt by reading the upper byte of the applicable mailbox. This read will not alter the contents of the mailbox. The use of mailboxes to generate interrupts to the opposite port and the reading of mailboxes to clear interrupts is detailed in Truth Table V.

If desired, any of the mailbox interrupts can be independently masked via software. Masking of the interrupt sources is done in the Mask Register. The masks are individual and independent: a port can mask any combination of interrupt sources with no effect on the other sources. Each port can modify only its own Mask Register. The use of this register is detailed in Truth Table V.

Two registers are provided to permit interpretation of interrupts: these are the Interrupt Cause Register and the Interrupt Status Register. The Interrupt Cause Register gives the user a snapshot of what has caused the interrupt to be generated - the specific mailbox written to by the opposite port. The information in this register provides post-mask signals: interrupt sources that have been masked will not be updated. The Interrupt Status Register gives the user the status of all bits that could potentially cause an interrupt regardless of whether they have been masked. The use of the Interrupt Cause Register and the Interrupt Status Register is detailed in Truth Table V.

Truth Table V – Mailbox Interrupts ($\overline{CE}$ = V_{IH})(8,9)

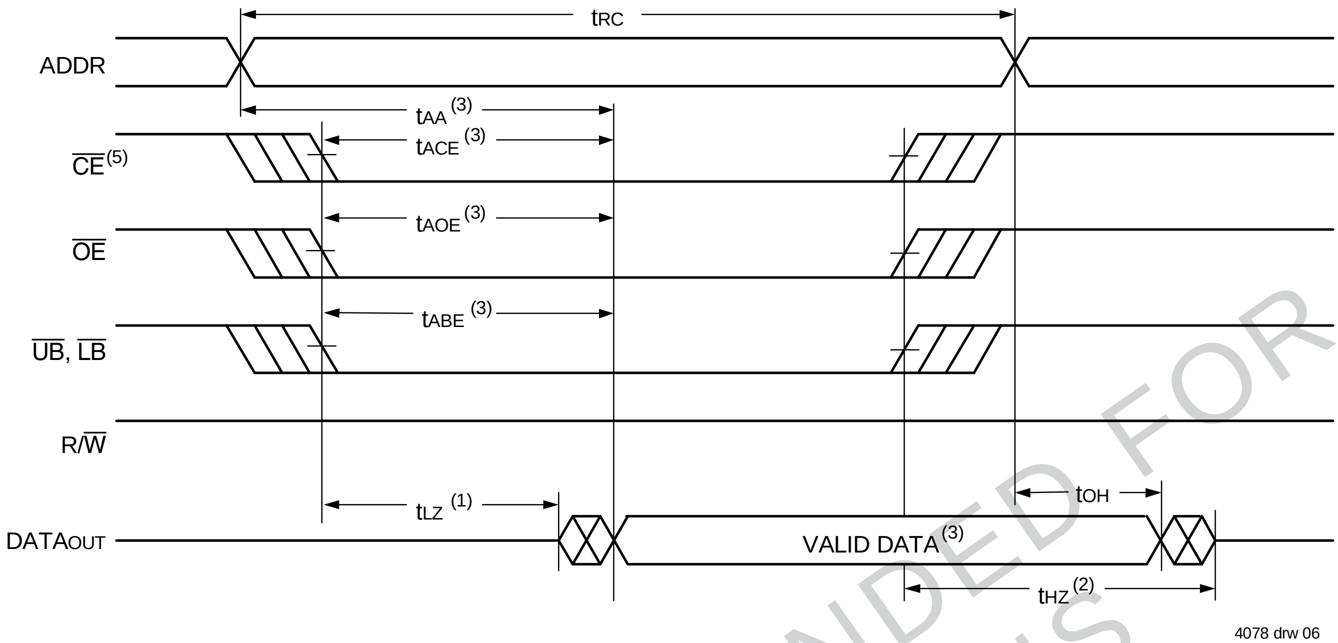
$\overline{MBSEL}$	R/$\overline{W}$	$\overline{UB}$	$\overline{LB}$	A5	A4	A3	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	DESCRIPTION
L	X	X	X	L	L	L	L	L	L	RESERVED (7)																RESERVED (7)
L	X	X	X	⋮	⋮	⋮	⋮	⋮	⋮	RESERVED (7)																RESERVED (7)
L	(1)	(1)	(1)	H	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 0 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 1 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 2 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 3 - SET INTERRUPT ON OPPOSITE PORT
↓	H	(2)	(2)	H	L	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 0 - CLEAR OPPOSITE PORT INTERRUPT
↓	H	(2)	(2)	H	L	L	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 1 - CLEAR OPPOSITE PORT INTERRUPT
↓	H	(2)	(2)	H	L	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 2 - CLEAR OPPOSITE PORT INTERRUPT
↓	H	(2)	(2)	H	L	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 3 - CLEAR OPPOSITE PORT INTERRUPT
L	(3)	(3)	(3)	H	L	H	L	L	L	(4)	(4)	(4)	(4)	(5)	(5)	(5)	(5)	(6)	(6)	(6)	(6)	X	X	X	X	MAILBOX INTERRUPT CONTROLS
L	X	X	X	⋮	⋮	⋮	⋮	⋮	⋮	RESERVED (7)																RESERVED (7)
L	X	X	X	H	H	H	H	H	H	RESERVED (7)																RESERVED (7)

4078 tbl 14

NOTES:

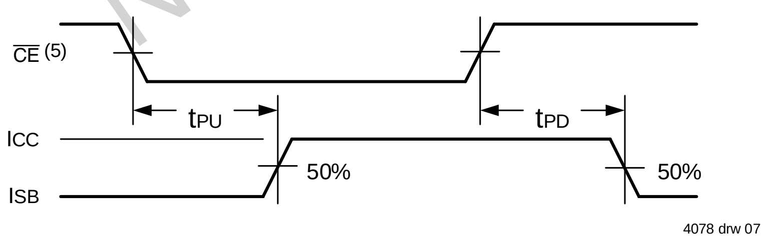
1. There are four independent mailbox locations available to each side, external to the standard memory array. The mailboxes can be written to in either 8-bit or 16-bit widths. The upper byte of each mailbox has an associated interrupt to the opposite port. The mailbox interrupts can be individually masked if desired, and the status of the interrupt determined by polling the Interrupt Status Register (see Note 6 for this table). A port can read its own mailboxes to verify the data written, without affecting the interrupt which is sent to the opposite port.
2. These registers allow a port to read the data written to a specific mailbox location by the opposite port. Reading the upper byte of the data in a particular mailbox clears the interrupt associated with that mailbox without modifying the data written. Once the address and R/$\overline{W}$ are stable, the actual clearing of the interrupt is triggered by the transition of $\overline{MBSEL}$ from V_{IH} to V_{IL}.
3. This register contains the Mask Register (bits D_0-D_3), the Interrupt Cause Register (bits D_4-D_7), and the Interrupt Status Register (bits D_8-D_{11}). The controls for R/$\overline{W}$, $\overline{UB}$, and $\overline{LB}$ are manipulated in accordance with the appropriate function. See Notes 4, 5, and 6 for this table. Bits D_{12}-D_{15} are "Don't Care".
4. This register, the Mask Register, allows the user to independently mask the various interrupt sources. Writing V_{IH} to the appropriate bit (D_0 = Mailbox 0, D_1 = Mailbox 1, D_2 = Mailbox 2, and D_3 = Mailbox 3) disables the interrupt, while writing V_{IL} enables the interrupt. All four bits in this register must be written at the same time. This register can be read at any time to verify the mask settings. The masks are individual and independent: any single interrupt source can be masked with no effect on the other sources. Each port can modify only its own mask settings.
5. This register, the Interrupt Cause Register, gives the user a snapshot of what has caused the interrupt to be generated. Reading V_{OL} for a specific bit (D_4 = Mailbox 0, D_5 = Mailbox 1, D_6 = Mailbox 2, and D_7 = Mailbox 3) indicates that the associated interrupt source has generated an interrupt. Acknowledging the interrupt clears the bit in this register (see Note 2 for this table). This register provides post-mask information: if the interrupt source has been masked, the associated bit in this register will not update.
6. This register, the Interrupt Status Register, gives the user the status of all interrupt sources that could potentially cause an interrupt regardless of whether they have been masked. Reading V_{OL} for a specific bit (D_8 = Mailbox 0, D_9 = Mailbox 1, D_{10} = Mailbox 2, and D_{11} = Mailbox 3) indicates that the associated interrupt source has generated an interrupt. Acknowledging the interrupt clears the associated bit in this register (see Note 2 for this table). This register provides pre-mask information: regardless of whether an interrupt source has been masked, the associated bit in this register will update.
7. Access to registers defined as "RESERVED" will have no effect, if written, and if read unknown values on D_0-D_{15} will be returned.
8. These registers are not guaranteed to initialize in any known state. At power-up, the initialization sequence should include the set-up of these registers.
9. 'L' = V_{IL} or V_{OL}, 'H' = V_{IH} or V_{OH}, 'X' = Don't Care.

Waveform of Read Cycles(4)



NOTES:
1. Timing depends on which signal is asserted last, CE, OE, LB, or UB.
2. Timing depends on which signal is de-asserted first CE, OE, LB, or UB.
3. Start of valid data depends on which timing becomes effective last: t_{AOE}, t_{ACE}, t_{AA}, or t_{ABE}.
4. MBSEL = V_{IH}.
5. Refer to Truth Table I.

Timing of Power-Up Power-Down



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(5)

Symbol	Parameter	70V7278X15 Com'l Only		70V7278X20 Com'l Only		70V7278X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{BS}	Bank Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	8	—	9	—	10	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	8	—	9	—	10	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	3	—	3	—	3	—	ns
t_{MWRD}	Mailbox Write to Read Time	5	—	5	—	5	—	ns

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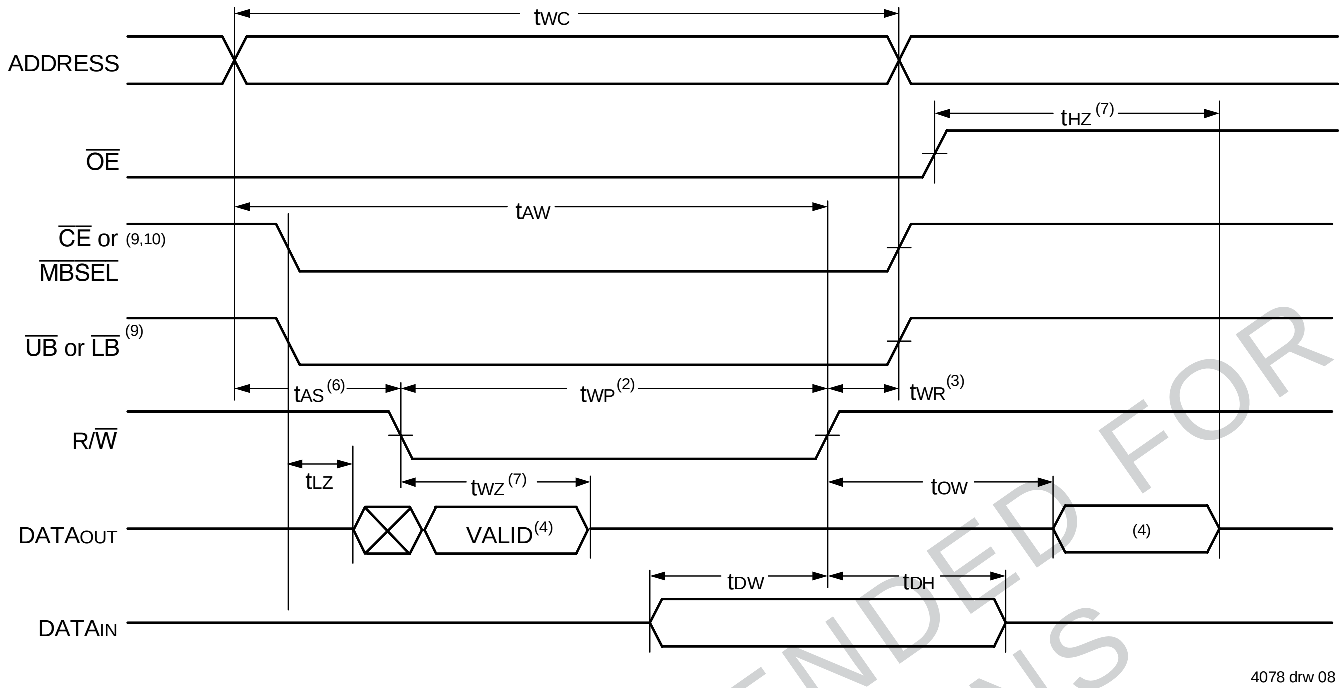
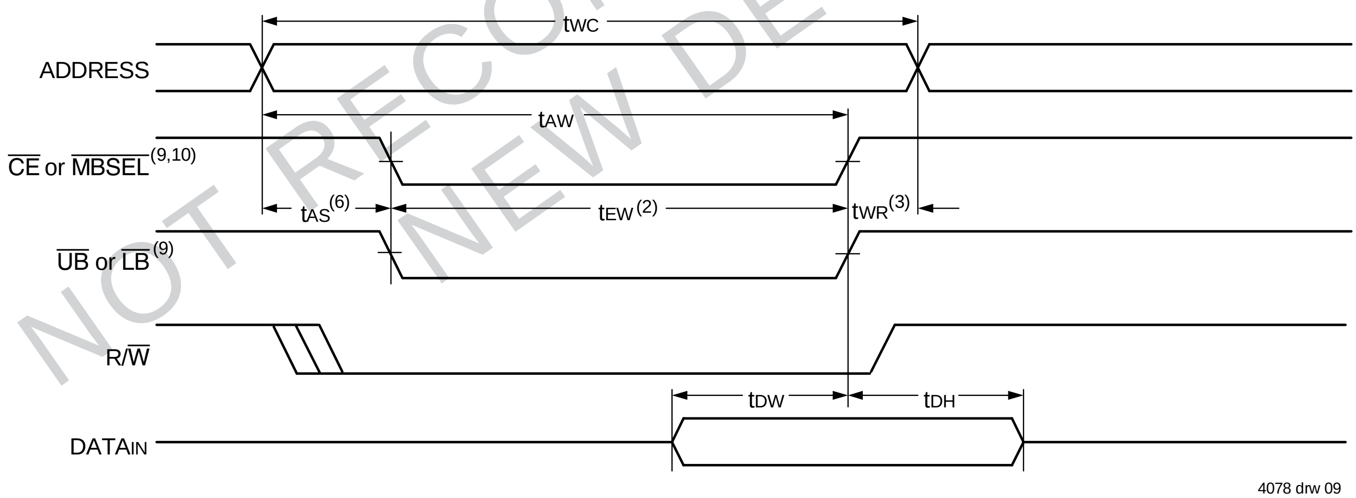
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{MBSEL}$ = V_{IH}. To access mailbox, $\overline{CE}$ = V_{IH} and $\overline{MBSEL}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time. Refer to Truth Tables I and III.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



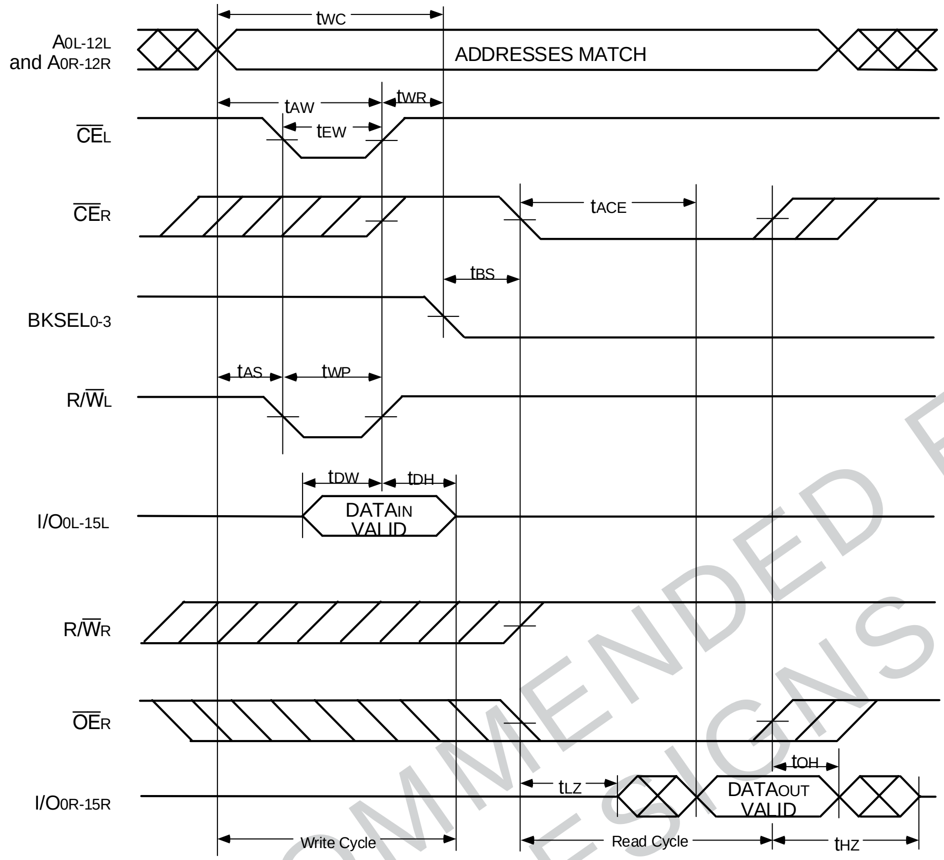
Timing Waveform of Write Cycle No. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled Timing(1,5)



NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{MBSEL}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{MBSEL}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{MBSEL}$ = V_{IH}. To access mailboxes, $\overline{CE}$ = V_{IH} and $\overline{MBSEL}$ = V_{IL}. t_{EW} must be met for either condition.
10. Refer to Truth Table I.

Timing Waveform of Left Port Write to Right Port Read of Same Data(1,2,3)



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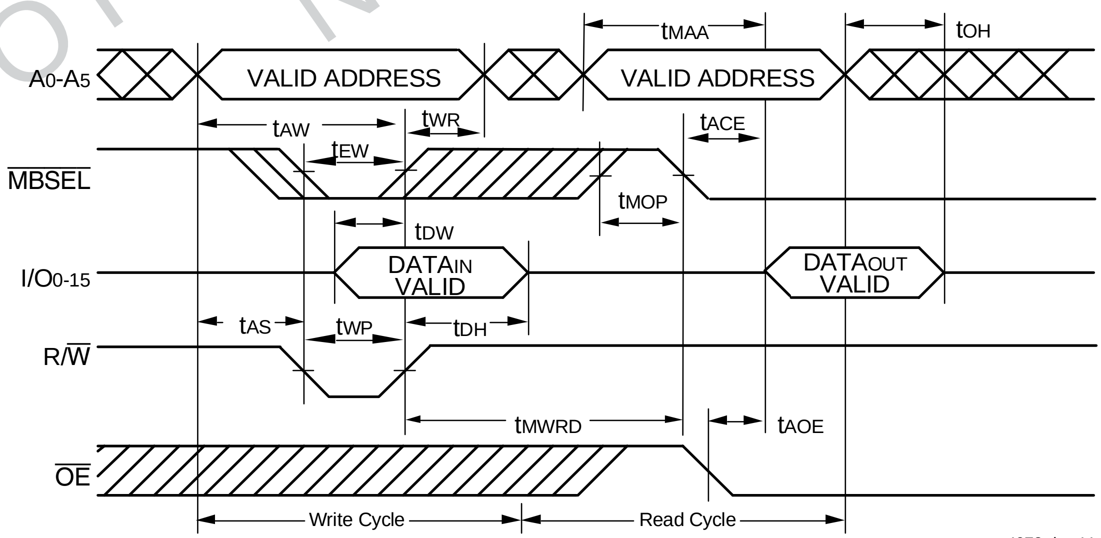
NOTES:
1. UB and LB are controlled as necessary to enable the desired byte accesses.
2. Timing for Right Port Write to Left Port Read is identical.
3. Refer to Truth Table I and IV.

Timing Waveform of Mailbox Read after Write Timing, Either Side(1,2)



4078 drw 11

NOTES:
1. CE = VIH for the duration of the above timing (both write and read cycle), refer to Truth Table I.
2. UB and LB are controlled as necessary to enable the desired byte accesses.

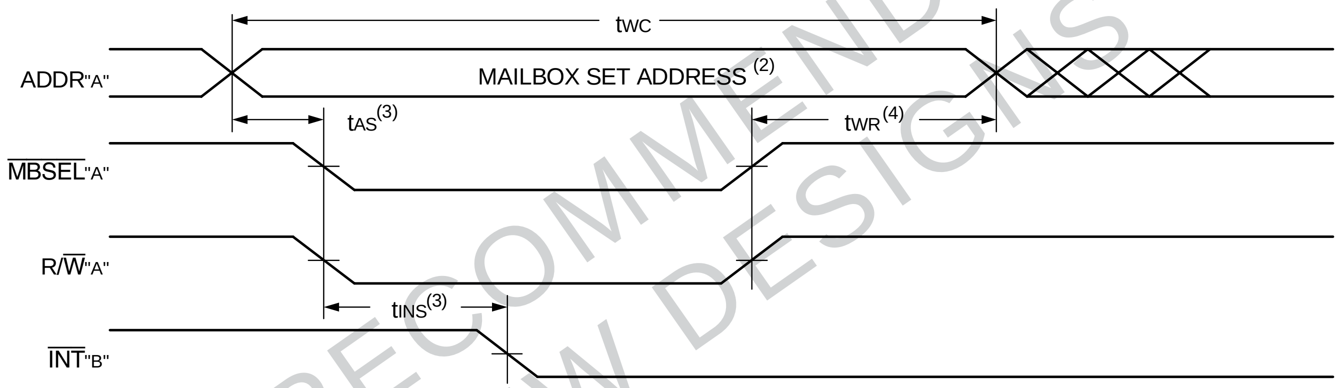
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1]

Symbol	Parameter	70V7278X15 Com'l Only		70V7278X20 Com'l Only		70V7278X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	15	—	20	—	25	ns
t_{INR}	Interrupt Reset Time	—	15	—	20	—	25	ns

4078 tbl 16

NOTES:
1. 'X' in part numbers indicates power rating (S or L).

Waveform of Interrupt Timing[1,5]



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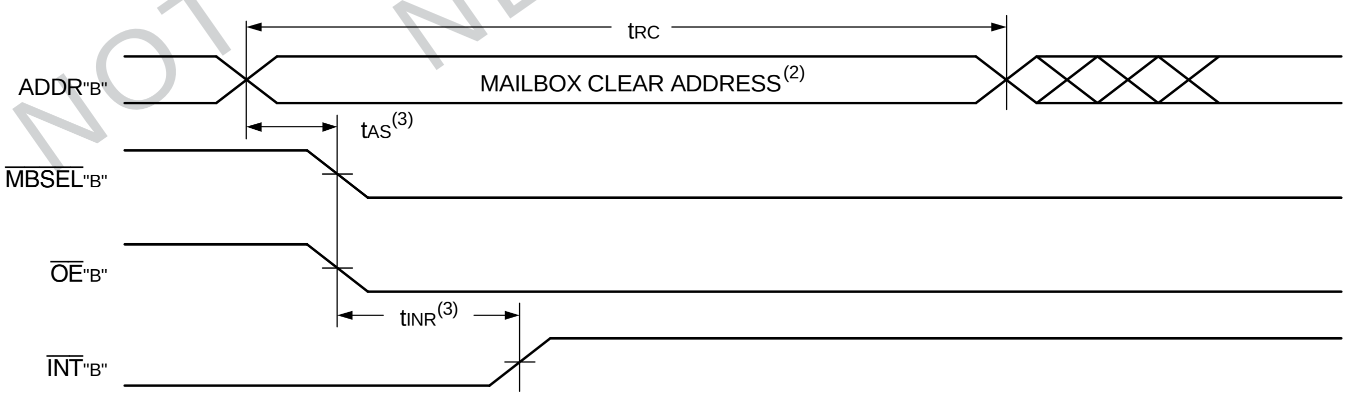

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NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt Truth Table V.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.
5. Refer to Truth Table I.

Depth and Width Expansion

The IDT70V7278 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V7278 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

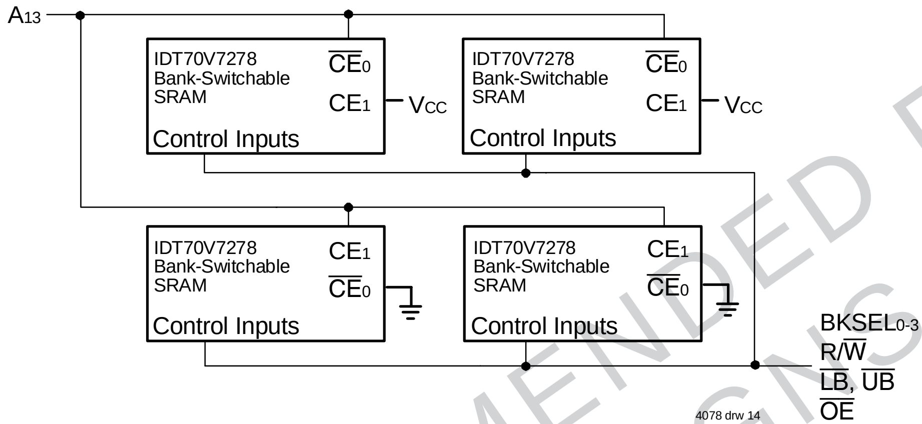

Figure 4. Depth and Width Expansion with IDT70V7278

Ordering Information

IDT XXXXX A 999 A A

Device Type	Power	Speed	Package	Process/ Temperature Range
XXXXX	A	999	A	A

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- I — Industrial (-40°C to +85°C)

Package:
- PF — 100-pin TQFP (PN100-1)

Speed (Speed in nanoseconds):
- 15 — Commercial Only
- 20 — Commercial & Industrial
- 25 — Commercial & Industrial

Power:
- S — Standard Power
- L — Low Power

Device Type:
- 70V7278 — 512Kbit (4 x 8K x 16) 3.3V Bank-Switchable Dual-Ported SRAM with External Bank Selects

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Datasheet Document History

3/5/99:	Initiated datasheet document history	
	Converted to new format	
	Cosmetic typographical corrections	
	Page 3 Added additional notes to pin configurations	
	Added 15ns speed grade	
6/10/99:	Changed drawing format	
9/1/99:	Removed Preliminary	
3/10/00:	Added Industrial Temperature Ranges and removed corresponding notes	
	Replaced IDT logo	
	Page 1 Added industrial temperature note	
	Changed ±200mV to 0mV in notes	
6/8/00:	Page 5	Increated storage temperature parameter
		Clarified T_A Parameter
	Page 6	DC Electrical parameters–changed wording from "open" to "disabled"

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