100 BASE-TX/FX REPEATER CONTROLLER

1.0 FEATURES

- IEEE 802.3u D5 repeater and management compatible
- Support 7 TX/FX ports and 1 universal port (TX or MII port selectable)
- Support 8-scale utilization and collision rate LED display
- Asynchronous Expansion port clock supported for easily stackable application
- Separate jabber and partition state machines for each port
- On-chip elasticity buffer for PHY signal re-timing to the MX98745 clock source
- Contents of internal register loaded from EEPROM
- PCS/MAC type MII interface selectable
- CMOS device features high integration and low power with a signle +5V supply

2.0 GENERAL DESCRIPTION

The MX98745, Second generation 100 Mb/s TX/FX Hub Controller (XRC II), is designed specifically to meet the needs of today's high speed Fast Ethernet networking systems. The MX98745 is fully IEEE 802.3u D5 clause 27 repeater compatible.

Difference from MX98741, which provides 8 dedicated TX/FX ports and 3 MII ports, MX98745 support 7 dedicated TX/FX ports and one programmble TX/FX/MII port. Whenever MII port is programmed, MX98745 also supports the flexibility to make user can easily select PCS or MAC type MII for system application. With this programmable MII interface, user can easily connect MX98745 to MX98742 (Bridge), or T4 transceiver. Or user can use this programmable MII interface to connect to either MAC or PCS type data transceiver.

All contents of internal registers are loaded from EEPROM in MX98745. If system application prefers default setting instead of using contents from EEPROM, EEPROM operation can be disabled by setting EECONF to low. This feature faciliates system modulization application.

8 scale of utilization LED is also provided by MX98745. They are 1%, 3%, 5%, 10%, 20%, 40%, 60% and 80+%. The defination for utiliztion is Mbs Received/100 Mb within one second sampling period. Meanwhile, RX/LINK, Partition, Isolation and Collision status are also provided through LED display.

A great improvement in MX98745 (compared to MX98741) is that it also provides "synchronous expansion port data transfer mode" to make stackable design more easier.

3.0 BLOCK DIAGRAMS

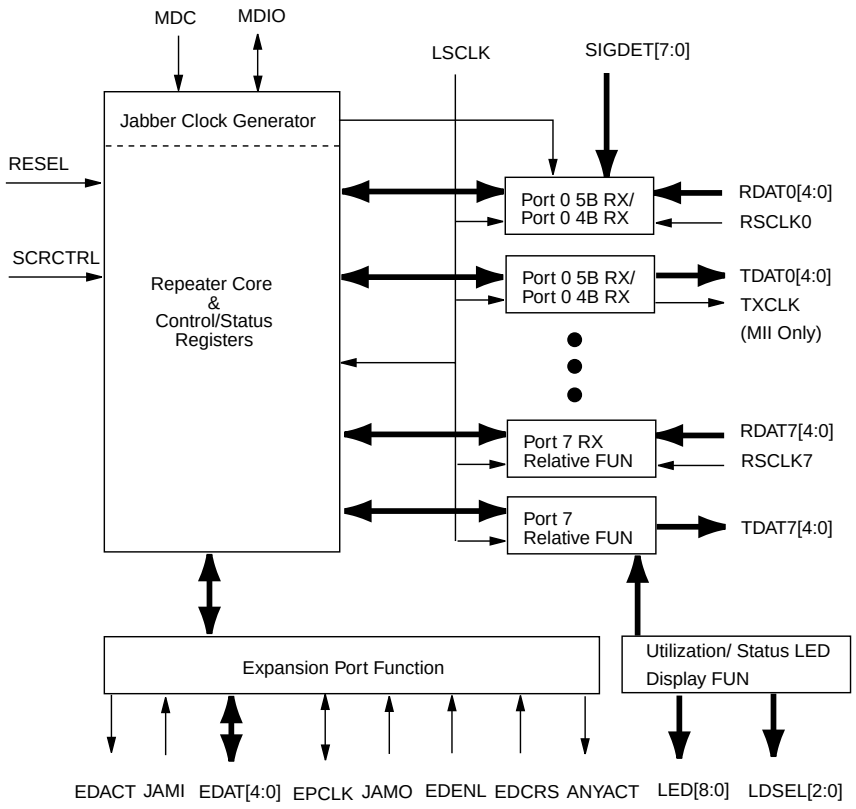


Figure 3-1 Block Diagram forMX98745

4.0 PIN CONFIGURATION

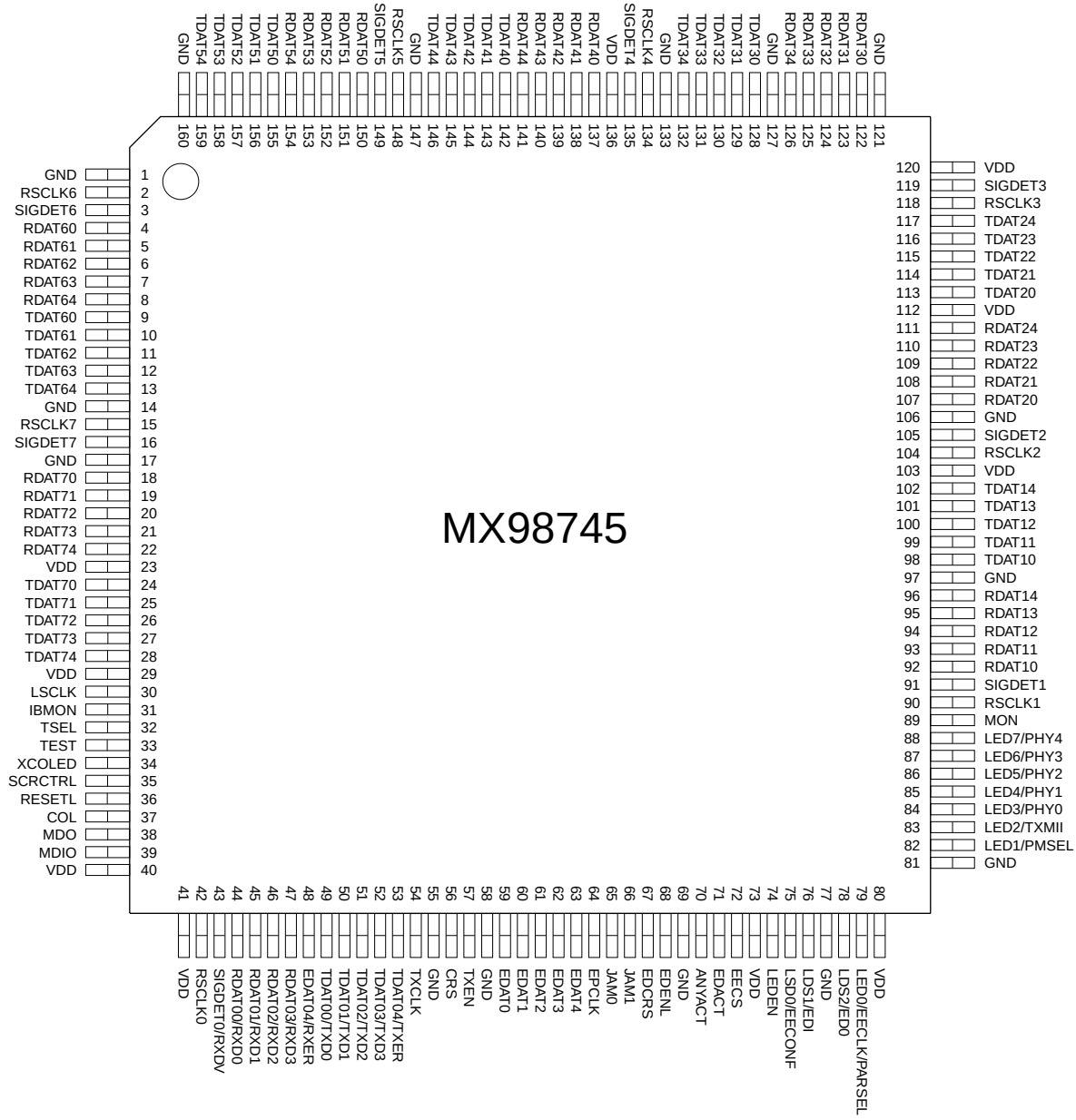


Figure 4-1 Pin Configuration for XRCII

5.0 PIN DESCRIPTION

A. MX Data Transceiver (Am78965/Am78966 or MC68836), 98 pins

PAD #	Name	I/O	Description
24-28 9-13 155-159 142-146 128-132 113-117 98-102	TDAT[7:1][0:4]	O, TTL	Transmit Data. These five outputs are 5B encoded transmit data sym bols, driven at the rising edge of LSCLK. TDAT4 is the Most Significant Bit.
30	LSCLK	I, TTL	Local Synchrnous Clock. This pin supplies the frequency reference to the MX98745 within same HUB. It should be driven by a crystal-controlled 25M clock source.
18-22 4-8 150-154 137-141 122-126 107-111 92-96	RDAT[7:1][0:4]	I, TTL	Receive Data. These 5 bit parallel data symbol from transceiver are latched by the rising edge of RSCLK of each port. RDAT4 is the Most Significant Bit.
15,2 148,134 118,104 90,42	RSCLK[7:0]	I, TTL	Recovered Symbol Clock. This is a 25 MHz clock, which is derived from the clock synchronization PLL circuit.
16,3, 149,135, 119,105, 91	SIGDET[7:1]	I, TTL	Signal Detect. This signal indicates that the received signal is above the detection threshold and will be used for the link test state machine.
31	Monitor	I, TTL	Monitor Mode. Internal Pulldown. When this pin is set to one, LED display pins LED[9:0] will be changed to monitor mode.

Table 5-1 Pin Description for XRCII

B. Expansion Port, 12 pins

PAD #	Name	I/O	Description
65	JAMO	O, CMOS	Forced Jam Out. Active High. The OR'd forced jam signals controlled by Carrier Integrity Monitor of each port. If collision occurs inside the XRC II (exclude JAMI), this pin is also asserted.
66	JAMI	I, TTL	Forced Jam Input. Active High. Asserted by external arbitor, and XRCII will generate JAM patterns to all its ports whenever this signal is validate more than 40 ns. This signal is filtered by LSCLK for 40ns internally.
68	EDENL	I, Sche	Enable Expansion Data. Active Low. Asserted by an external arbitor. XRC II will not drive data onto EDAT until this pin is asserted. Assertion time less than 40ns will not be recognized by XRC II.
63-59	EDAT[4:0]	I/O, TTL	Expansion Data. Bidirectional 5 bit-wide data. By default, EDAT is an input. An external arbitor coordinates multiple devices on EDAT.
64	EPCLK	I/O, TTL	Expansion port Data Clock. This clock will be outputed by XRCII along with the EDAT[4:0]. Another module of XRCII should use this signal as expansion port data input clock.
70	ANYACT	O, CMOS	Any Activity. Active High. When XRCII tries to release data onto EDAT, this pin will be asserted by XRC II.
67	EDCRS	I, Sche	Expansion Data Carrier Sense. When this pin is asserted, XRC II will recognize that there is activity on expansion port data bus EDAT and perform corresponding activity within XRCII itself.
71	EDACT	O, CMOS	Expansion Data Activity. When XRCII detects that EDENL is asserted by external arbitor, it will assert EDACT high. System application can use this signal to control the data bus flow of EDAT.

Table 5-1 Pin Description for XRC II (Continued)

C. Universal Port (UP), 14 pins

PAD #	Name	I/O	Description
43	SIGDET0/ RXDV	I, TTL	Signal Detect/Receive Data Valid. When TXMII (pin 84) is detected high during power on reset, This pin works as Signal detect in 5B data mode. When TXMII is low, this pin is output and works as RXDV in MII mode. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter
44-47	RDAT0[0:3]/ RXD[0:3]	I, TTL	Receive Data[3:0]. No matter TXMII's value is, these four pins work as the receive data both in TX mode and MII mode. Receive data is synchronous to RSCLK0's rising edge.
48	RDAT04/ RXER	I, TTL	Receive Data Bit 4/Receive Data Error. When TXMII is detected as 1, this pin works as the MSB of RDAT0[4:0]. When MII mode is selected, this pin is RXER and synchronous to RSCLK0's rising edge.
56	CRS	I/O, TTL	Carrier Sense. In PCS Mode, synchronous to TXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. In MAC mode (PMSEL is low), this pin is input.
57	TXEN	O, CMOS	Transmit Enable. This pin is output and synchronous to the TXCLK's rising edge whenever valid data is presented on TXD[3:0]
49-52	TDAT[0:3]/ TXD[0:3]	O, CMOS	Transmit Data. No matter TXMII's value is, these four pins work as the transmit data both in TX mode and MII mode. In TX mode, TDAT is synchronous to LSCLK rising edge. In MII mode, TXD[0:3] is synchronous to TXCLK rising edge.
53	TDAT04/ TXER	O, CMOS	Transmit Data Bit 4/Transmit ERROR. When TXMII is set to one, this pin work as the MSB of TDAT of port 0. When TXMII is low, This pin acts as TXEN and is synchronous to the TXCLK's rising edge. When TXER is asserted for one or more than one TXCLK period while TXEN is also asserted, one or more"HALT" symbols will present at TXD[3:0].
37	COL	I/O, CMOS	Collision. This signal is asserted if both the receiving media and TXEN are active. When PCS type MII is selected, this pin is output from XRCII and indicates that there is collision within the XRCII. When PMSEL is 0, COL is input to XRCII and indicates that there is collision on the receiving port.
54	TXCLK	I/O, CMOS	Transmit Clock. 25M Hz clock. TXD[3:0], TXEN, TXER are synchronous to this clock's rising edge. In PCS type MII (PMSEL is 1), CRS and COL are also synchronous to this clock's rising edge.

Table 5-1 Pin Description for XRCII (Continued)

D. Management, 2 pins

PAD #	Name	I/O	Description
38	MDC	I, TTL	Management Data Clock. The timing reference for MDIO. The minumum high and low times are 200 ns each.
39	MDIO	I/O, TTL	Management Data Input/Output. A bi-directional signal. The selection of input/output direction is based on IEEE802.3u management functions (Section 22.2.4).

E. Test/Miscellaneous, 5 pins

PAD #	Name	I/O	Description
33	TEST	I	Test. Industrial test pin. Set to 0 for normal operation. When programmed to logic 1, XRC II is in test mode.
32	TSEL	I	Test Select. Used by industrial test. Internal Pulldown. Set to 0 for normal operation.
34	XCOLED	O, LED	Collision LED. Active low. When there is collision within the XRC II, XCOLED will be on for 80ms and off for 20ms.
35	SCRCTRL	I, TTL	Scrambler Control. Active High. When this pin is set to 0. All TX port will be set to descramble mode, i.e. contents of register #17 will be disabled. When this pin is set to 1. Each port's scrambler/descrambler is controller by corre sponding bit in register #17. Internally pullup.
36	RESETL	I, Sche	Reset. Active Low. Will be filtered by LSCLK within the MX98745.
31	IBMON	I, TTL	Internal Bus Monitor. In house debugging usage. Internally pull down.

Table 5-1 Pin Description for XRC II (Continued)

F. LED Display/EEPROM Interface, 14 pins

PAD #	Name	I/O	Description
74	LEDEN	O,	Led Output Enable. When LEDEN is asserted high, it means that varuous internal CMOS status is shown on LED[7:0] according to the value on LDS[2:0]
78, 76, 75	LDS2/EDO, LDS1/EDI, LDS0/EECONF	I/O, TTL	LED Output Select. LDS0 is internally pulldown and value on LDS0 will be latched internally by MX98745 at the rising edge of RESETL as the value of EECONF. Value on LDS1 will act as EEPROM Data Input signal during EEPROM loading operation (after power on reset and EECONF is set to 1) and LDS2 will be data output from EEPROM. When EECONF is low, EEPROM operation will be disabled. After power on reset, LDS[2:0] work as the select pins of LED[7:0] output. The following are corresponding definition LDS2 LDS1 LDS0 0 0 1 Link/Receive 0 1 0 Isolation 0 1 1 Partition 1 0 0 Utilization 1 0 1 Collision Rate
79	LEDO/, EECK/, PARSEL	I/O TTL	LED 0/EEPROM Clock/Partition Select. Value on this pin will be latched by MX98745 at the rising edge of RESETL as the value of Partition Select (PARSEL). When EECONF is set to 1, this pin will work as EEPROM clock pin and output by MX98745 after power on reset. When EEPROM operation is enabled, internal repeater function will be disabled until contents in EEPROM is loaded into MX98745. After EEPROM operation is completed, this pin will display port 0's Receivee/Link, Partition, Isolation status and indicates 10% Network utilization and 3% collision rate according to the value of LDS[2:0].
82	LED1/PMSEL	I/O, TTL	LED 1/PCS & MAC type MII Select. When Power on reset, value on this pin will be latched at the rising edge of RESETL and be the value of PMSEL which can program the universal port (port 0) to PCS or MAC type MII interface. In normal operation (after power on reset), this pin will display port 1's Receivee/Link, Partition, Isolation status and indicates 20% Network utilization and 6% collision rate according to the value on LDS[2:0]

Table 5-1 Pin Description for XRC II (Continued)

F. LED Display (Continued)

PAD #	Name	I/O	Description
83	LED2/ TXMII	I/O, TTL	LED 2/Port0 TX/MII mode Select. When Power on reset, value on this pin will be latched at the rising edge of RESETL and be the value of TXMII which can program the universal port (port 0) to TX mode (5B interface) or MII mode (4B) interface. When TXMII is set to 1, Port 0 of XRC II will be programmed to TX mode and PMSEL will be disabled. In normal operation (after power on reset), this pin will display port 2's Receivee/Link, Partition, Isolation status and indicates 30% Network utilization and 9% collision rate according to the value on LDS[2:0]
84	LED3/ PHY0	I/O, TTL	LED 3/Physical Address 0. Value on LED3 will be latched at the rising edge of RESET as the setting of Device physical address 0. If EECONF is set to 1, PHY0 will be overwritten by the contents of EEPROM. After EEPROM operation is completed (in case EECONF is set to 1), this pin will display port 3's Receivee/Link, Partition, Isolation status and indicates 10% Network utilization and 8% collision rate according to the value on LDS[2:0]
85	LED4/ PHY1	I/O, TTL	LED 4/Physical Address 1. Value on LED4 will be latched at the rising edge of RESETL as the physical address 1 of MX98745. If EECONF is set, Physical address will be overwritten by the value from EEPROM. After EEPROM operation is completed, this pin will display port 4's Receivee/ Link, Partition, Isolation status and indicates 20% Network utilization and 10% collision rate according to the value on LDS[2:0].
86	LED5/ PHY2	I/O, TTL	LED 5/Physical Address 2. Value on LED5 will be latched at the rising edge of RESETL as the physical address 2 of MX98745. If EECONF is set, Physical address will be overwritten by the value from EEPROM. After EEPROM operation is completed, this pin will display port 5's Receivee/ Link, Partition, Isolation status and indicates 40% Network utilization and 13% collision rate according to the value on LDS[2:0].
87	LED6/ PHY3	I/O, TTL	LED 6/Physical Address 3. Value on LED6 will be latched at the rising edge of RESETL as the physical address 3 of MX98745. If EECONF is set, Physical address will be overwritten by the value from EEPROM. After EEPROM operation is completed, this pin will display port 6's Receivee/ Link, Partition, Isolation status and indicates 60% Network utilization and 15% collision rate according to the value on LDS[2:0].

Table 5-1 Pin Description for XRC II (Continued)

F. LED Display (Continued)

PAD #	Name	I/O	Description
88	LED7/ PHY4	I/O, TTL	LED 7/Physical Address 4. Value on LED7 will be latched at the rising edge of RESETL as the physical address 4 of MX98745. If EECONF is set, Physical address will be overwritten by the value from EEPROM. After EEPROM operation is completed, this pin will display port 7's Receivee/ Link, Partition, Isolation status and indicates 80+% Network utilization and 20+% collision rate according to the value on LDS[2:0].
72	EECS	O, CMOS	EEPROM Chip Select. Output by MX98745 when EECONF is set and EEPROM operation is activated by MX98745.
89	MON	I/O, TTL	Monitor. Value on this pin will be latched at the rising edge of RESETL. When programmed to high, internal state machines's states will be outputed to this pin serially for debugging usage. For normal operation, left unconnected.

G. Power/Ground Pins

PAD #	Name	I/O	Description
1,14, 17,55, 58,69, 77,81, 97,106, 121,127, 133,147, 160	GND		Ground.
23,29, 41,73, 80,103, 112,120, 136,	VDD		5V Power Supply.

Table 5-1 Pin Description for XRC II (Continued)

6.0 FUNCTIONAL AND OPERATION DESCRIPTION

6.1 All TX MODE SELECTED

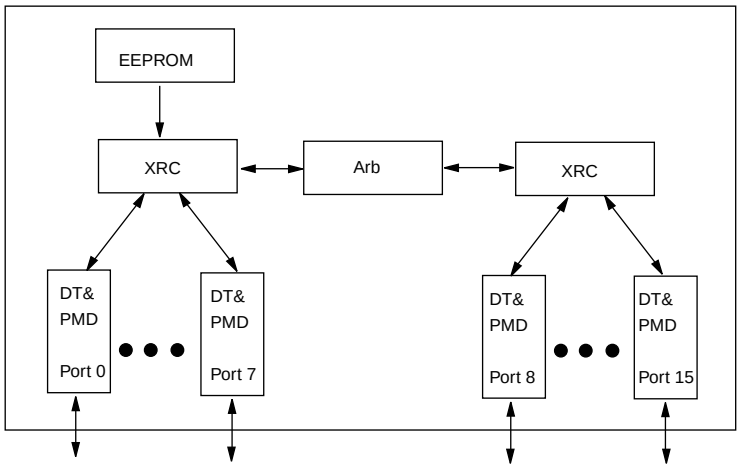


Figure 6-1 Pure TX Mode operation for XRC II

6.2 TX AND MII MIXED MODE

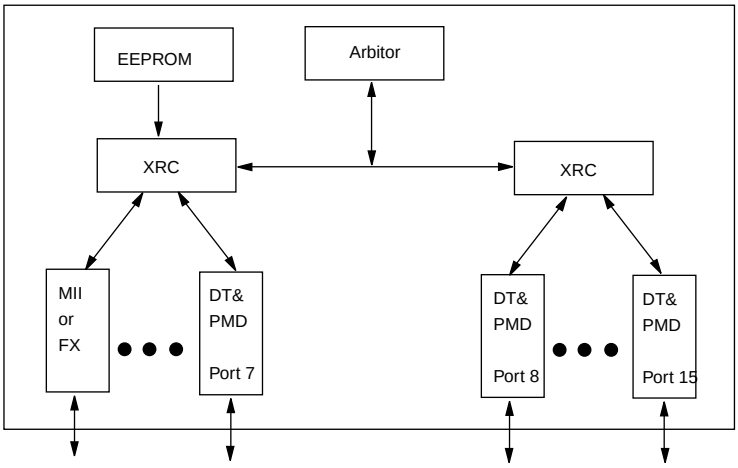


Figure 6-2 TX/MII Mixed Mode operation for XRC II

6.3 INTERNAL REGISTERS

All the registers can be accessed through MII's MDC and MDIO. Although XRC II connects to multiple 100-TX PHY's, they are all identical. Each XRC has only one PHY address as defined by PHY[4:0] pins (which will be latched by the rising edge of RESETL, and will be overwritten by the contents of EEPROM whenever EECONF is set to 1). If multiple XRC's are on the same MDIO bus, each of them should have different PHY address. Other non-XRC PHY devices (e.g. T4) are also allowed to be managed with the same management interface as long as PHY address of each device is distinct.

Register 0 and 1 are Command and Status registers which specified in [1]. Additional registers provided by MX98745 is located from address 16 to 31 (decimal value). Port Control Registers are located from address #16 to address #20. These control registers include port reset control register (#16), Port Scremabler control register (#17), Port Enable Control Register (#18), Isolation Disable Control Register (#19) and Partition Disable Control Register (#20).

Port Status Registers are located from address #25 to address #29. These registers include Link Status Register (#25), Partition Status Register (#26), Elastic Buffer Status Register (#27), Jabber Status Register (#28) and Isolation Status Register (#29).

Register #31 is Configuration Register. Value latched at the rising edge of RESETL will be stored in this register. Value on this register will be overwritten by contents of EEPROM in case EECONF is set to 1 except PMSEL and TXMII which will be affected only by hardwire setting.

A. Command Register (register #0) (R/W)

Bit(s)	Name	Description	R/W
0.15	Reset	1 : PHY reset. A 240ns reset pulse will be generated to reset XRC internal logic. 0 : normal operation.	R/W SC
0.14	Loop Back	1 : enable loopback mode. 0 : disable loopback mode. The default setting is 0.	R/W
0.13	Speed Selection	Forced to 1 and indicate 100 Mb/s. Write 0 to this bit has no effect.	R
0.12	Auto-Negotiation Enable	Forced to 0 and indicate that Auto-Negotiation process is disable. Write 1 to this bit has no effect.	R R/W
0.11	Power Down	1 : power down. COCLK and TXCLK for each port will be disabled. Clock for Management Block will keep running. During Power down, all state machines will be reset to its default state. 0 : normal operation.	R/W
0.10	Isolate	1 : electrically Isolate PHY from MII 0 : normal operation	R/W

Bit(s)	Name	Description	R/W
0.9	Restart Auto-Negotiation	Forced to 0 and indicate that Auto-Negotiation process is disable. Write 1 to this bit has no effect.	R
0.8	Duplex Mode	Forced to 0 and indicate that only Half Duplex is available. Write 1 to this bit has no effect.	R
0.7	Collision Test	1 : enable COL signal test. The PHY will assert the COL signal within 5120 ns in response to the assertion of TXEN. While this bit is set to one, the PHY will deassert the COL signal within 40 ns in respons to the deassertion of TXEN. 0 : normal operation. Set to 0 after power on reset.	R/W
0.6:0	Reserved	Value 0 will be read when one tries to read these bits.	R

Table 6-1 Control Register Bit Definition

B. Status Register (register #1) (R)

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	Forced to 0 and indicates that XRC is not able to perform 100BASE-T4.	R
1.14	100BASE-X Full Duplex	Forced to 0 and indicates that XRC is not able to perform 100BASE-X Fill Duplex.	R
1.13	100BASE-X Half Duplex	Forced to 1 and indicates that XRC is able to perform 100BASE-X Half Duplex.	R
1.12	10 Mb/s Full Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Full Duplex.	R
1.11	10 Mb/s Half Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Half Duplex.	R
1.10:6	Reserved	Value 0 will be released by XRC when read.	R
1.5	Auto-Negotiation	Forced to 0. Complete	R
1.4	Remote Fault	Forced to 0.	R
1.3	Auto-Negotiation Ability	Forced to 0.	R
1.2	Link Status	1 : All ports are link up. 0 : Any port is link fail. Will be set to 1 after this port is read.	R
1.1	Jabber Detect	1 : Jabber condition in any port is detected. 0 : No Jabber condition detected for all ports	R
1.0	Extended Capability	Forced to 1.	R

Table 6-2 Status Register Bit Definition

C. Port Reset Register (register #16) (R/W)

Bit(s)	Name	Description	R/W
16.15:8	Reserved	Ignored when read.	R
16.7	ResetP7	1 : reset Port 7's Logic. 0 : not reset Port 7's Logic. Power on low.	
16.6	ResetP6	1 : reset Port 6's Logic. 0 : not reset Port 6's Logic. Power on low.	R/W
16.5	ResetP5	1 : reset Port 5's Logic. 0 : not reset Port 5's Logic. Power on low.	R/W
16.4	ResetP4	1 : reset Port 4's Logic. 0 : not reset Port 4's Logic. Power on low.	R/W
16.3	ResetP3	1 : reset Port 3's Logic. 0 : not reset Port 3's Logic. Power on low.	R/W
16.2	ResetP2	1 : reset Port 2's Logic. 0 : not reset Port 2's Logic. Power on low.	R/W
16.1	ResetP1	1 : reset Port 1's Logic. 0 : not reset Port 1's Logic. Power on low.	R/W
16.0	ResetP0	1 : reset Port 0's Logic. 0 : not reset Port 0's Logic. Power on low.	R/W

Table 6-3 Port Reset Register Bit Definition

Each bit will not clear to 0 automatically whenever it is set to 1. To ensure the MX98745 works properly, one should write 0 back to Port reset register after written 1 to corresponding bit.

D. Scrambler Control Register (register #17) (R/W)

Bit(s)	Name	Description	R/W
17.15:8	Reserved	Write any value to these bits have no effect. Written value will be released onto MDIO whenever Read Command is issued	R/W
17.7	ScrenP7	1 : Enable Scrambler/Descrambler at Port 7 0 : Disable Scrambler/Descrambler at Port 7 The default value after power on is 1.	R/W
17.6	ScrenP6	1 : Enable Scrambler/Descrambler at Port 6 0 : Disable Scrambler/Descrambler at Port 6 The default value after power on is 1.	R/W
17.5	ScrenP5	1 : Enable Scrambler/Descrambler at Port 5 0 : Disable Scrambler/Descrambler at Port 5 The default value after power on is 1.	R/W
17.4	ScrenP4	1 : Enable Scrambler/Descrambler at Port 4 0 : Disable Scrambler/Descrambler at Port 4 The default value after power on is 1.	R/W
17.3	ScrenP3	1 : Enable Scrambler/Descrambler at Port 3 0 : Disable Scrambler/Descrambler at Port 3 The default value after power on is 1.	R/W
17.2	ScrenP2	1 : Enable Scrambler/Descrambler at Port 2 0 : Disable Scrambler/Descrambler at Port 2 The default value after power on is 1.	R/W
17.1	ScrenP1	1 : Enable Scrambler/Descrambler at Port 1 0 : Disable Scrambler/Descrambler at Port 1 The default value after power on is 1.	R/W
17.0	ScrenP0	1 : Enable Scrambler/Descrambler at Port 0 0 : Disable Scrambler/Descrambler at Port 0 The default value after power on is 1.	R/W

Table 6-4 Scrambler Control Register Bit Definition

Note : When SCRCTRL is set to 0, contents of this register will be disabled.

E. Port Enable Control Register (register #18) (R/W) (Continued)

Bit(s)	Name	Description	R/W
18.15:8	Reserved	Write any value to these bits have no effect. Written value will be released onto MDIO whenever Read Command is issued	R/W
18.7	EnP7	1 : Enable RX/TX functions at Port 7. 0 : Disable RX/TX functions at Port 7. The default value after power on is 1.	R/W
18.6	EnP6	1 : Enable RX/TX functions at Port 6. 0 : Disable RX/TX functions at Port 6. The default value after power on is 1.	R/W
18.5	EnP5	1 : Enable RX/TX functions at Port 5. 0 : Disable RX/TX functions at Port 5. The default value after power on is 1.	R/W
18.4	EnP4	1 : Enable RX/TX functions at Port 4. 0 : Disable RX/TX functions at Port 4. The default value after power on is 1.	R/W
18.3	EnP3	1 : Enable RX/TX functions at Port 3. 0 : Disable RX/TX functions at Port 3. The default value after power on is 1.	R/W
18.2	EnP2	1 : Enable RX/TX functions at Port 2. 0 : Disable RX/TX functions at Port 2. The default value after power on is 1.	R/W
18.1	EnP1	1 : Enable RX/TX functions at Port 1. 0 : Disable RX/TX functions at Port 1. The default value after power on is 1.	R/W
18.0	EnP0	1 : Enable RX/TX functions at Port 0. 0 : Disable RX/TX functions at Port 0. The default value after power on is 1.	R/W

Table 6-5 Port Enable Control Register Bit Definition

F. Isolation Disable Register (register #19) (R/W)

Bit(s)	Name	Description	R/W
19.15:8	Reserved	Write any value to these bits have no effect. Written value will be released onto MDIO whenever Read Command is issued	R/W
19.7	ISODIS7	1 : Port 7 Isolation function is disabled 0 : Port 7 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.6	ISODIS6	1 : Port 6 Isolation function is disabled 0 : Port 6 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.5	ISODIS5	1 : Port 5 Isolation function is disabled 0 : Port 5 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.4	ISODIS4	1 : Port 4 Isolation function is disabled 0 : Port 4 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.3	ISODIS3	1 : Port 3 Isolation function is disabled 0 : Port 3 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.2	ISODIS2	1 : Port 2 Isolation function is disabled 0 : Port 2 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.1	ISODIS1	1 : Port 1 Isolation function is disabled 0 : Port 1 Isolation function is not disabled. The default value is 0 after reset.	R/W
19.0	ISODIS0	1 : Port 0 Isolation function is disabled 0 : Port 0 Isolation function is not disabled. The default value is 0 after reset.	R/W

Table 6-6 Isolation Disable Register Bit Definition

G. Partition Disable Register (register #20) (R/W)

Bit(s)	Name	Description	R/W
20.15:8	Reserved	Write any value to these bits have no effect. Written value will be released onto MDIO whenever Read Command is issued	R/W
20.7	PTNDIS7	1 : Port 7 Parition function is disbled. 0 : Port 7 Partition function is not disabled. The default value is 0 after reset.	R/W
20.6	PTNDIS6	1 : Port 6 Parition function is disbled. 0 : Port 6 Partition function is not disabled. The default value is 0 after reset.	R/W
20.5	PTNDIS5	1 : Port 5 Parition function is disbled. 0 : Port 5 Partition function is not disabled. The default value is 0 after reset.	R/W
20.4	PTNDIS4	1 : Port 4 Parition function is disbled. 0 : Port 4 Partition function is not disabled. The default value is 0 after reset.	R/W
20.3	PTNDIS3	1 : Port 3 Parition function is disbled. 0 : Port 3 Partition function is not disabled. The default value is 0 after reset.	R/W
20.2	PTNDIS2	1 : Port 2 Parition function is disbled. 0 : Port 2 Partition function is not disabled. The default value is 0 after reset.	R/W
20.1	PTNDIS1	1 : Port 1 Parition function is disbled. 0 : Port 1 Partition function is not disabled. The default value is 0 after reset.	R/W
20.0	PTNDIS0	1 : Port 0 Parition function is disbled. 0 : Port 0 Partition function is not disabled. The default value is 0 after reset.	R/W

Table 6-7 Partition Disable Register Bit Definition (Continued)

H. Link Status Register (register #25) (R)

Bit(s)	Name	Description	R/W
25.15:8	Reserved	Always 0.	R
25.7	LinkP7	1 : Link Status is OK at port 7 0 : Link Status is Fail at Port 7 Status is updated at every LSCLK clock.	R
25.6	LinkP6	1 : Link Status is OK at port 6 0 : Link Status is Fail at Port 6 Status is updated at every LSCLK clock.	R
25.5	LinkP5	1 : Link Status is OK at port 5 0 : Link Status is Fail at Port 5 Status is updated at every LSCLK clock.	R
25.4	LinkP4	1 : Link Status is OK at port 4 0 : Link Status is Fail at Port 4 Status is updated at every LSCLK clock.	R
25.3	LinkP3	1 : Link Status is OK at port 3 0 : Link Status is Fail at Port 3 Status is updated at every LSCLK clock.	R
25.2	LinkP2	1 : Link Status is OK at port 2 0 : Link Status is Fail at Port 2 Status is updated at every LSCLK clock.	R
25.1	LinkP1	1 : Link Status is OK at port 1 0 : Link Status is Fail at Port 1 Status is updated at every LSCLK clock.	R
25.0	LinkP0	1 : Link Status is OK at port 0 0 : Link Status is Fail at Port 0 Status is updated at every LSCLK clock.	R

Table 6-8 Link Status Register Bit Definition

I. Partition Status Register (register #26) (R)

Bit(s)	Name	Description	R/W
26.15:8	Reserved	Always 0.	R
26.7	PartP7	1 : Port 7 has been partitioned 0 : Port 7 has not been partitioned Status is updated every 40 ns.	R
26.6	PartP6	1 : Port 6 has been partitioned 0 : Port 6 has not been partitioned Status is updated every 40 ns.	R
26.5	PartP5	1 : Port 5 has been partitioned 0 : Port 5 has not been partitioned Status is updated every 40 ns.	R
26.4	PartP4	1 : Port 4 has been partitioned 0 : Port 4 has not been partitioned Status is updated every 40 ns.	R
26.3	PartP3	1 : Port 3 has been partitioned 0 : Port 3 has not been partitioned Status is updated every 40 ns.	R
26.2	PartP2	1 : Port 2 has been partitioned 0 : Port 2 has not been partitioned Status is updated every 40 ns.	R
26.1	PartP1	1 : Port 1 has been partitioned 0 : Port 1 has not been partitioned Status is updated every 40 ns.	R
26.0	PartP0	1 : Port 0 has been partitioned 0 : Port 0 has not been partitioned Status is updated every 40 ns.	R

Table 6-9 Partition Status Register Bit Definition

J. Elastic Buffer Over/Underflow Status Register (register #27) (R)

Bit(s)	Name	Description	R/W
27.15:0	Reserved	Always 0.	R
27.7	EBOUF7	1 : Elastic Buffer Over/Underflow at Port 7 0 : Normal Condition. Clear to 0 after read.	R
27.6	EBOUF6	1 : Elastic Buffer Over/Underflow at Port 6 0 : Normal Condition. Clear to 0 after read.	R
27.5	EBOUF5	1 : Elastic Buffer Over/Underflow at Port 5 0 : Normal Condition. Clear to 0 after read.	R
27.4	EBOUF4	1 : Elastic Buffer Over/Underflow at Port 4 0 : Normal Condition. Clear to 0 after read.	R
27.3	EBOUF3	1 : Elastic Buffer Over/Underflow at Port 3 0 : Normal Condition. Clear to 0 after read.	R
27.2	EBOUF2	1 : Elastic Buffer Over/Underflow at Port 2 0 : Normal Condition. Clear to 0 after read.	R
27.1	EBOUF1	1 : Elastic Buffer Over/Underflow at Port 1 0 : Normal Condition. Clear to 0 after read.	R
27.0	EBOUF0	1 : Elastic Buffer Over/Underflow at Port 0 0 : Normal Condition. Clear to 0 after read.	R

Table 6-10 Elastic Buffer Over/Underflow Status Register Bit Definition

K. Jabber Status Register (register #28) (R)

Bit(s)	Name	Description	R/W
28.15:0	Reserved	Always 0.	R
28.7	JABP7	1 : Receive Jabber Active at Port 7 0 : No Jabber condition at Port 7	R
28.6	JABP6	1 : Receive Jabber Active at Port 6 0 : No Jabber condition at Port 6	R
28.5	JABP5	1 : Receive Jabber Active at Port 5 0 : No Jabber condition at Port 5	R
28.4	JABP4	1 : Receive Jabber Active at Port 4 0 : No Jabber condition at Port 4	R
28.3	JABP3	1 : Receive Jabber Active at Port 3 0 : No Jabber condition at Port 3	R
28.2	JABP2	1 : Receive Jabber Active at Port 2 0 : No Jabber condition at Port 2	R
28.1	JABP1	1 : Receive Jabber Active at Port 1 0 : No Jabber condition at Port 1	R
28.0	JABP0	1 : Receive Jabber Active at Port 0 0 : No Jabber condition at Port 0	R

Table 6-11 Jabber Status Register Bit Definition

L. Isolation Status Register (register #29) (R)

Bit(s)	Name	Description	R/W
29.15:0	Reserved	Always 0.	R
29.7	ISO7	1 : Port Isolation is occuring at port 7, 0 : Port Isolation is not occuring at port 7.	R
29.6	ISO6	1 : Port Isolation is occuring at port 6, 0 : Port Isolation is not occuring at port 6.	R
29.5	ISO5	1 : Port Isolation is occuring at port 5, 0 : Port Isolation is not occuring at port 5.	R
29.4	ISO4	1 : Port Isolation is occuring at port 4, 0 : Port Isolation is not occuring at port 4.	R
29.3	ISO3	1 : Port Isolation is occuring at port 3, 0 : Port Isolation is not occuring at port 3.	R
29.2	ISO2	1 : Port Isolation is occuring at port 2, 0 : Port Isolation is not occuring at port 2.	R
29.1	ISO1	1 : Port Isolation is occuring at port 1, 0 : Port Isolation is not occuring at port 1.	R
29.0	ISO0	1 : Port Isolation is occuring at port 0, 0 : Port Isolation is not occuring at port 0.	R

Table 6-12 Isolation Status Register Bit Definition

M. Configuration Register (register #31) (R/W)

Bit(s)	Name	Description	R/W
31.15	Reserved	Reserved for further usage.	R/W
31.14	L40H80	1:Internal arbiter will qualify EDENL for more than 80 ns. 0:Internal arbiter will qualify EDENL for more than 40 ns. Power on low.	R/W
31.13:12	Reserved	Reserved for further usage.	
31.11	EECF	Power on reset value of LDS0. After power on reset, Write 1 to this bit will not make EEPROM operation. When EECF is low, then value on corresponding pins (known as hardwire setting) will be latched by MX98745 and overwrite the default setting of MX98745.	R
31.10	Reserved	Force to High all the time.	R/W
31.9	MONITOR	1 : Set XRC II to monitor mode and monitor serial output of internal state machine through LED7..0 0 : Put MX98745 in normal mode.	R
31.8	INTARB	0:Internal Arbitor function is disabled. 1:Internal Arbitor function is enabled Power on low.	R/W
31.7	FLWSPEC	1 : Partition function meets IEEE 802.3u i.e. when two ports collide more than 128 times, two ports will be partitoned by MX98745 simultaneously. 0 : Those ports which Receive after Transmit will be partitioned.(Same as MX98741) i.e. ports encounter transmit collision will be paritioned only.	R/W
		Value on LED0 will be stored in this bit in case EECONF is 0.	
31.6	PXM	1:PCS type MII for port0 0:MAC type MII for port0 value on LED1 will be stored at this bit after power on reset. When TXXMII is set to 1, this bit has no effect. Contents will not be overwritten by EEPROM.	R/W
31.5	TXXMII	1 : TX port is programmed (5B) for port 0 0 : MII mode (4B) is programmed for port 0 After power on reset, value on LED2 will be stored on this bit. Contents will not be overwritten while loading EEPROM.	R/W
31.4:0	PHY[4:0]	Physical address of MX98745. When EECONF is set to 0 (Disabled), value on LED[7:3] will be stored in these five bits at the rising edge of RESETL. If EECONF is set to high, value from EEPROM will overwrite the hardwire setting.	R/W

Table 6-13 Configuration Register Bit Definition

6.4 EEPROM Mapping

Word #	Bit 15 8	7 0
5	MSB of Register #31	LSB of Register #31
4	MSB of Register #20	LSB of Register #20
3	MSB of Register #19	LSB of Register #19
2	MSB of Register #18	LSB of Register #18
1	MSB of Register #17	LSB of Register #17
0	MSB of Register #16	LSB of Register #16

7.0 ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Supply Voltage (VCC)	4.75V to 5.25V
DC Input Voltage (Vin)	-0.5V to VCC+0.5V
DC Output Voltage (Vout)	-0.5V to VCC+0.5V
Storage Temperature Range (TSTG)	-55 C to 150 C
Power Dissipation (PD)	750 mW
ESD rating (Rzap = 1.5K, Czap = 100pF)	2000V

Table 7-1 Absolute Maximum Rating for MX98745

Notice :
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cauase permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

8.0 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
A. Supply Current					
ICC	Average Active (TXing/ RXing) Supply Current	X1 = 25MHz VIN = Switching	-	150	mA
ICCIDLE	Average Idle Supply Current	X1 = 25MHz VIN=VCC/GND	-	10	mA
IDD	Static IDD Current	X1=Undriven	-	600	uA
B. TTL Inputs, Outputs, Tri-States					
Vil	Maximum Low Level Input Voltage	GND = 0V	-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	VCC+0.5	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA
Voh	Minimum High Level Output Voltage (Others/MII/Expansion)	Ioh = -2mA/ -4mA/ -8mA	2.4	-	V
Vol	Maximum Low Level Output Voltage (Others/MII/Expansion)	Iol = 2mA/ 4mA/ 8mA	-	0.4	V
Ioz	Maximum TRI-STATE Output Leakage Current	VOUT=VCC/ GND	-10.0	10.0	uA
C. CMOS Inputs, Outputs					
Voh	Minimum High Level Output Voltage	Ioh = -20uA	VCC-0.1	-	V
Vol	Maximum Low Level Output Voltage	Iol = 20uA	-	0.1	V
Vil	Maximum Low Level	Input Voltage	-	0.8	V
Vih	Minimum High Level	Input Voltage	2.0	-	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA

Table 8-1 DC Characteristics for MX98745

9.0 AC CHARACTERISTICS AND WAVEFORMS

A. Media Independent Interface

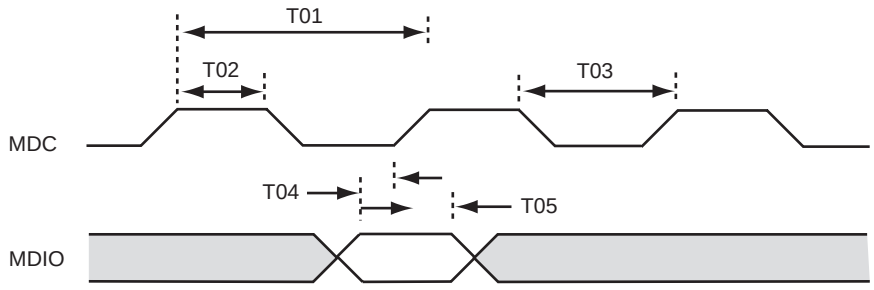


Figure 9-1 MDIO Timing Relationship MDC

Symbol	Description	MIN.	MAX.	UNIT
T01	Period for MDC	400	-	ns
T02	High Time for MDC	160	-	ns
T03	Low Time for MDC	160	-	ns
T04	MDIO Setup to MDC rising edge (sourced by STA)	10	-	ns
T05a	MDIO Hold to MDC rising edge (sourced by STA)	10	-	ns
T05b	MDIO Hold to MDC rising edge (source by XRC)	18	25	ns

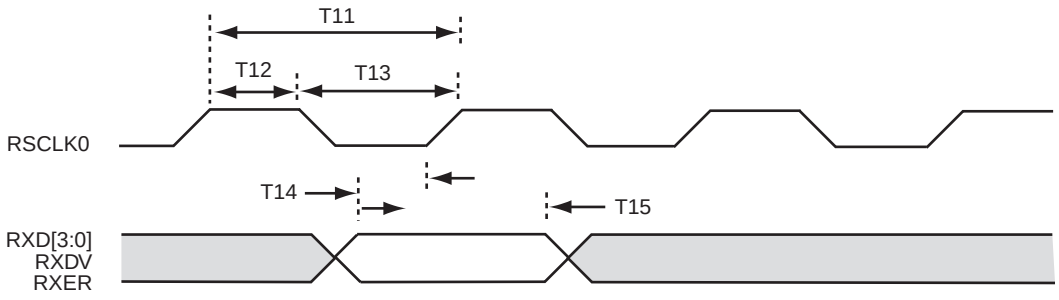


Figure 9-2 Receive Signal Timing Relationships for MII mode

Symbol	Description	MIN.	MAX.	UNIT
T11	RSCLK0 Period (Note 1)	40	40	ns
T12	RSCLK0 High Time	10	-	ns
T13	RSCLK0 Low Time	7	-	ns
T14	RXD[3:0]/RXDV/RXER Setup Time to RSCLK0 rising edge (Note 2)	10	-	ns
T15	RXD[3:0]/RXDV/RXER Hold Time to RSCLK0 rising edge (Note 2)	10	-	ns

Note 1 : The accurate RSCLK frequency shall be 25 MHz +/- 50 ppm.

Note 2 : The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

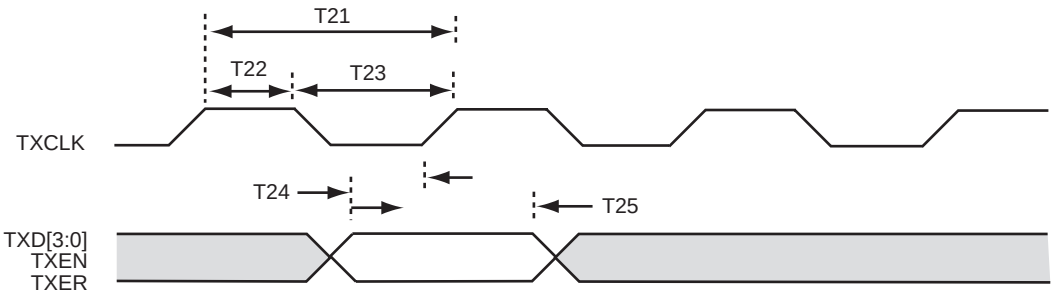


Figure 9-3 Trannsmit Signal Timing Relationships at the MII

Symbol	Description	MIN.	MAX.	UNIT
T21	TXCLK Period (Note 1)	40	40	ns
T22	TXCLK High Time	20	-	ns
23	TXCLK Low Time	18	-	ns
T24	TXD[3:0]/TXEN/TXER Setup Time to TXCLK rising edge (Note 2)	20	-	ns
T25	TXD[3:0]/TXEN/TXER Hold Time to TXCLK rising edge (Note 2)	15	-	ns

Note 1 : The accurate TXCLK frequency shall be 25 MHz +/- 50 ppm. In PCS type MII, this signal is outputed by MX9745. In MAC type MII, this signal is input to MX98745.

Note 2 : The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region. (see section 22.3 in [1])

B. Data Transceiver Interface

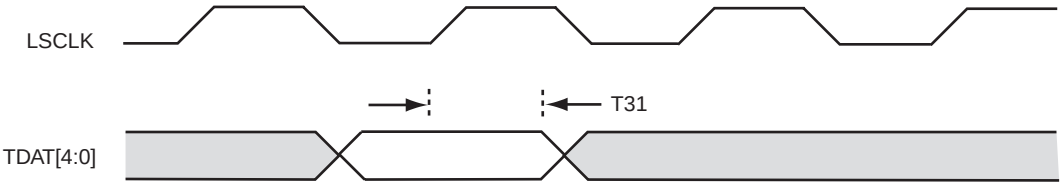


Figure 9-4 Trannsmit Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
T31	TDAT[4:0] to LSCLK Delay Time	10	15	ns

Note : Tested under 30pF loading.

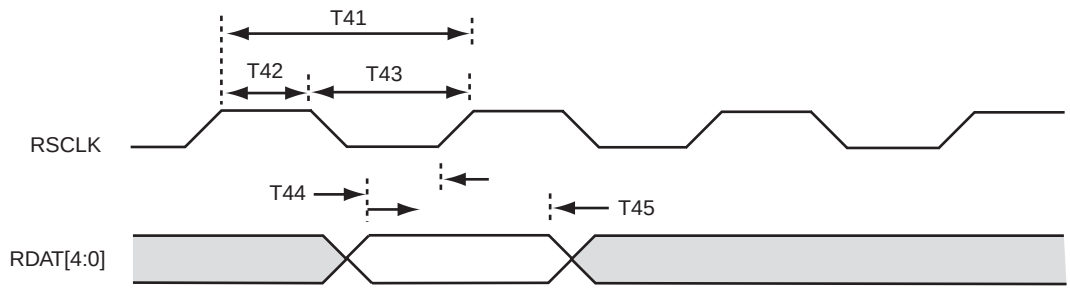


Figure 9-5 Receive Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
41	RSCLK Period (Note 1)	40	40	ns
T42	RSCLK Pulse Width High	11	-	n
T43	RSCLK Pulse Width Low Time	20	-	ns
T44	RDAT[4:0] Valid to RSCLK Rise	2	-	ns
T45	RSCLK Rise to RDAT[4:0] Invalid	4	-	ns

Note 1 : The accurate RSCLK frequency shall be 25 MHz +/- 50 ppm.

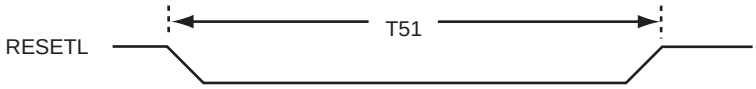


Figure 9-6 Timing Constraint RESEL

Symbol	Description	MIN.	MAX.	UNIT
T51	Pulse Width for RESETL	800	-	us

Note : RESETL must keep active low until LSCLK is stable more than 200 us.

C. Expansion Port Interface

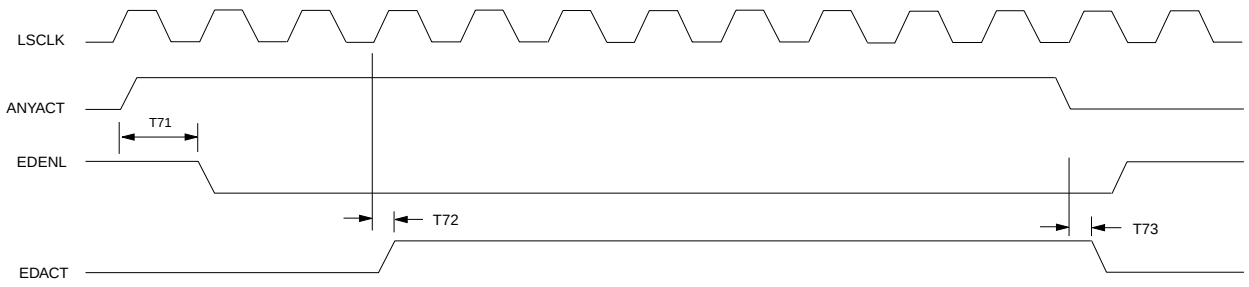


Figure 9-7 Expansion Port with One port activates

Symbol	Description	MIN.	MAX.	UNIT
T71	ANYACT asserted to EDENL asserted (Note 3)		80	ns
T72	LSCLK rising to EDACT asserted (Note 1, 2)		20	ns
T73	LSCLK rising to EDACT deassert		20	ns

Note 1 : EDENL will be filtered by 2 LSCLK clock within MX98745. Whenever MX98745 detects EDENL, it will assert EDACT at the rising edge of LSCLK

Note 2 : Expansion port data will be released onto EDAT[4:0] at the next LSCLK rising edge right after EDACT is asserted which is not shown in this figure.

Note 3 : ANYACT has not any timing relationship to LSCLK in MX98745. i.e. it is asynchronous to LSCLK.

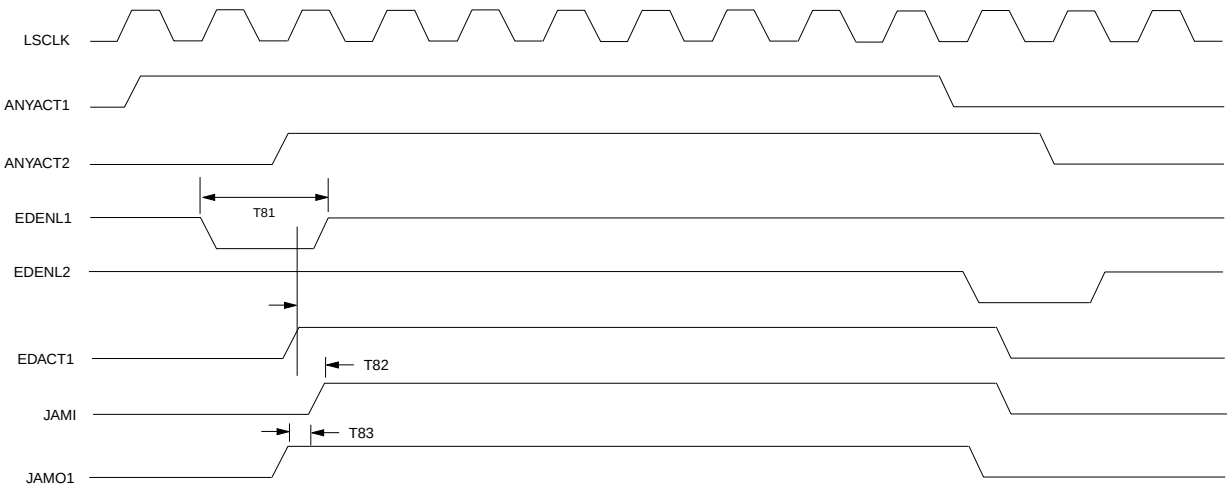


Figure 9-8 Expansion Port with Collision (Note 1)

Symbol	Description	MIN.	MAX.	UNIT
T81	Valid EDENL duration to make EDACT active	80		ns
T82	Collision Condition to JAMI asserted (Note 2)		10	ns
T83	JAMO asserted to JAMI asserted (Note 3)		10	ns

Note 1 : EDENL2 asserted after collision will not make EDACT2 assert in MX98745 due to MX98745 will mask activity from expansion port from ces sation of collision to cessation of ANYACT2.
Note 2 : Deassert timing is the same
Note 3 : Deassert timing is the same. Either T72 or T73 should cause JAMI assert
Note 4 : EDENL, JAMI and EDCRS (not shown in this timing) should be filtered by LSCLK to resolve asynchronous issue.

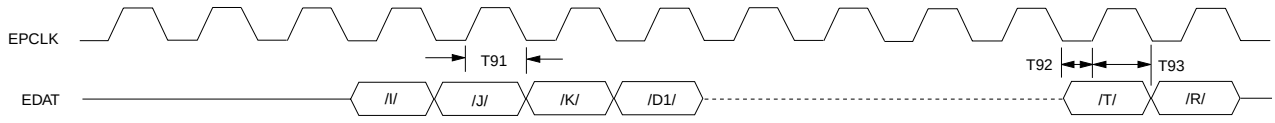


Figure 9-9 EPCLK and EDAT Timing Relationship

Symbol	Description	MIN.	MAX.	UNIT
T91	EPCLK to EDAT delay time (EPCLK and EDAT outputed from MX98745)	12	16	ns
T92	EDAT Setup Time (Input to MX98745)	5	-	ns
T93	EDAT Hold Time (Input to MX98745)	5	-	ns

D. LED Display

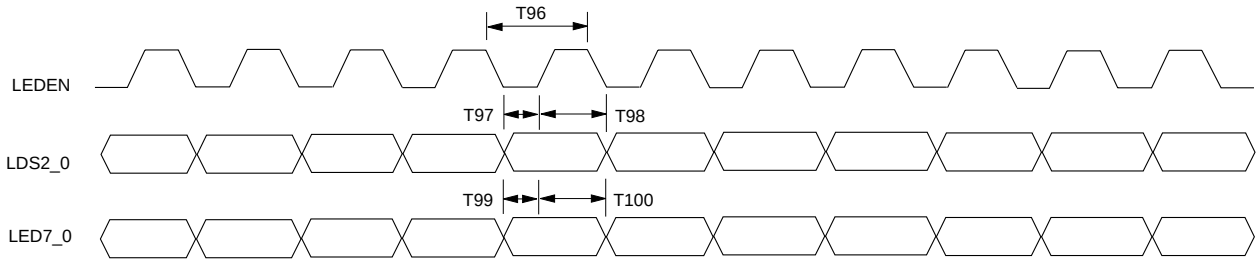


Figure 9-10 Timing Relationship for LED Display

Symbol	Description	MIN.	MAX.	UNIT
T96	LEDEN Period	9.9	10.1	ms
T97	LDS2_0 Setup Time	4.0	-	ms
T98	LDS2_0 Hold Time	4.9	-	ms
T99	LED7_0 Setup Time	4.0	-	ms
T100	LED7_0 Hold Time	4.9	-	ms

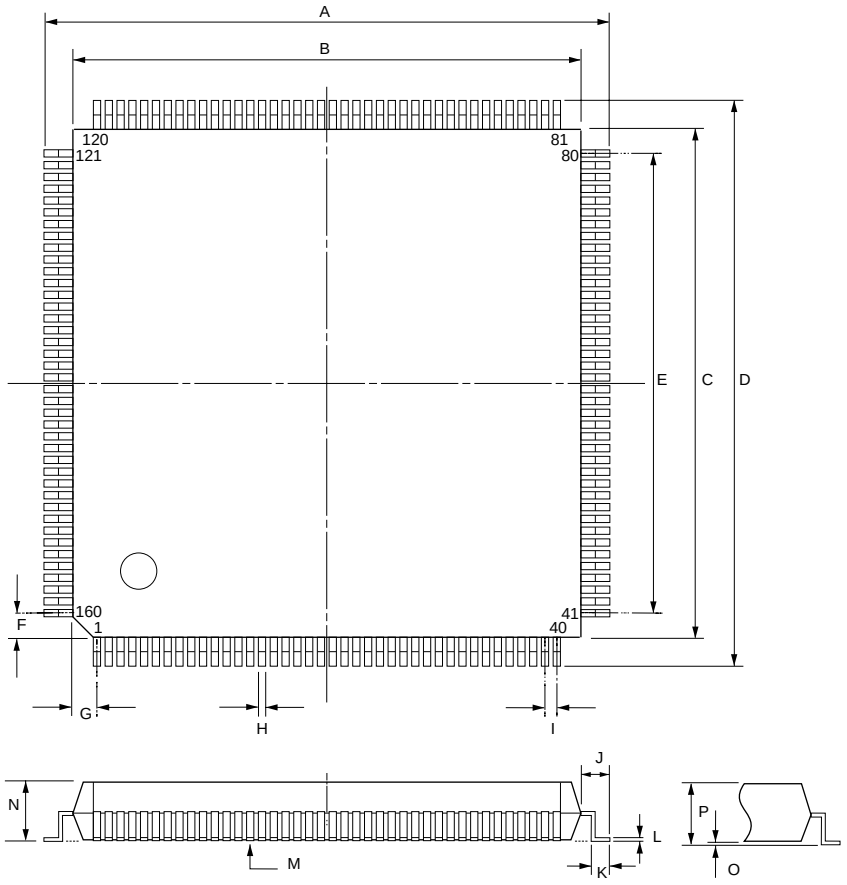
Note :
Where LED7_0 definition relative to LDS2_0 configuration, please reference pin description of LDS2_0

10.0 PACKAGE INFORMATION

160-PIN PLASTIC QUAD FLAT PACK

ITEM	MILLIMETERS	INCHES
A	31.20 ± .30	1.228 ± .012
B	28.00 ± .10	1.102 ± .004
C	28.00 ± .10	1.102 ± .004
D	31.20 ± .30	1.228 ± .012
E	25.35	.999
F	1.33 [REF]	.052 [REF]
G	1.33 [REF]	.052 [REF]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF.]	.063 [REF.]
K	.80 ±.20	.031 ± .008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.
P	3.68 max.	.145 max.

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.



HISTORY OF CHANGE MADE

Rev. No.	Description	Date
1.1	P 1, 9, 10, 11:Change scale for utilization and collision rate LED display.	JAN. 31, 1997
1.2	P28:Change configuration register (register #31) description.	MAR. 12, 1997
1.3	P30:Change 7.0 ABSOLUTE MAXIMUM RATINGS:Power Dissipation, from 1500mw to 750mw.	
	P30:Change 8.0 DC Characteristics:ICC(MAX.), form 300mA to 150mA.	JUL. 03, 1997
1.4	P2:Change expansion port signal name from EPCLK to ANYACT.	JUL. 10, 1998

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