NBXDBA012

3.3 V, 106.25 MHz / 212.5 MHz LVPECL Clock Oscillator

The NBXDBA012 dual frequency crystal oscillator (XO) is designed to meet today's requirements for 3.3 V LVPECL clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide selectable 106.25 MHz or 212.5 MHz, ultra low jitter and phase noise LVPECL differential output. This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000.

Features

- LVPECL Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise – 0.4 ps (12 kHz – 20 MHz)
- Selectable Output Frequency – 106.25 MHz / 212.5 MHz
- Frequency Stability – ±50 PPM
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range 3.3 V ±10%
- This is a Pb–Free Device

Applications

- 1X and 2X Fiber Channel
- Host Bus Adapter

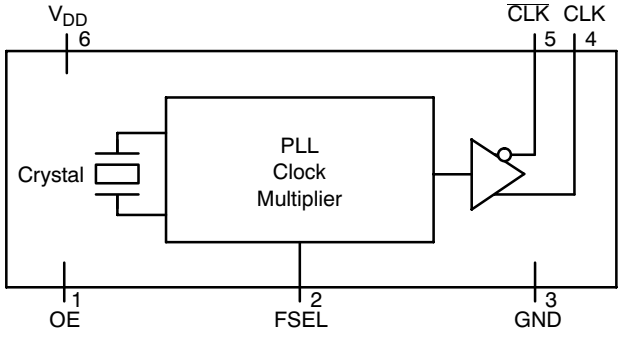

Figure 1. Simplified Logic Diagram

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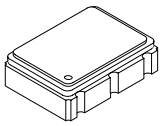
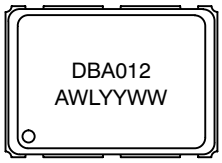


6 PIN CLCC
TBD SUFFIX
CASE 848AB

MARKING DIAGRAM



DBA012	= NBXDBA012 (±50 PPM)
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NBXDBA012LN1TAG	CLCC–6 (Pb–Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

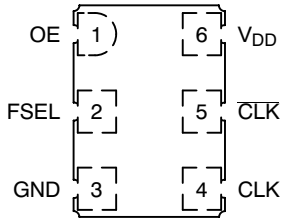


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
2	FSEL	LVTTL/LVCMOS Control Input	Output Frequency Select Pin. Pin will default to logic HIGH when left open. See Output Frequency Select pin description Table 3.
3	GND	Power Supply	Ground 0 V.
4	CLK	LVPECL Output	Non−Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2$ V.
5	$\overline{CLK}$	LVPECL Output	Non−Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to $V_{TT} = V_{DD} - 2$ V.
6	V_{DD}	Power Supply	Positive power supply voltage. Voltage should not exceed 3.3 V ±10%.

Table 2. OUTPUT ENABLE TRI−STATE FUNCTION

OE Pin	Output Pin
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. OUTPUT FREQUENCY SELECT

FSEL Pin	Output Frequency (MHz)
Open (pin will float high)	106.25
HIGH Level	106.25
LOW Level	212.5

Table 4. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
I_{out}	LVPECL Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−55 to +120	°C
T_{sol}	Wave Solder	See Figure 6		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. DC CHARACTERISTICS (V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current (Note 2)			80	95	mA
V_{IH}	OE and FSEL Input HIGH Voltage		2000		V_{DD}	mV
V_{IL}	OE and FSEL Input LOW Voltage		GND − 300		800	mV
I_{IH}	Input HIGH Current OE FSEL		−100 −100		+100 +100	μA
I_{IL}	Input LOW Current OE FSEL		−100 −100		+100 +100	μA
V_{OH}	Output HIGH Voltage (Note 2)	 V_{DD} = 3.3 V	V_{DD}−1145 2155		V_{DD}−895 2405	mV
V_{OL}	Output LOW Voltage (Note 2)	 V_{DD} = 3.3 V	V_{DD}−1945 1355		V_{DD}−1600 1700	mV
V_{OUTPP}	Output Voltage Amplitude (Note 2)			780		mV

NOTE: NBX circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2. Measurement taken with outputs terminated with 50 ohm to V_{DD}−2 V.

Table 7. AC CHARACTERISTICS (V_{DD} = 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency	FSEL = HIGH		106.25		MHz
		FSEL = LOW		212.5		
Δf	Frequency Stability	10 Years Aging			±50	ppm
Φ_{NOISE}	Phase−Noise Performance f_{CLKout} = 106.25 MHz/212.5 MHz	100 Hz of Carrier		−103/−90		dBc/Hz
		1 kHz of Carrier		−125/−122		dBc/Hz
		10 kHz of Carrier		−135/−127		dBc/Hz
		100 kHz of Carrier		−137/−128		dBc/Hz
		1 MHz of Carrier		−137/−131		dBc/Hz
		10 MHz of Carrier		−162/−159		dBc/Hz
$t_{jit}(\Phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.4	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		3	10	ps
	Cycle to Cycle, Peak−to−Peak	1000 Cycles		15	35	ps
	Period, RMS	10,000 Cycles		2	5	ps
	Period, Peak−to−Peak	10,000 Cycles		10	25	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		48	50	52	%
t_R	Output Rise Time (20% and 80%)			150	550	ps
t_F	Output Fall Time (80% and 20%)			150	550	ps
t_{start}	Start−up Time			1	5	ms
	Aging	1st Year			3	ppm
		Every Year After 1st			1	ppm

NOTE: NBX circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

Table 8. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL−STD−833, Method 2002, Condition B
Solderability	Mechanical	MIL−STD−833, Method 2003
Vibration	Mechanical	MIL−STD−833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL−STD−202, Method 215
Resistance to Soldering Heat	Mechanical	MIL−STD−203, Method 210, Condition I or J
Thermal Shock	Environment	MIL−STD−833, Method 1001, Condition A
Moisture Resistance	Environment	MIL−STD−833, Method 1004

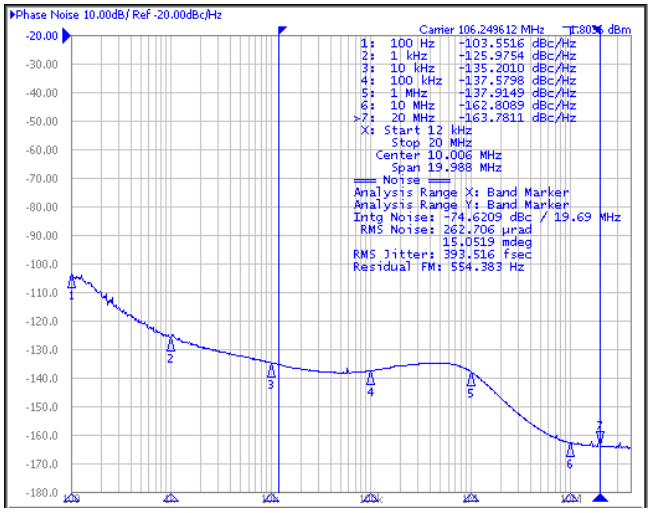


Figure 3. Typical Phase Noise Plot @ 106.25 MHz

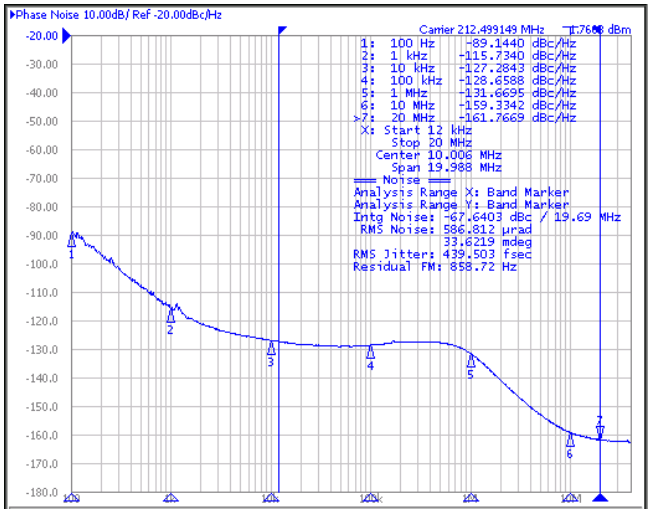


Figure 4. Typical Phase Noise Plot @ 212.5 MHz

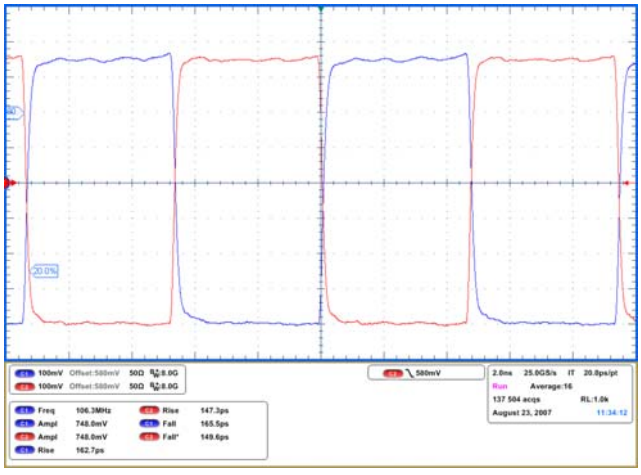


Figure 5. Typical Output Waveform @ 106.25 MHz

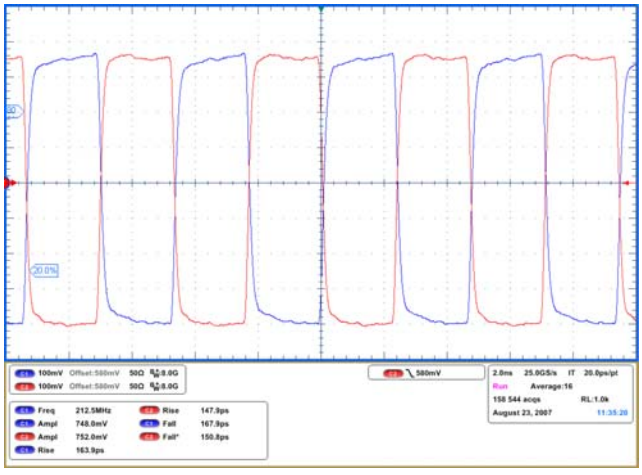


Figure 6. Typical Output Waveform @ 212.5 MHz

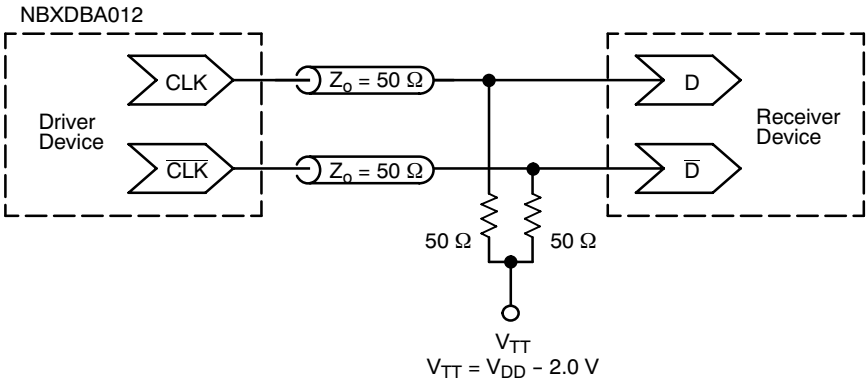


Figure 7. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

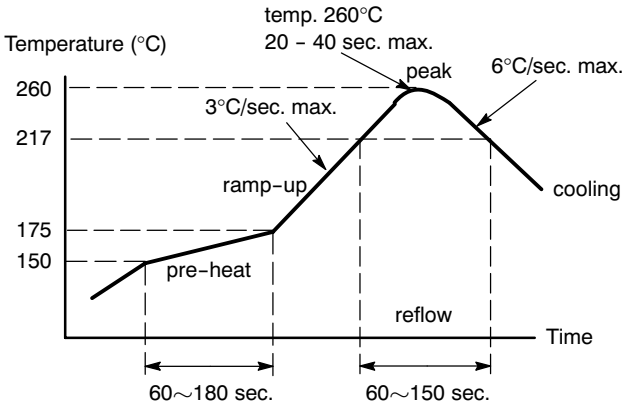
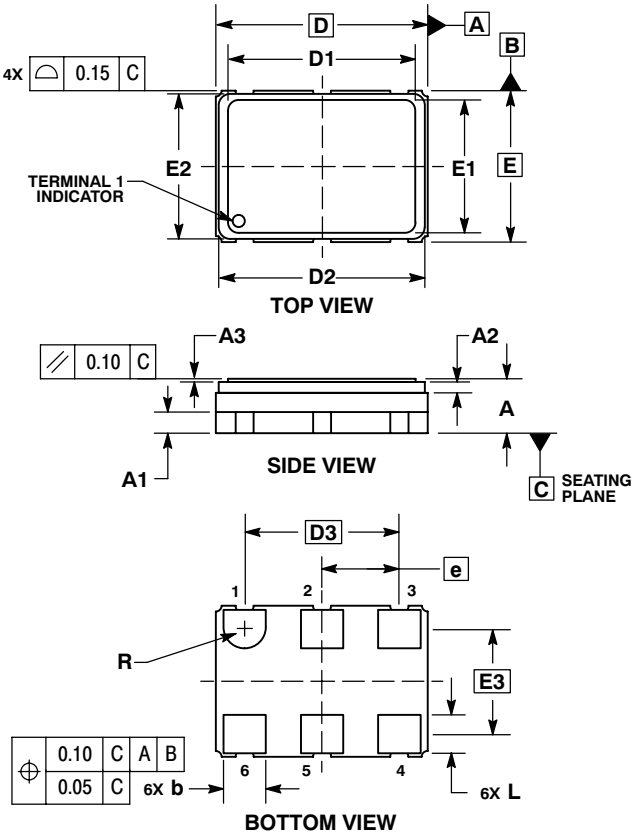


Figure 8. Recommended Reflow Soldering Profile

NBXDBA012

PACKAGE DIMENSIONS

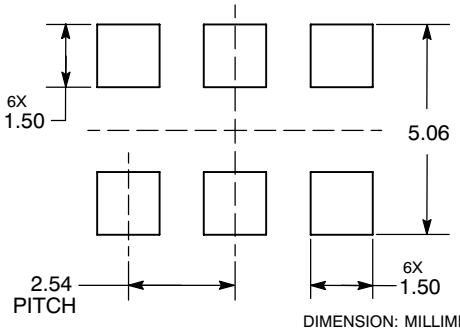
6 PIN CLCC, 7x5, 2.54P
CASE 848AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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