74LVC594A

8-bit shift register with output register

Rev. 01 — 24 May 2007 Product data sheet

1. General description

The 74LVC594A is an 8-bit serial-in/serial or parallel-out shift register with a storage register. Separate clock and reset inputs are provided on both shift and storage registers.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial Power-down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The shift register has a serial input (DS) and a serial output (Q7S) for cascading purposes. Data is shifted on the positive-going transitions of the SHCP input. The data in the shift register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. A LOW level on one of the two register reset pins ($\overline{SHR}$ and $\overline{STR}$) will clear the corresponding register.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM JESD22-A114-D exceeds 2000 V
  - CDM JESD22-C101-C exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC594AD	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC594APW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC594ABQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

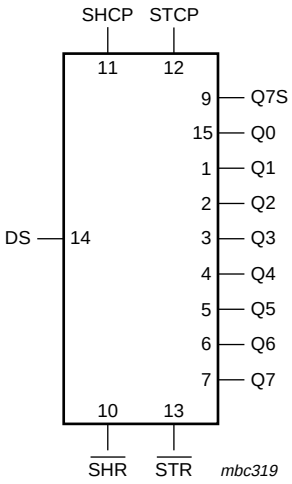


Fig 1. Logic symbol

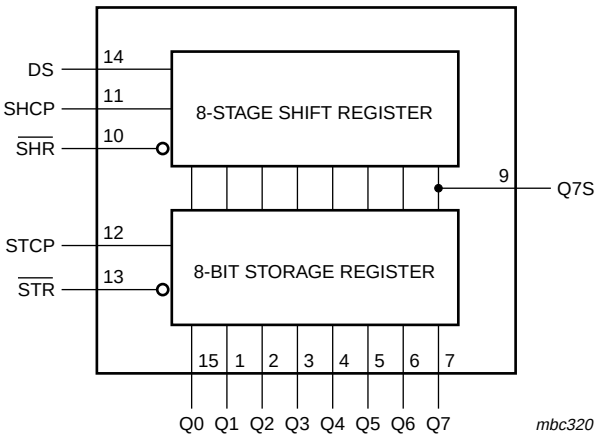


Fig 2. Functional diagram

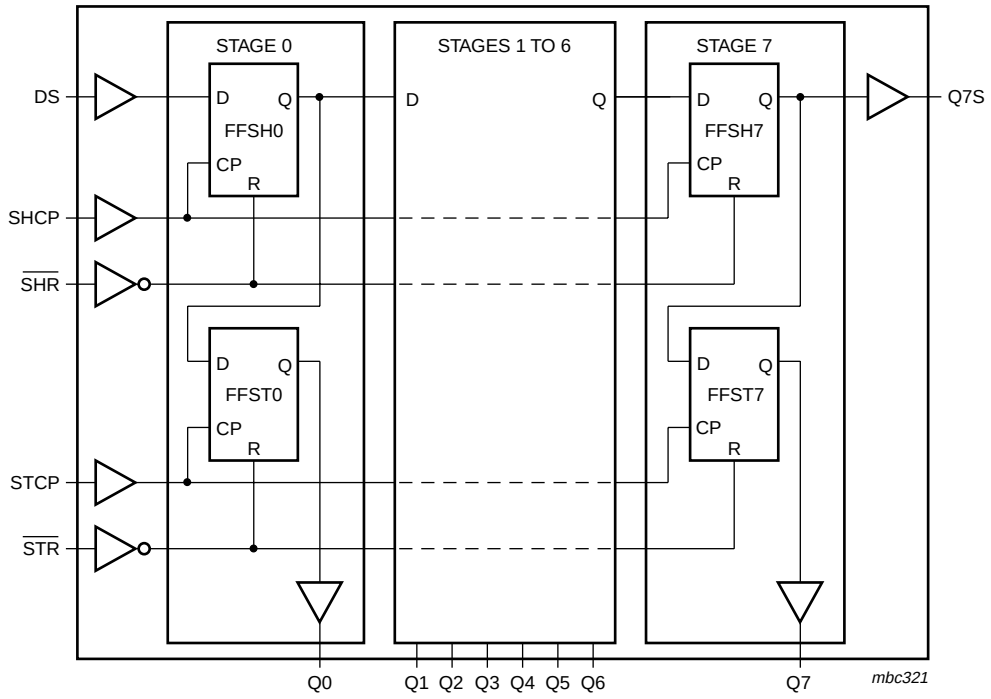


Fig 3. Logic diagram

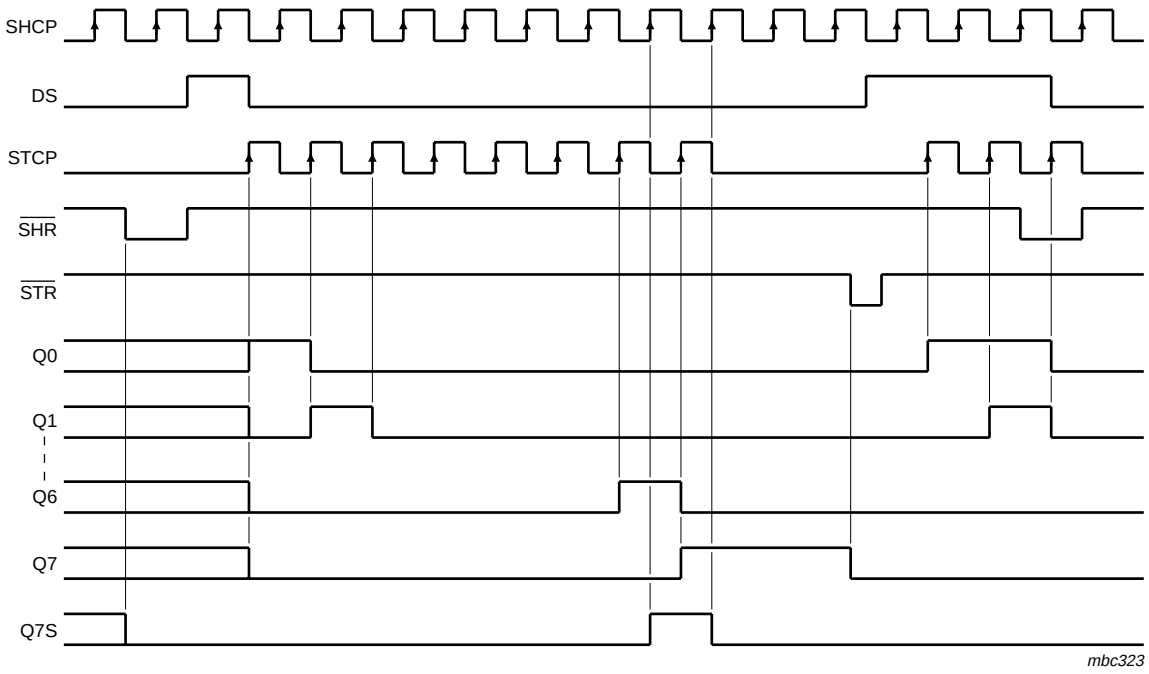


Fig 4. Timing diagram

6. Pinning information

6.1 Pinning

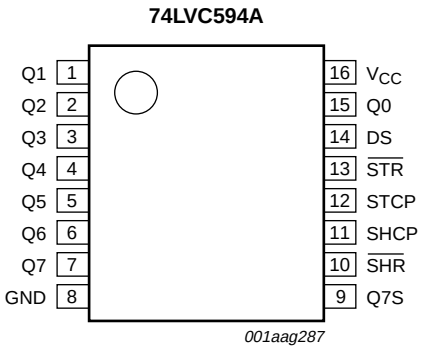
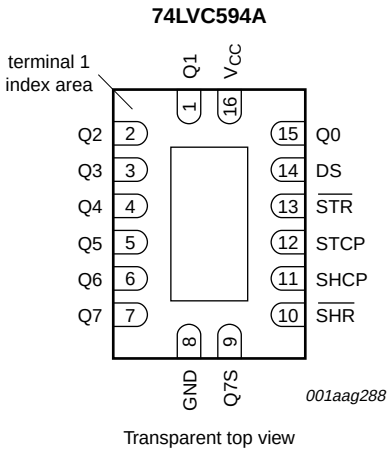


Fig 5. Pin configuration SO16 and TSSOP16



Transparent top view

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q[0:7]	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{SHR}$	10	shift register reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{STR}$	13	storage register reset (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Input					Output		Function
SHCP	STCP	$\overline{SHR}$	$\overline{STR}$	DS	Q7S	Qn	
X	X	L	X	X	L	NC	a LOW-state on $\overline{SHR}$ only affects the shift register
X	X	X	L	X	NC	L	a LOW-state on $\overline{STR}$ only affects the storage register
X	↑	L	H	X	L	L	empty shift register loaded into storage register
↑	X	H	X	H	Q6S	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	H	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	H	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW-to-HIGH transition;
X = don't care;
NC = no change;

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	3-state	[1]	–0.5	6.5	V
		output HIGH or LOW state	[1]	–0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	3-state	0	-	5.5	V
		output HIGH or LOW state	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	µA

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	0.1	10	-	20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 1.65 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	SHCP to Q7S; see Figure 7	[2]						
		V_{CC} = 1.2 V		-	17.5	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	5.2	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	3.2	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V		1.5	3.5	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	3.1	6.7	1.5	7.7	ns
		STCP to Qn; see Figure 8	[2]						
		V_{CC} = 1.2 V		-	19.3	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	7.6	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	4.8	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V		1.5	5.2	7.6	1.5	8.7	ns
		V_{CC} = 3.0 V to 3.6 V		1.2	4.5	6.7	1.2	7.7	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	$\overline{SHR}$ to Q7S; see Figure 11						
		V_{CC} = 1.2 V	-	12.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	5.0	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.8	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V	1.2	3.9	7.6	1.2	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	3.3	6.7	1.2	7.7	ns
		$\overline{STR}$ to Qn; see Figure 12						
		V_{CC} = 1.2 V	-	20.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	7.7	15.8	2.0	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	5.0	8.1	1.5	9.3	ns
		V_{CC} = 2.7 V	1.2	5.3	7.6	1.2	8.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	4.4	6.7	1.2	7.7	ns
t_W	pulse width	SHCP, STCP HIGH or LOW; see Figure 7 and Figure 8						
		V_{CC} = 1.65 V to 1.95 V	6.0	2.5	-	7.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.0	-	5.5	-	ns
		V_{CC} = 2.7 V	4.5	1.5	-	5.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.5	-	4.5	-	ns
		$\overline{SHR}$, $\overline{STR}$ LOW; see Figure 11 and Figure 12						
		V_{CC} = 1.65 V to 1.95 V	6.0	2.5	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	2.0	-	4.5	-	ns
		V_{CC} = 2.7 V	2.5	1.5	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.5	-	3.0	-	ns
t_{su}	set-up time	DS to SHCP; see Figure 9						
		V_{CC} = 1.65 V to 1.95 V	5.0	1.0	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	0.8	-	4.5	-	ns
		V_{CC} = 2.7 V	2.0	0.6	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	0.6	-	2.5	-	ns
		$\overline{SHR}$ to STCP; see Figure 10						
		V_{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V_{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns
		SHCP to STCP; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	8.0	3.5	-	8.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	5.0	2.1	-	5.5	-	ns
		V_{CC} = 2.7 V	4.0	1.8	-	4.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	4.0	1.7	-	4.5	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	DS to SHCP; see Figure 9							
		V_{CC} = 1.65 V to 1.95 V		1.5	0.2	-	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	0.1	-	2.0	-	ns
		V_{CC} = 2.7 V		1.5	–0.1	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	–0.2	-	1.5	-	ns
t_{rec}	recovery time	$\overline{SHR}$ to SHCP, $\overline{STR}$ to STCP; see Figure 11 and Figure 12							
		V_{CC} = 1.65 V to 1.95 V		5.0	–2.7	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V		4.0	–1.5	-	4.5	-	ns
		V_{CC} = 2.7 V		2.0	–1.0	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	–1.0	-	2.5	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Figure 7 and Figure 8							
		V_{CC} = 1.65 V to 1.95 V		80	130	-	70	-	MHz
		V_{CC} = 2.3 V to 2.7 V		100	140	-	90	-	MHz
		V_{CC} = 2.7 V		110	150	-	100	-	MHz
		V_{CC} = 3.0 V to 3.6 V		130	180	-	115	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	50	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	45	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	44	-	-	-	pF

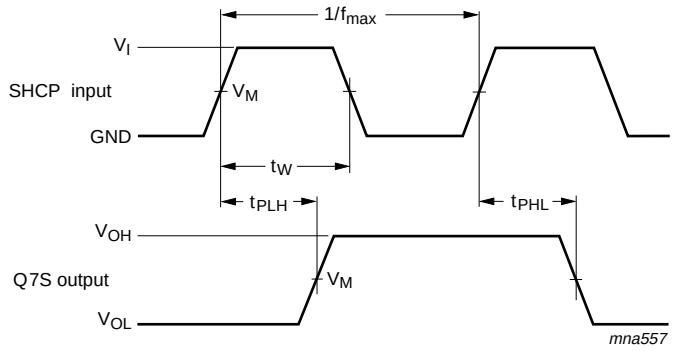
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

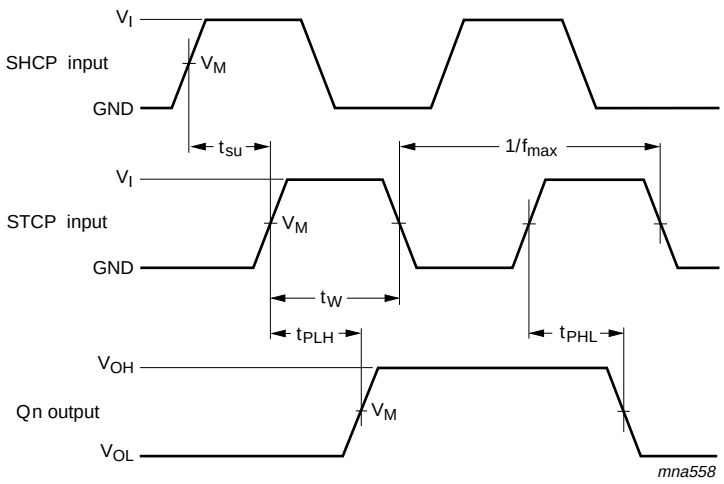
12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

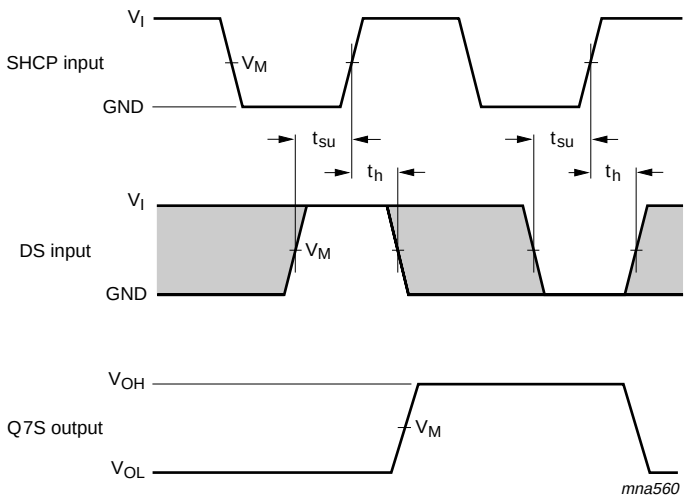
Fig 7. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 8. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time

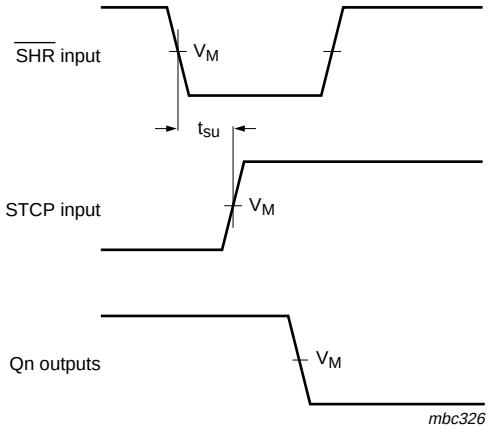


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

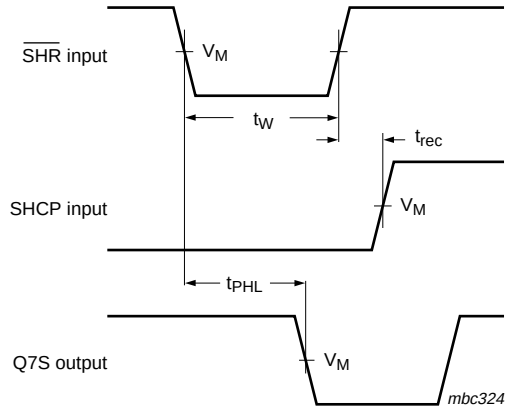
Fig 9. The data set-up and hold times for the serial data input (DS)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

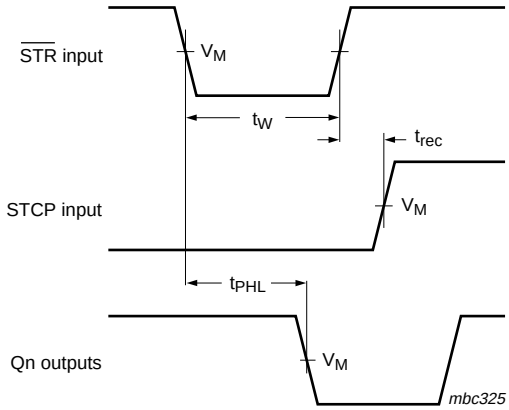
Fig 10. The shift reset ($\overline{SHR}$) to storage clock (STCP) set-up times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 11. The shift reset ($\overline{SHR}$) pulse width, the shift reset to serial data output (Q7S) propagation delays and the shift reset to shift clock (SHCP) recovery time



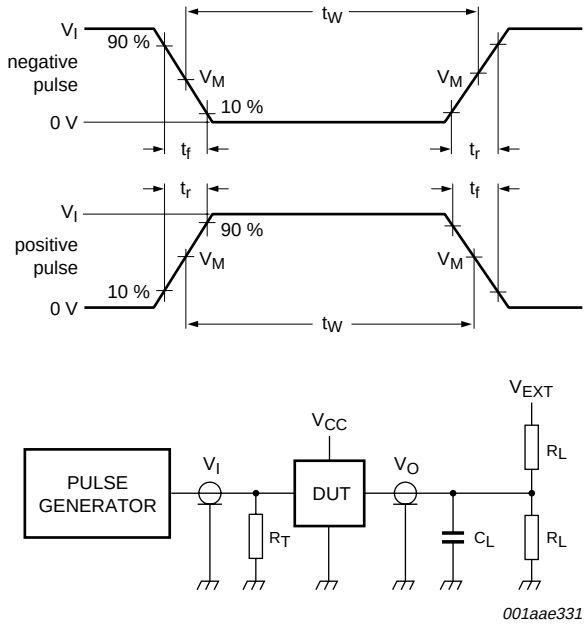
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 12. The storage reset ($\overline{STR}$) pulse width, the storage reset to parallel data output (Qn) propagation delays and the storage reset to storage clock (STCP) recovery time

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
$V_{CC} < 2.7$ V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
$V_{CC} \geq 2.7$ V	1.5 V	1.5 V



Test data is given in Table 9. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

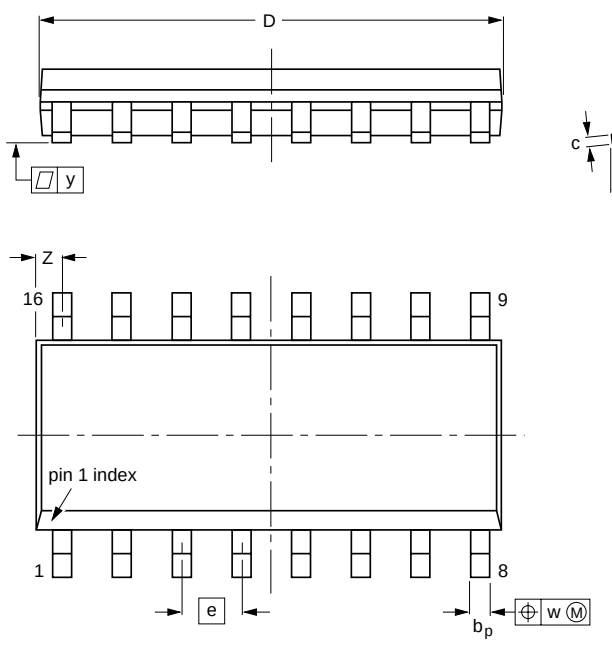
Fig 13. Load circuitry for switching times

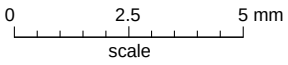
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

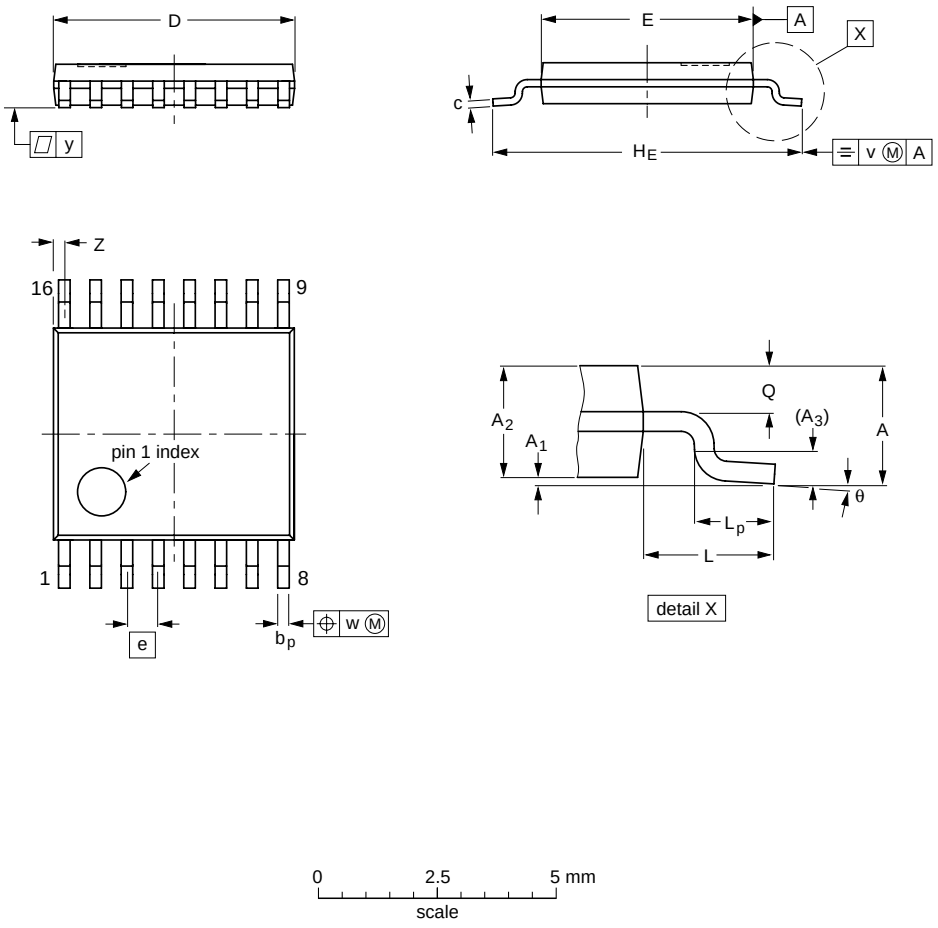
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

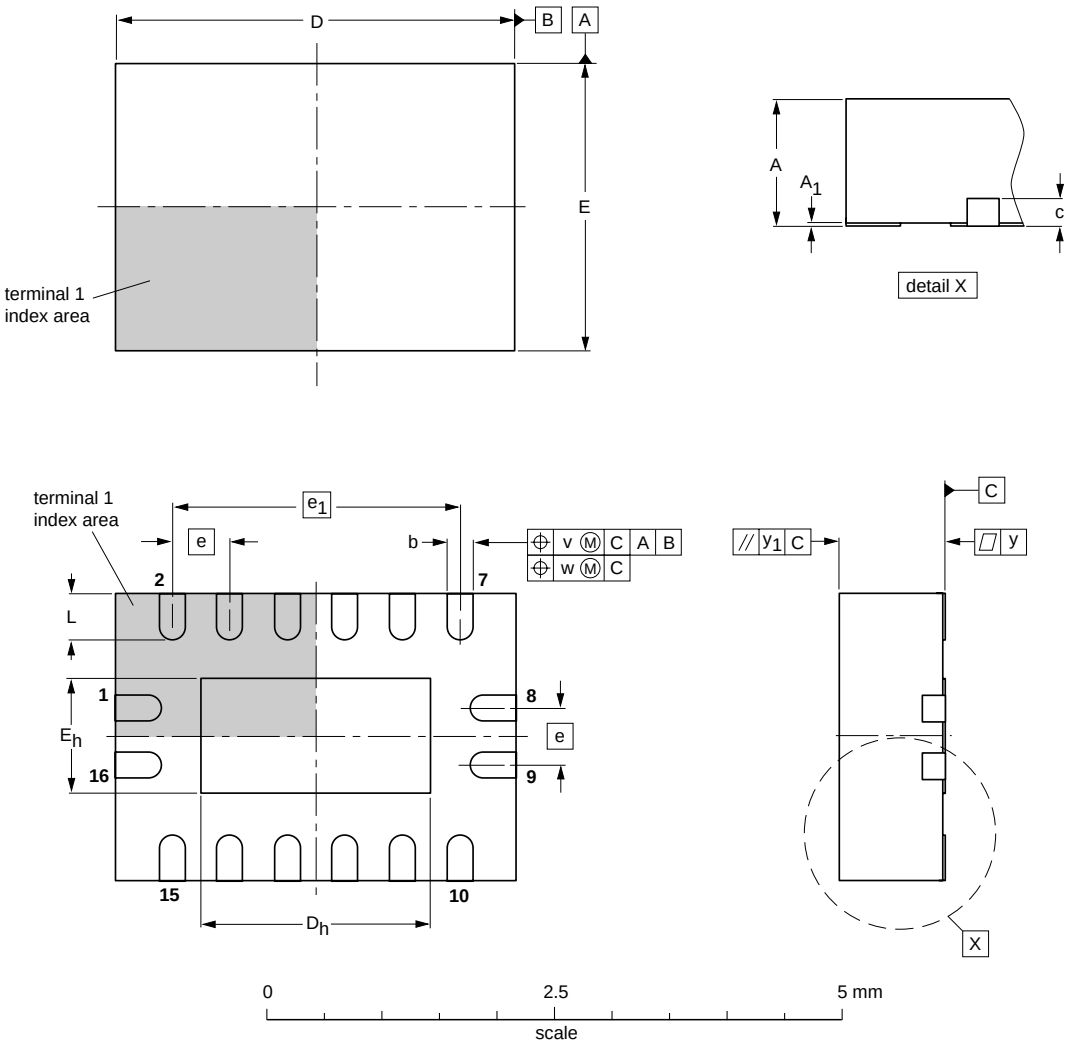
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 16. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC594A_1	20070524	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

18. Contents

1 General description 1
2 Features 1
3 Applications 1
4 Ordering information 2
5 Functional diagram 2
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 5
8 Limiting values 5
9 Recommended operating conditions 6
10 Static characteristics 6
11 Dynamic characteristics 7
12 Waveforms 10
13 Package outline 14
14 Abbreviations 17
15 Revision history 17
16 Legal information 18
16.1 Data sheet status 18
16.2 Definitions 18
16.3 Disclaimers 18
16.4 Trademarks 18
17 Contact information 18
18 Contents 19

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 May 2007
Document identifier: 74LVC594A_1