# AOT7N60/AOTF7N60

## 600V,7A N-Channel MOSFET

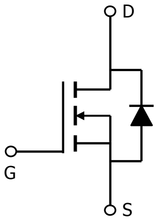
## General Description

The AOT7N60 & AOTF7N60 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.

By providing low $R_{DS(on)}$, $C_{iss}$ and $C_{rss}$ along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

## Features

| | |
|---|---|
| $V_{DS}$ | 700V@150℃ |
| $I_D$ (at $V_{GS}$=10V) | 7A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | < 1.2Ω |



**Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted**

| Parameter | | Symbol | AOT7N60 | AOTF7N60 | Units |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 600 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | | V |
| Continuous Drain Current | $T_C$=25℃ | $I_D$ | 7 | 7* | A |
| | $T_C$=100℃ | | 4.8 | 4.8* | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 28 | | |
| Avalanche Current [C] | | $I_{AR}$ | 3 | | A |
| Repetitive avalanche energy [C] | | $E_{AR}$ | 135 | | mJ |
| Single plused avalanche energy [G] | | $E_{AS}$ | 270 | | mJ |
| Peak diode recovery dv/dt | | dv/dt | 5 | | V/ns |
| Power Dissipation [B] | $T_C$=25℃ | $P_D$ | 192 | 38.5 | W |
| | Derate above 25$^{o}$C | | 1.54 | 0.3 | W/ $^{o}$C |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | | ℃ |
| Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds | | $T_L$ | 300 | | ℃ |

**Thermal Characteristics**

| Parameter | Symbol | AOT7N60 | AOTF7N60 | Units |
|---|---|---|---|---|
| Maximum Junction-to-Ambient [A,D] | $R_{\theta JA}$ | 65 | 65 | ℃/W |
| Maximum Case-to-sink [A] | $R_{\theta CS}$ | 0.5 | -- | ℃/W |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 0.65 | 3.25 | ℃/W |

* Drain current limited by maximum junction temperature.

**Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V, $T_J$=25℃ | 600 | | | V |
| | | $I_D$=250µA, $V_{GS}$=0V, $T_J$=150℃ | | 700 | | |
| $BV_{DSS}$ /ΔTJ | Zero Gate Voltage Drain Current | ID=250µA, VGS=0V | | 0.72 | | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=600V, $V_{GS}$=0V | | | 1 | µA |
| | | $V_{DS}$=480V, $T_J$=125℃ | | | 10 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±30V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=5V $I_D$=250µA | 3 | 3.9 | 4.5 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=3.5A | | 1 | 1.2 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=40V, $I_D$=3.5A | | 12 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.74 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 7 | A |
| $I_{SM}$ | Maximum Body-Diode Pulsed Current | | | | 28 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | 685 | 861 | 1035 | pF |
| $C_{oss}$ | Output Capacitance | | 65 | 84 | 100 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 5.2 | 6.6 | 7.9 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 3 | 4.1 | 6.2 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=480V, $I_D$=7A | 19.3 | 23 | 28 | nC |
| $Q_{gs}$ | Gate Source Charge | | 3.8 | 5 | 5.5 | nC |
| $Q_{gd}$ | Gate Drain Charge | | 9.3 | 11.2 | 13.5 | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=300V, $I_D$=7A, $R_G$=25Ω | | 25 | | ns |
| $t_r$ | Turn-On Rise Time | | | 49.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 51.5 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 43.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=7A,dI/dt=100A/µs,$V_{DS}$=100V | 212 | 255 | 306 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=7A,dI/dt=100A/µs,$V_{DS}$=100V | 2.0 | 2.6 | 3.1 | µC |

A. The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A$=25℃.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃, Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

G. L=60mH, $I_{AS}$=3A, $V_{DD}$=150V, $R_G$=25Ω, Starting $T_J$=25℃

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

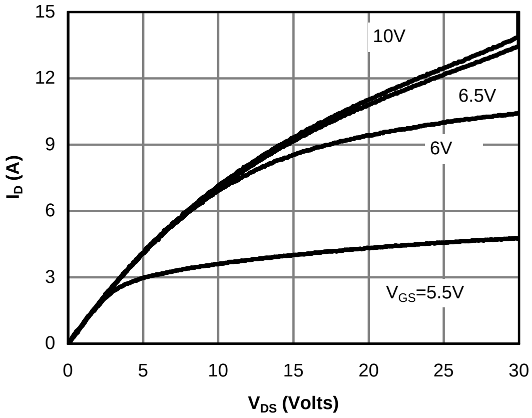


Fig 1: On-Region Characteristics

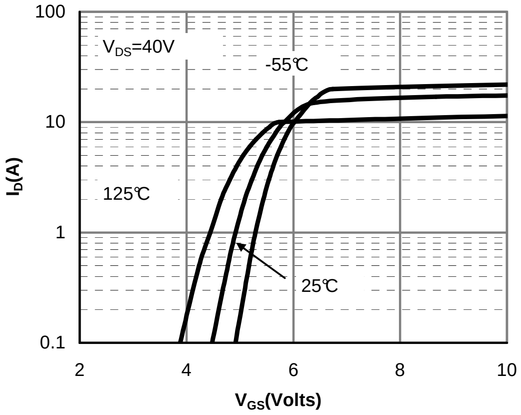


Figure 2: Transfer Characteristics

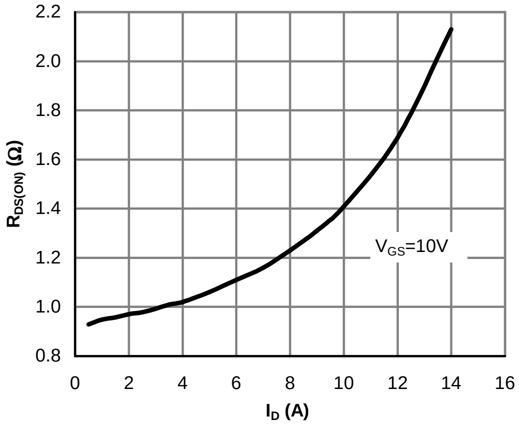


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

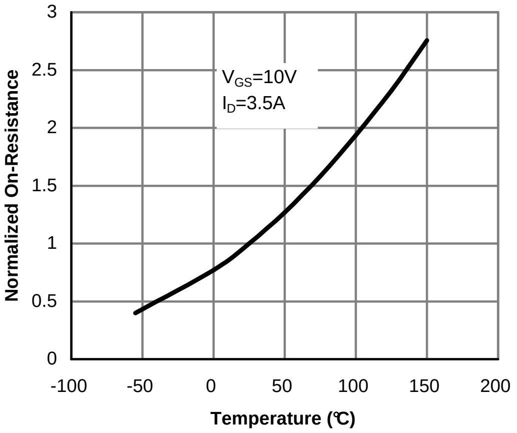


Figure 4: On-Resistance vs. Junction Temperature

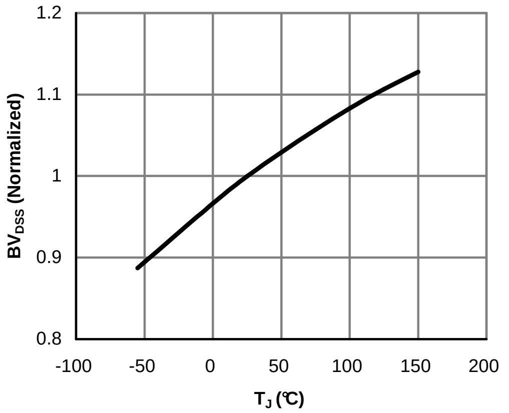


Figure 5:Break Down vs. Junction Temparature

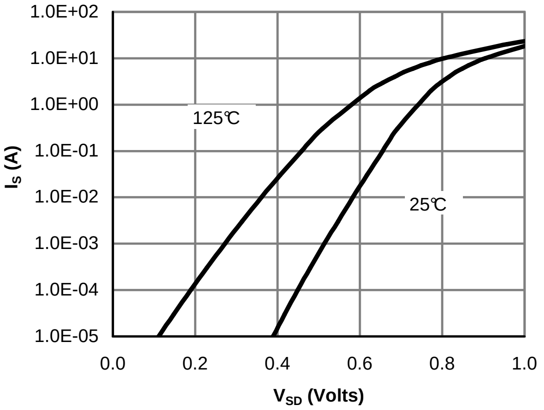


Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

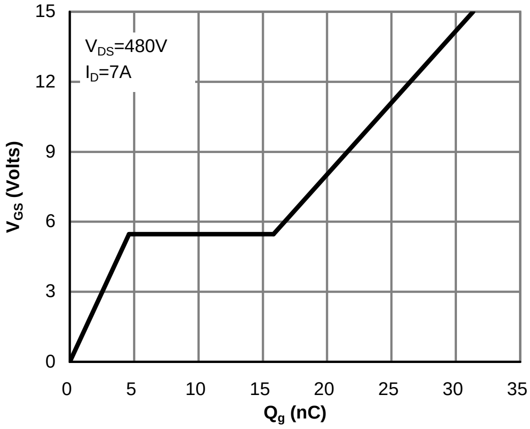


Figure 7: Gate-Charge Characteristics

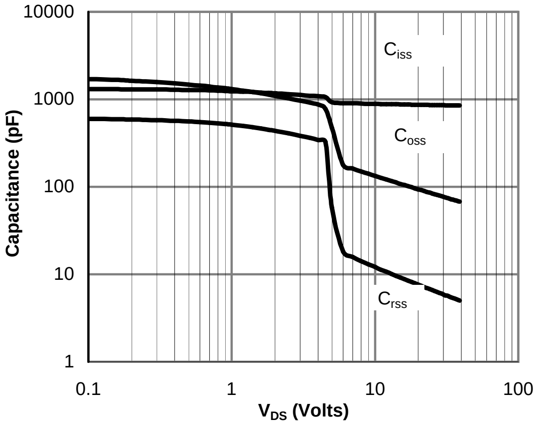


Figure 8: Capacitance Characteristics

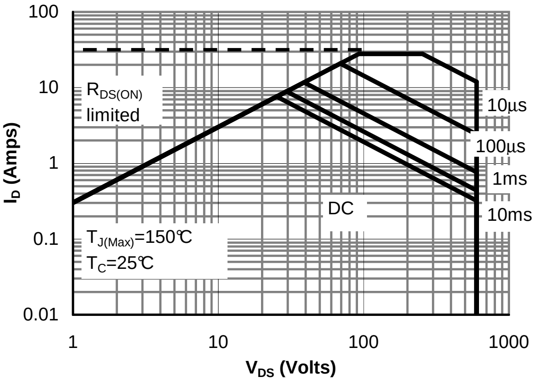


Figure 9: Maximum Forward Biased Safe Operating Area for AOT7N60 (Note F)

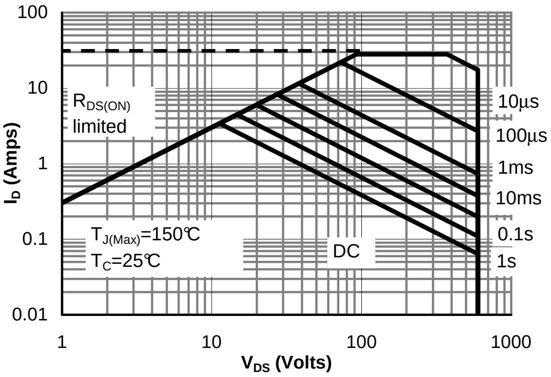


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF7N60 (Note F)

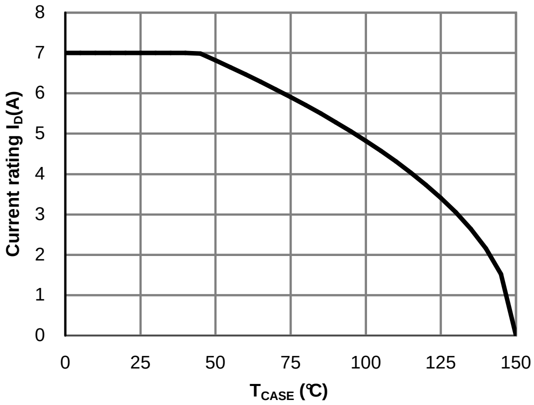


Figure 11: Current De-rating (Note B)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

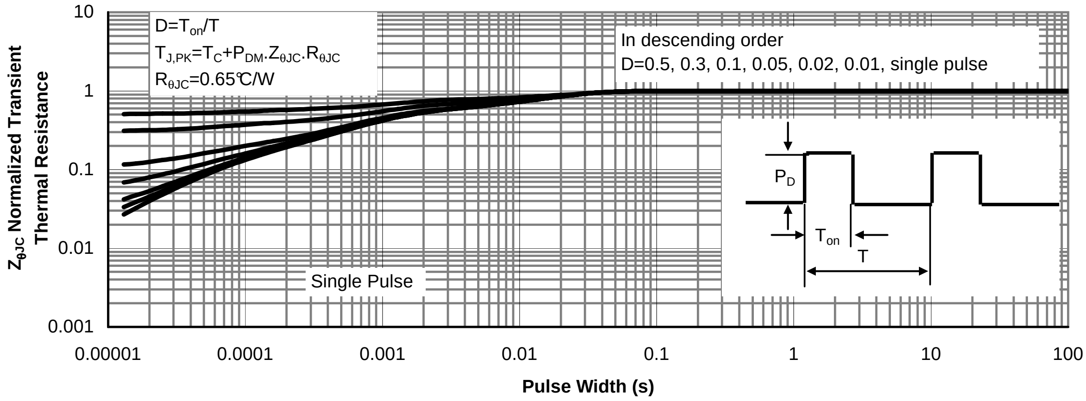


**Figure 12: Normalized Maximum Transient Thermal Impedance for AOT7N60 (Note F)**

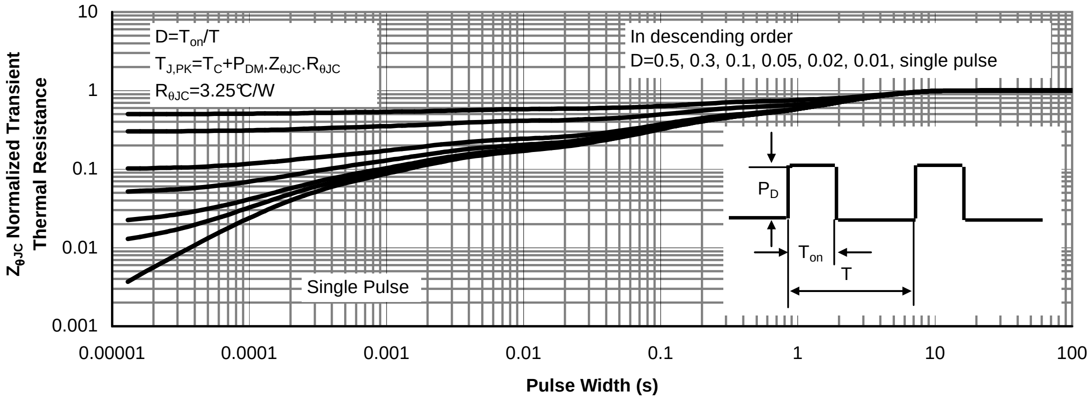
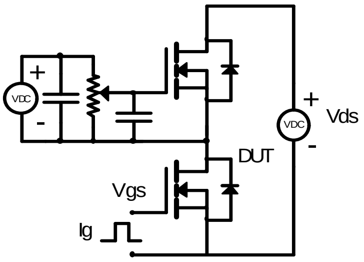
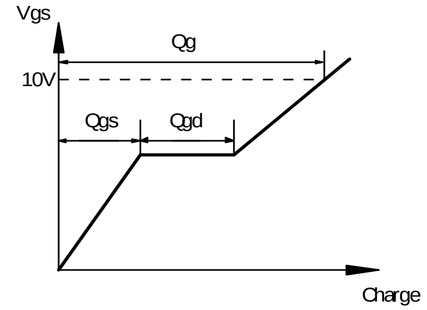


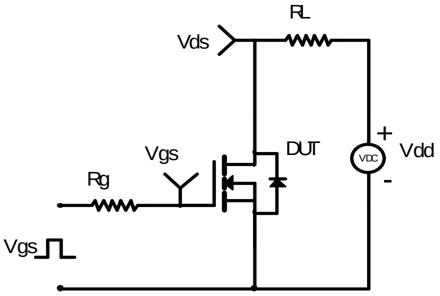
**Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF7N60 (Note F)**

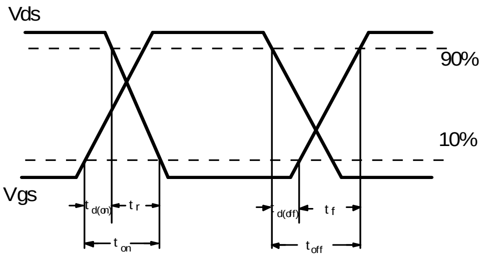
### Gate Charge Test Circuit & Waveform


VDC
+
-
Vds
VDC
+
-
DUT
Vgs
Ig

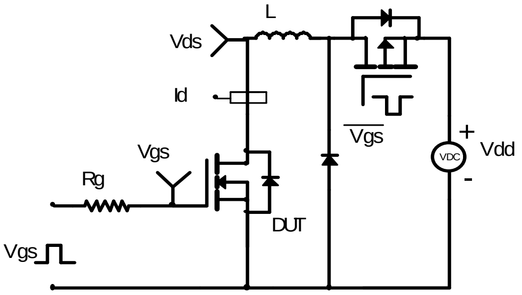

Vgs
Qg
10V
Qgs
Qgd
Charge

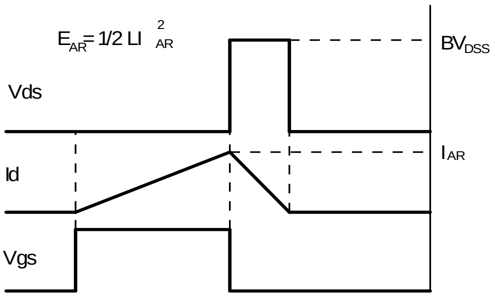
### Resistive Switching Test Circuit & Waveforms


RL
Vds
Vgs
DUT
Rg
+
VDC
Vdd
-
Vgs

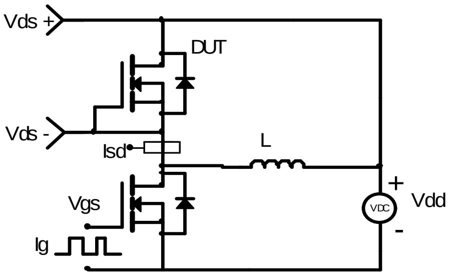

Vds
90%
10%
Vgs
t d(on)
t r
t on
t d(off)
t f
t off

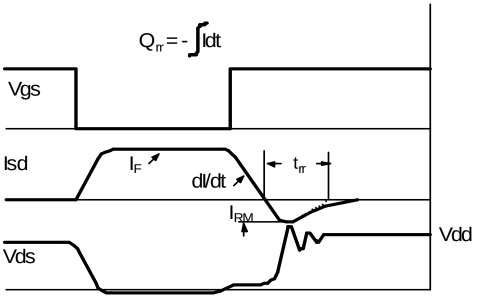
### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms


L
Vds
Id
Vgs
Vgs
Rg
+
VDC
Vdd
-
DUT
Vgs


E_AR = 1/2 LI²_AR
BV_DSS
Vds
Id
I_AR
Vgs

### Diode Recovery Test Circuit & Waveforms


Vds +
DUT
Vds -
Isd
L
+
VDC
Vdd
-
Vgs
Ig


Q_rr = - ∫Idt
Vgs
Isd
I_F
dI/dt
t_rr
I_RM
Vds
Vdd