T-52-31

# Recent Additions
# CD54AC653/3A
# CD54ACT653/3A

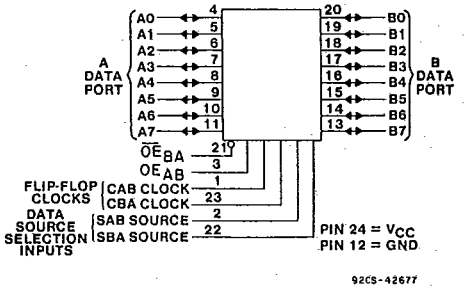
## Octal-Bus Transceiver/Register, Open-Drain (A Side), 3-State (B Side)

Inverting

The RCA CD54AC653 and CD54ACT653 are octal-bus transceivers/registers that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC653 and CD54ACT653 are inverting types having open drains on the A outputs and 3-state outputs on the B side. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables $OE_{AB}$ and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling $OE_{AB}$ and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54AC653 and CD54ACT653 are supplied in 24-lead dual-in-line ceramic packages (F suffix).




FUNCTIONAL DIAGRAM

### Package Specifications

(See Section 11, Fig. 13)

## Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | |
| Quiescent Supply Current (MSI) $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8• | — | 160• | μA |

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

**ACT INPUT LOADING TABLE**

| INPUT | UNIT LOAD* |
|---|---|
| CAB, CBA | 1.25 |
| SAB, SBA | 1.2 |
| $OE_{AB}$ | 0.67 |
| $\overline{OE}_{BA}$ | 1.17 |
| An, Bn | 0.4 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | -55 to +125°C MIN. | -55 to +125°C MAX. | UNITS |
|---|---|---|---|---|---|
| Propagation Delays: Stored A Data to $\overline{B}$ Bus | $t_{PLH}$ $t_{PHL}$ | 1.5<br>3.3*<br>5† | —<br>4<br>2.7 | 194<br>21.7<br>15.5 | ns |
| Stored $\overline{B}$ Data to A Bus | $t_{PZL}$ | 1.5<br>3.3<br>5 | —<br>4<br>2.7 | 194<br>23.3<br>15.5 | ns |
| | $t_{PLZ}$ | 1.5<br>3.3<br>5 | —<br>4.7<br>3.2 | 232<br>23.1<br>18.5 | ns |
| A Data to $\overline{B}$ Bus | $t_{PLH}$ $t_{PHL}$ | 1.5<br>3.3<br>5 | —<br>3.7<br>2.4 | 178<br>19.9<br>14.2 | ns |
| $\overline{B}$ Data to A Bus | $t_{PZL}$ | 1.5<br>3.3<br>5 | —<br>3.7<br>2.4 | 178<br>21.3<br>14.2 | ns |
| | $t_{PLZ}$ | 1.5<br>3.3<br>5 | —<br>4.4<br>3 | 215<br>21.5<br>17.2 | ns |
| Select to Data (B Bus) | $t_{PLH}$ $t_{PHL}$ | 1.5<br>3.3<br>5 | —<br>4<br>2.7 | 194<br>21.7<br>15.5 | ns |
| Select to Data (A Bus) | $t_{PZL}$ | 1.5<br>3.3<br>5 | —<br>4<br>2.7 | 194<br>23.3<br>15.5 | ns |
| | $t_{PLZ}$ | 1.5<br>3.3<br>5 | —<br>4.7<br>3.2 | 232<br>23.1<br>18.5 | ns |
| 3-State Enabling/Disabling Time (B Bus) Bus to Output or Register to Output | $t_{PZL}$ $t_{PZH}$ $t_{PLZ}$ $t_{PHZ}$ | 1.5<br>3.3<br>5 | —<br>4<br>2.7 | 194<br>23.3<br>15.5 | ns |
| Off-State Enabling/Disabling Time (A Bus) Bus to Output or Register to Output | $t_{PZL}$ $t_{PLZ}$ | 1.5<br>3.3<br>5 | —<br>4<br>2.7 | 194<br>23.3<br>15.5 | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | | | pF |
| Min. (Valley) $V_{OH}$ (B Side) During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ | 5 | 4 Typ. @ 25°C | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ | 5 | 1 Typ. @ 25°C | | V |
| Input Capacitance | $C_I$ | — | — | 10 | pF |
| 3-State Output Capacitance (B Side) | $C_O$ | — | — | 15 | pF |
| Off-State Output Capacitance (A Side) | $C_O$ | — | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V
min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§$C_{PD}$ is used to determine the dynamic power consumption, per package.
For AC, $P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_L f_o)$ where $f_i$ = input frequency
$f_o$ = output frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage

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# Recent Additions
# CD54AC653/3A
# CD54ACT653/3A

**SWITCHING CHARACTERISTICS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | -55 to +125°C | | UNITS |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Propagation Delays: Store A Data to $\overline{B}$ Bus | $t_{PLH}$ $t_{PHL}$ | 5† | 2.7 | 15.5 | ns |
| Store $\overline{B}$ Data to A Bus | $t_{PZL}$ | 5 | 2.7 | 15.5 | ns |
| | $t_{PLZ}$ | 5 | 3.2 | 18.5 | ns |
| A Data to $\overline{B}$ Bus | $t_{PLH}$ $t_{PHL}$ | 5 | 2.4 | 14.2 | ns |
| $\overline{B}$ Data to A Bus | $t_{PZL}$ | 5 | 2.4 | 14.2 | ns |
| | $t_{PLZ}$ | 5 | 3 | 17.2 | ns |
| Select to Data (B Bus) | $t_{PLH}$ $t_{PHL}$ | 5 | 2.7 | 15.5 | ns |
| Select to Data (A Bus) | $t_{PZL}$ | 5 | 2.7 | 15.5 | ns |
| | $t_{PLZ}$ | 5 | 3.2 | 18.5 | ns |
| 3-State Enabling/Disabling Time (B Bus) Bus to Output or Register to Output | $t_{PZL}$ $t_{PZH}$ $t_{PLZ}$ $t_{PHZ}$ | 5 | 2.7 | 15.5 | ns |
| Off-State Enabling/Disabling Time (A Bus) Bus to Output or Register to Output | $t_{PZL}$ $t_{PLZ}$ | 5 | 2.7 | 15.5 | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | | | pF |
| Min. (Valley) $V_{OH}$ (B Side) During Switching of Outher Outputs (Output Under Test Not Switching) | $V_{OHV}$ | 5 | 4 Typ. @ 25° C | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ | 5 | 1 Typ. @ 25°C | | V |
| Input Capacitance | $C_I$ | — | — | 10 | pF |
| 3-State Output Capacitance (B Side) | $C_O$ | — | — | 15 | pF |
| Off-State Output Capacitance (A Side) | $C_O$ | — | — | 15 | pF |

†5 V: min. is @ 5.5 V
max. is @ 4.5 V
min. is @ 5.25 V for 0 to +70°C
max. is @ 4.75 V for 0 to +70°C

§$C_{PD}$ is used to determine the dynamic power consumption, per package.
For ACT, $P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where $f_i$ = input frequency
$f_o$ = output frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage