Precision 8-Ch/Dual 4-Ch Low Voltage Analog Multiplexers

DESCRIPTION

The DG9408, DG9409 uses BiCMOS wafer fabrication technology that allows the DG9408, DG9409 to operate on single and dual supplies. Single supply voltage ranges from 3 V to 12 V while dual supply operation is recommended with ± 3 V to ± 6 V.

The DG9408 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG9409 is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. The DG9408, DG9409 are offered in a QFN package that has a nickel-palladium-gold device terminations and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all the JEDEC standards for reflow and MSL ratings.

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- 2.7 V to 12 V single supply or ± 3 V to ± 6 V dual supply operation
- Low on-resistance - R_{ON}: 3.9 Ω typ.
- Fast switching: t_{ON} - 42 ns, t_{OFF} - 24 ns
- Break-before-make guaranteed
- Low leakage
- TTL, CMOS, LV logic (3 V) compatible
- 2000 V ESD protection (HBM)
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

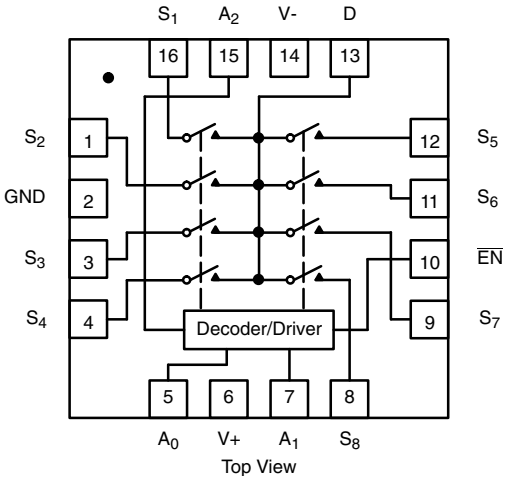
- High accuracy
- Single and dual power rail capacity
- Wide operating voltage range
- Simple logic interface

APPLICATIONS

- Data acquisition systems
- Battery operated equipment
- Portable test equipment
- Sample and hold circuits
- Communication systems
- SDSL, DSLAM
- Audio and video signal routing

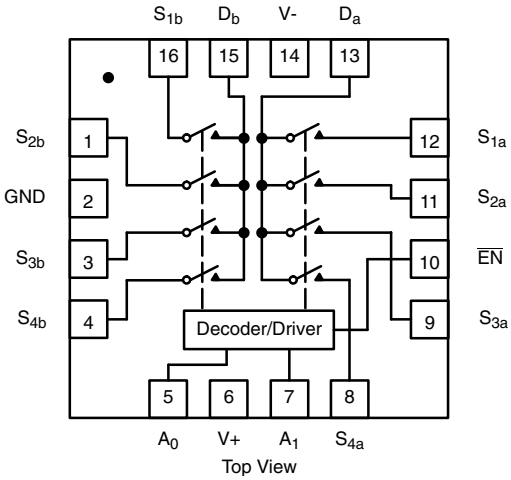
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9408
QFN16



Top View

DG9409
QFN16



Top View

TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE DG9408				
A_2	A_1	A_0	$\overline{EN}$	On Switch
X	X	X	1	None
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

TRUTH TABLE DG9409			
A_1	A_0	$\overline{EN}$	On Switch
X	X	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

X = Don't care

For low and high voltage levels for V_{AX} and V_{EN} consult "Digital Control" Parameters for Specific V+ operation. See Specifications Tables for:

Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin QFN (4 mm x 4 mm)	DG9408DN-T1-E4
		DG9409DN-T1-E4

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		Limit	Unit
Voltage Referenced V+ to V-		14	V
GND		7	
Digital Inputs[a], V_S, V_D		(V-) - 0.3 to (V+) + 0.3	
Current (Any Terminal Except S or D)		30	mA
Continuous Current, S or D		100	
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle max.)		200	
Package Solder Reflow Conditions[d]	16-pin (4 x 4 mm) QFN	240	°C
Storage Temperature		- 65 to 150	
Power Dissipation (Package)[b], (T_A = 70 °C)	16-pin (4 x 4 mm) QFN[c]	1880	mW

Notes:
a. Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 23.5 mW/°C above 70 °C.
d. Manual soldering with soldering iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (Single Supply 12 V)								
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 12 V, ± 10 %, V- = 0 V V_A, $V_{\overline{EN}}$ = 0.8 V or 2.4 V[f]		**Temp.[b]**	**Limits** - 40 °C to 85 °C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch								
Analog Signal Range[e]	V_{ANALOG}			Full	0		12	V
On-Resistance	R_{ON}	V+ = 10.8 V, V_D = 2 V or 9 V, I_S = 50 mA sequence each switch on		Room Full		4	7 7.5	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V+ = 10.8 V, V_D = 2 V or 9 V, I_S = 50 mA		Room			3.6	
On-Resistance Flatness[i]	R_{ON} Flatness			Room			8	
Switch Off Leakage Current	$I_{S(off)}$	$V_{\overline{EN}}$ = 2.4 V, V_D = 11 V or 1 V, V_S = 1 V or 11 V		Room Full	- 2 - 15		2 15	nA
	$I_{D(off)}$			Room Full	- 2 - 15		2 15	
Channel On Leakage Current	$I_{D(on)}$	$V_{\overline{EN}}$ = 0 V, V_S = V_D = 1 V or 11 V		Room Full	- 2 - 15		2 15	
Digital Control								
Logic High Input Voltage	V_{INH}			Full	2.4			V
Logic Low Input Voltage	V_{INL}			Full			0.8	
Input Current	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2.4 V or 0.8 V		Full	- 1		1	µA
Dynamic Characteristics								
Transition Time	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, (DG9408) V_{S1b} = 8 V, V_{S4b} = 0 V, (DG9409) see fig. 2		Room Full		42	71 75	ns
Break-Before-Make Time	t_{BBM}	$V_{S(all)}$ = V_{DA} = 5 V see fig. 4		Room Full	2	24		
Enable Turn-On Time	$t_{ON(\overline{EN})}$	V_{AX} = 0 V, V_{S1} = 5 V (DG9408) V_{AX} = 0 V, V_{S1b} = 5 V (DG9409) see fig. 3		Room Full		42	70 75	
Enable Turn-Off Time	$t_{OFF(\overline{EN})}$			Room Full		24	44 46	
Charge Injection[e]	Q	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		Room		29		pC
Off Isolation[e, h]	OIRR	f = 100 kHz, R_L = 1 kΩ		Room		- 80		dB
Crosstalk[e]	X_{TALK}			Room		- 85		
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 2.4 V	DG9408	Room		21		pF
			DG9409	Room		23		
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2.4 V	DG9408	Room		211		
			DG9409	Room		112		
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	DG9408	Room		238		
			DG9409	Room		137		
Power Supplies								
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V+		Room			1	µA

SPECIFICATIONS (Dual Supply V+ = 5 V, V- = - 5 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, V- = - 5 V, ± 10 % V_A, $V_{\overline{EN}}$ = 0.8 V or 2 V[f]	**Temp.[b]**	**Limits** - 40 °C to 85 °C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	- 5		5	V
On-Resistance	R_{ON}	V+ = 4.5 V, V- = - 4.5 V, V_D = ± 3.5 V, I_S = 50 mA sequence each switch on	Room Full		5	8 8.5	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V+ = 4.5 V, V- = - 4.5 V, V_D = ± 3.5 V, I_S = 50 mA	Room			3.6	Ω
On-Resistance Flatness[i]	R_{ON} Flatness		Room			8.2	Ω
Switch Off Leakage Current[a]	$I_{S(off)}$	V+ = 5.5 , V- = - 5.5 V $V_{\overline{EN}}$ = 2.4 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room Full	- 2 - 15		2 15	nA
	$I_{D(off)}$		Room Full	- 2 - 15		2 15	nA
Channel On Leakage Current[a]	$I_{D(on)}$	V+ = 5.5 V, V- = - 5.5 V $V_{\overline{EN}}$ = 0 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room Full	- 2 - 15		2 15	nA
Digital Control							
Logic High Input Voltage	V_{INH}		Full	2			V
Logic Low Input Voltage	V_{INL}		Full			0.8	V
Input Current[a]	I_{IN}	V_{AX} = V_{EN} = 2 V or 0.8 V	Full	- 1		1	µA
Dynamic Characteristics							
Transition Time[e]	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = - 3.5 V, (DG9408) V_{S1b} = 3.5 V, V_{S4b} = - 3.5 V, (DG9409) see fig. 2	Room Full		68	89 94	ns
Break-Before-Make Time[e]	t_{BBM}	$V_{S(all)}$ = V_{DA} = 3.5 V see fig. 4	Room Full	1	16		ns
Enable Turn-On Time[e]	$t_{ON(\overline{EN})}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG9408) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG9409) see fig. 3	Room Full		68	88 94	ns
Enable Turn-Off Time[e]	$t_{OFF(\overline{EN})}$		Room Full		58	78 81	ns
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 2 V — DG9408	Room		23		pF
		DG9409	Room		23		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2 V — DG9408	Room		223		pF
		DG9409	Room		113		pF
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V — DG9408	Room		246		pF
		DG9409	Room		137		pF
Power Supplies							
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V+	Room			1	µA
	I-		Room	- 1			µA

SPECIFICATIONS (Single Supply 5 V)								
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, ± 10 %, V- = 0 V V_A, $V_{\overline{EN}}$ = 0.8 V or 2 V[f]		**Temp.[b]**	**Limits** - 40 °C to 85 °C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch								
Analog Signal Range[e]	V_{ANALOG}			Full	0		5	V
On-Resistance	R_{ON}	V+ = 4.5 V, V_D or V_S = 1 V or 3.5 V, I_S = 50 mA		Room Full		7	10.5 11	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V+ = 4.5 V, V_D = 1 V or 3.5 V, I_S = 50 mA		Room			3.6	Ω
On-Resistance Flatness[i]	R_{ON} Flatness			Room			9	Ω
Switch Off Leakage Current[a]	$I_{S(off)}$	V+ = 5.5 V V_S = 1 V or 4 V, V_D = 4 V or 1 V		Room Full	- 2 - 15		2 15	nA
	$I_{D(off)}$			Room Full	- 2 - 15		2 15	nA
Channel On Leakage Current[a]	$I_{D(on)}$	V+ = 5.5 V V_D = V_S = 1 V or 4 V, sequence each switch on		Room Full	- 2 - 15		2 15	nA
Digital Control								
Logic High Input Voltage	V_{INH}	V+ = 5 V		Full	2			V
Logic Low Input Voltage	V_{INL}			Full			0.8	V
Input Current[a]	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2 V or 0.8 V		Full	- 1		1	µA
Dynamic Characteristics								
Transition Time[e]	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = 0 V, (DG9408) V_{S1b} = 3.5 V, V_{S4b} = 0 V, (DG9409) see fig. 2		Room Full		73	94 104	ns
Break-Before-Make Time[e]	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 3.5 V see fig. 4		Room Full	2	29		ns
Enable Turn-On Time[e]	$t_{ON(\overline{EN})}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG9408) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG9409) see fig. 3		Room Full		74	94 104	ns
Enable Turn-Off Time[e]	$t_{OFF(\overline{EN})}$			Room Full		38	57 61	ns
Charge Injection[e]	Q	C_L = 1 nF, R_{GEN} = 0 , V_{GEN} = 0 V		Room		20		pC
Off Isolation[e, h]	OIRR	R_L = 1 kΩ, f = 100 kHz		Room		- 81		dB
Crosstalk[e]	X_{TALK}			Room		- 85		dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 0 V	DG9408	Room		22		pF
			DG9409	Room		24		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2 V	DG9408	Room		223		pF
			DG9409	Room		113		pF
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	DG9408	Room		244		pF
			DG9409	Room		143		pF
Power Supplies								
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V+		Room			1	µA

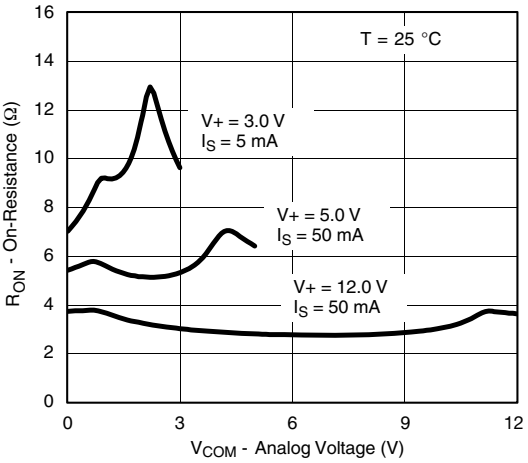
SPECIFICATIONS (Single Supply 3 V)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, ± 10 %, V- = 0 V $V_{\overline{EN}}$ = 0.4 V or 1.8 V[f]		Temp.[b]	Limits - 40 °C to 85 °C Min.[c]	Typ.[d]	Max.[c]	Unit
Analog Switch								
Analog Signal Range[e]	V_{ANALOG}			Full	0		3	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_D = 0.5 V or 2.2 V, I_S = 5 mA		Room Full		12	25.5 26.5	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V+ = 2.7 V, V_D = 0.5 V or 2.2 V, I_S = 5 mA		Room			3.6	Ω
On- Resistance Flatness[i]	R_{ON} Flatness	V+ = 2.7 V, V_D = 0.5 V or 2.2 V, I_S = 5 mA		Room			13	Ω
Switch Off Leakage Current[a]	$I_{S(off)}$	V+ = 3.3 V V_S = 2 V or 1 V, V_D = 1 or 2 V		Room Full	- 2 - 15		2 15	nA
	$I_{D(off)}$			Room Full	- 2 - 15		2 15	nA
Channel On Leakage Current[a]	$I_{D(on)}$	V+ = 3.3 V V_D = V_S = 1 V or 2 V, sequence each switch on		Room Full	- 2 - 15		2 15	nA
Digital Control								
Logic High Input Voltage	V_{INH}			Full	1.8			V
Logic Low Input Voltage	V_{INL}			Full			0.4	V
Input Current[a]	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 1.8 V or 0.4 V		Full	- 1		1	µA
Dynamic Characteristics								
Transition Time	t_{TRANS}	V_{S1} = 1.5 V, V_{S8} = 0 V, (DG9408) V_{S1b} = 1.5 V, V_{S4b} = 0 V, (DG9409) see fig. 2		Room Full		140	165 182	ns
Break-Before-Make Time	t_{BBM}	$V_{S(all)}$ = V_{DA} = 1.5 V see fig. 4		Room Full	2	63		ns
Enable Turn-On Time	$t_{ON(\overline{EN})}$	V_{AX} = 0 V, V_{S1} = 1.5 V (DG9408) V_{AX} = 0 V, V_{S1b} = 1.5 V (DG9409) see fig. 3		Room Full		140	162 178	ns
Enable Turn-Off Time	$t_{OFF(\overline{EN})}$			Room Full		76	97 104	ns
Charge Injection[e]	Q	C_L = 1 nF, R_{GEN} = 0 , V_{GEN} = 0 V		Room		7		pC
Off Isolation[e, h]	OIRR	f = 100 kHz, R_L = 1 kΩ		Room		- 81		dB
Crosstalk[e]	X_{TALK}			Room		- 85		dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 1.8 V	DG9408	Room		23		pF
			DG9409	Room		25		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 1.8 V	DG9408	Room		230		pF
			DG9409	Room		120		pF
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	DG9408	Room		256		pF
			DG9409	Room		147		pF
Power Supplies								
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V+		Room			1	µA

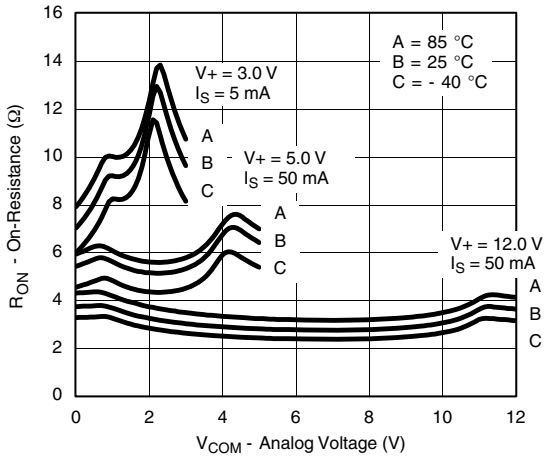
Notes:
a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. ΔR_{DON} = R_{DON} Max - R_{DON} Min.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.
i. R_{DON} flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

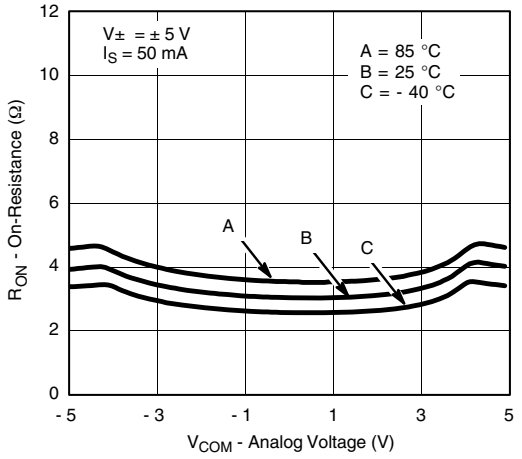
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



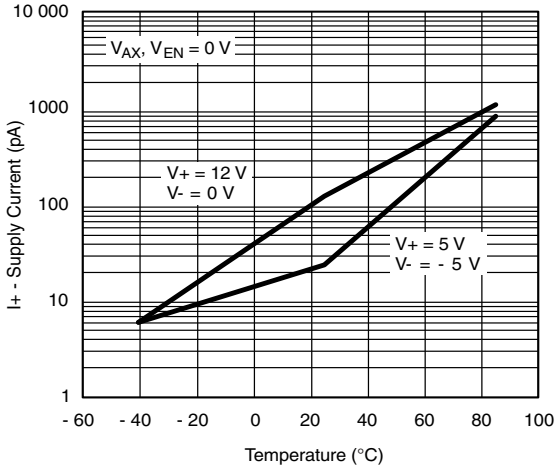
R_{ON} vs. V_{COM} and Single Supply Voltage



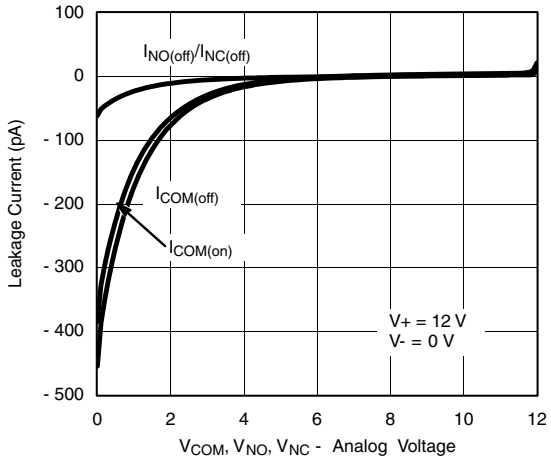
R_{ON} vs. Analog Voltage and Temperature



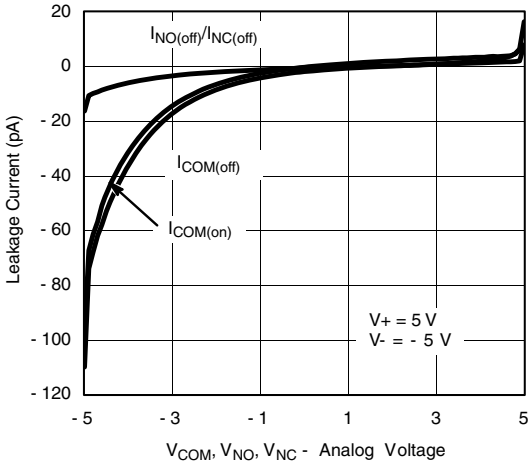
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

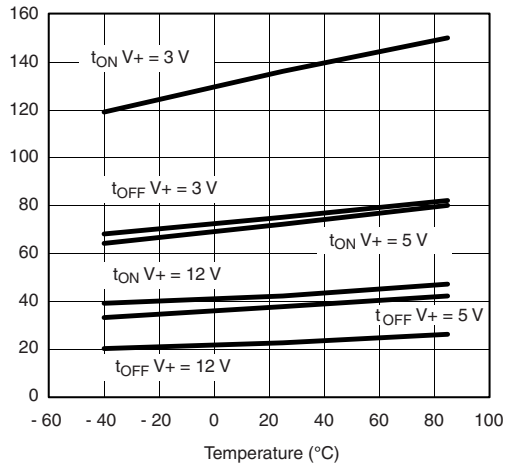


Leakage Current vs. Analog Voltage

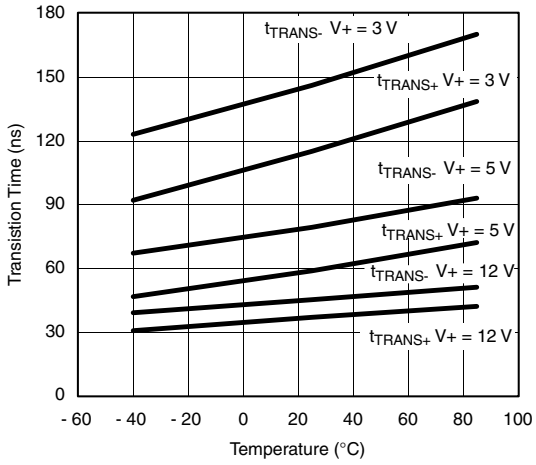


Leakage Current vs. Analog Voltage

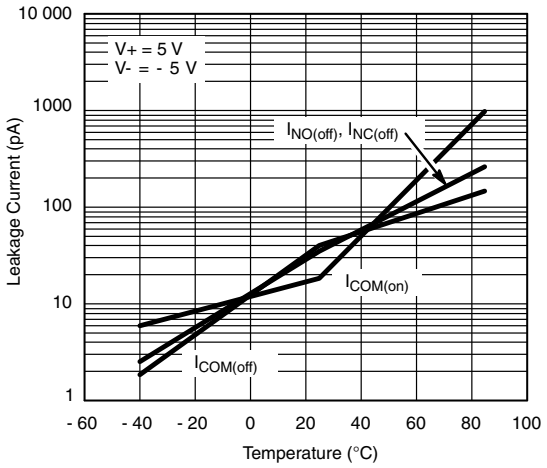
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



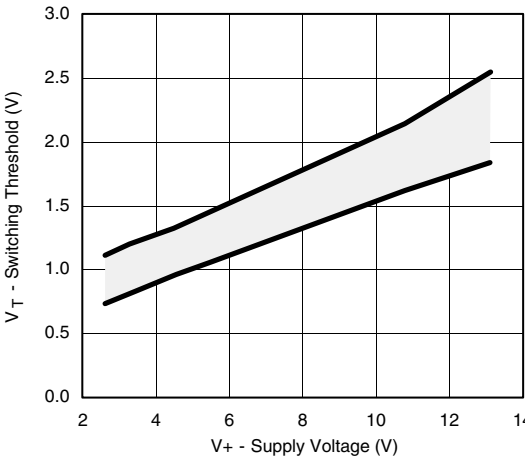
Switching Time vs. Temperature and Single Supply Voltage



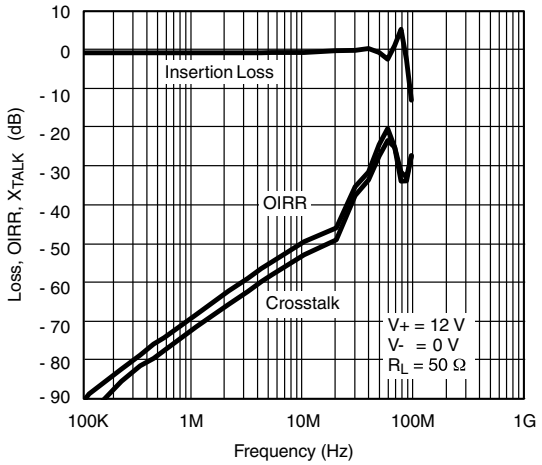
Transition Time vs. Temperature and Single Supply Voltage



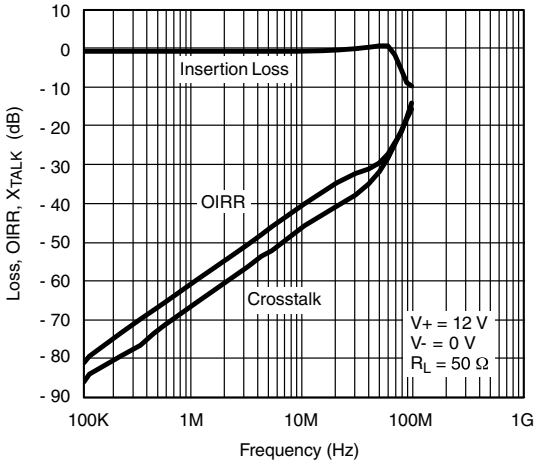
Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage

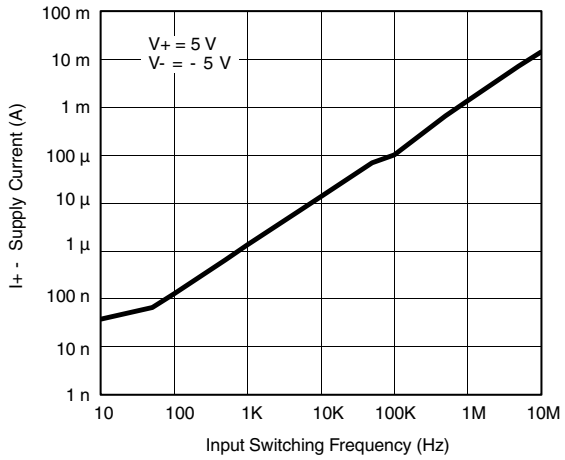


Insertion Loss, Off Isolation and Crosstalk vs. Frequency (DG9408)



Insertion Loss, Off Isolation and Crosstalk vs. Frequency (DG9409)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Supply Current vs. Input Switching Frequency

SCHEMATIC DIAGRAM (Typical Channel)

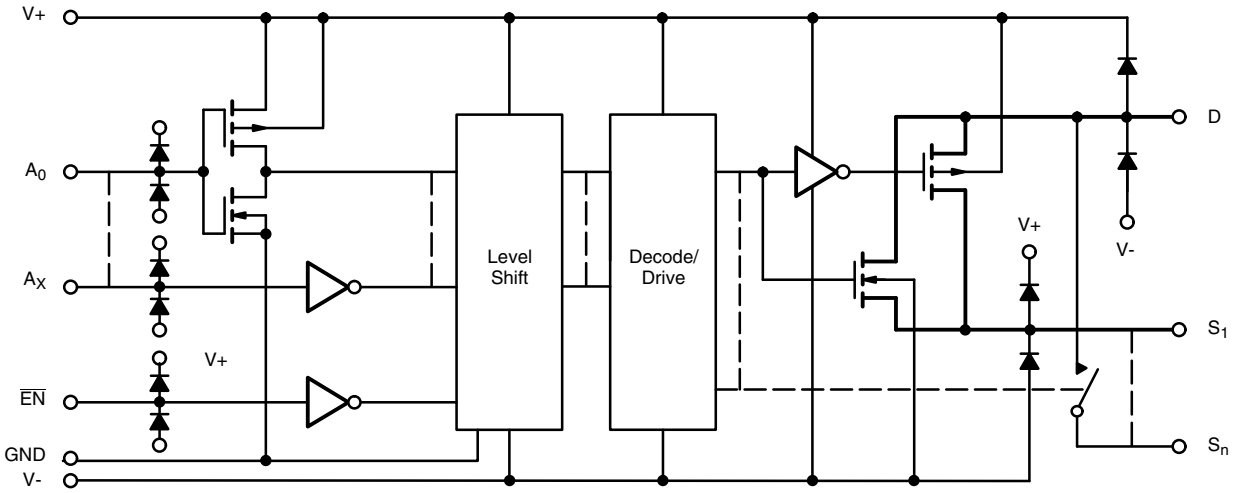
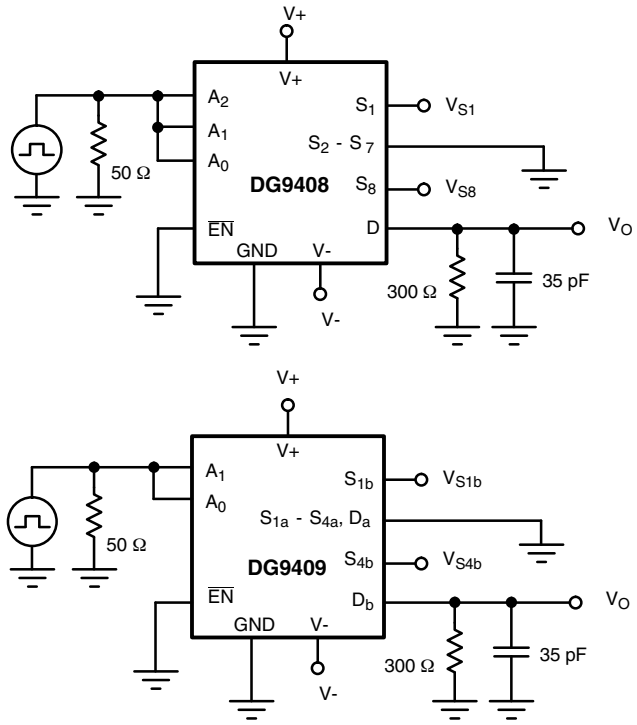
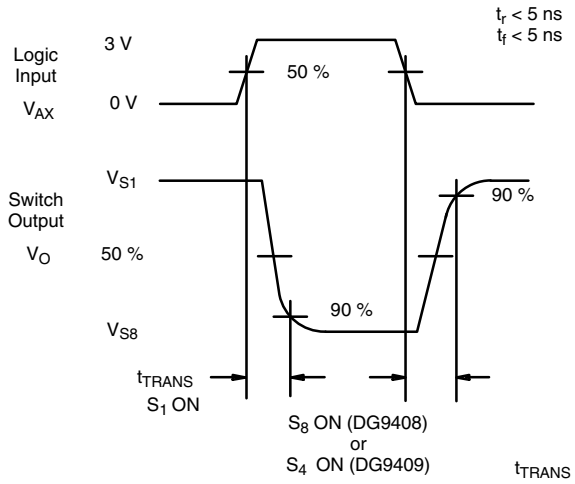


Figure 1.

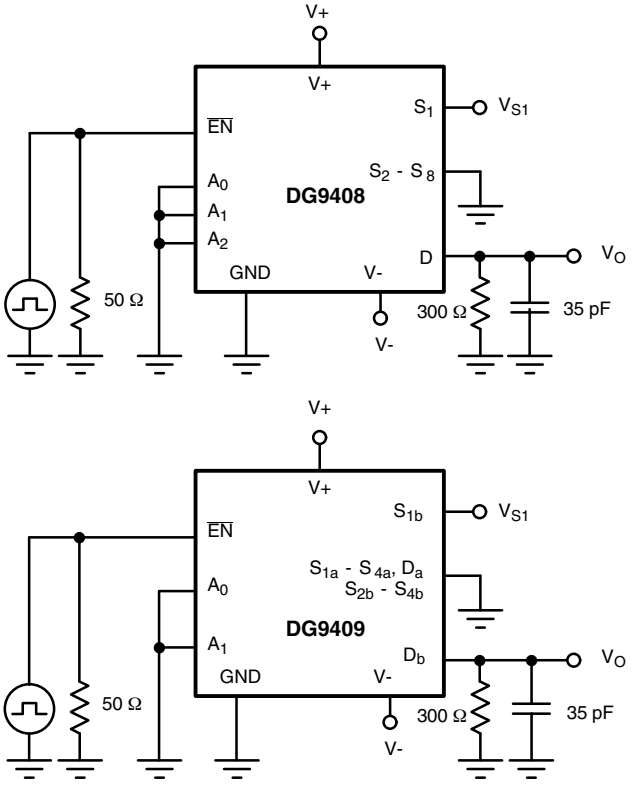
TEST CIRCUITS

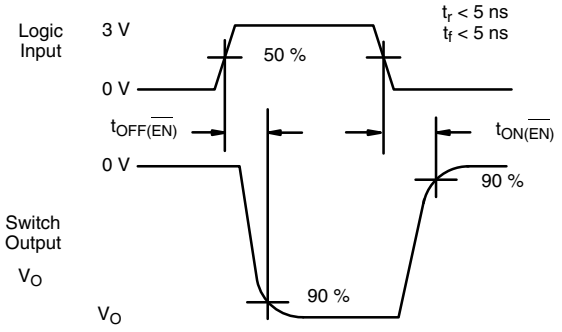




Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 2. Transition Time

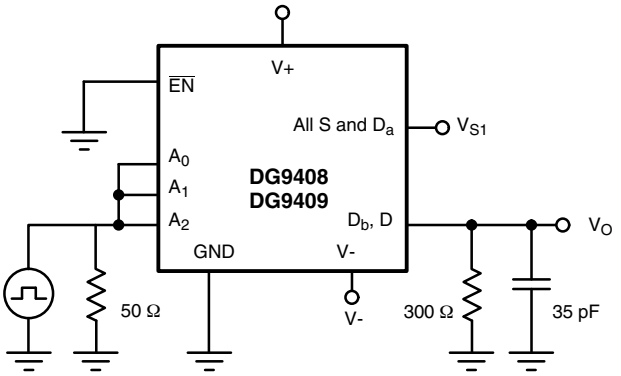


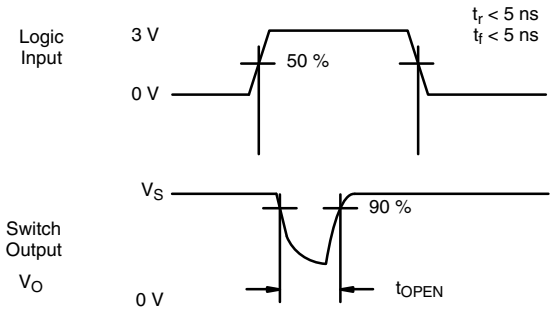


Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 3. Enable Switching Time

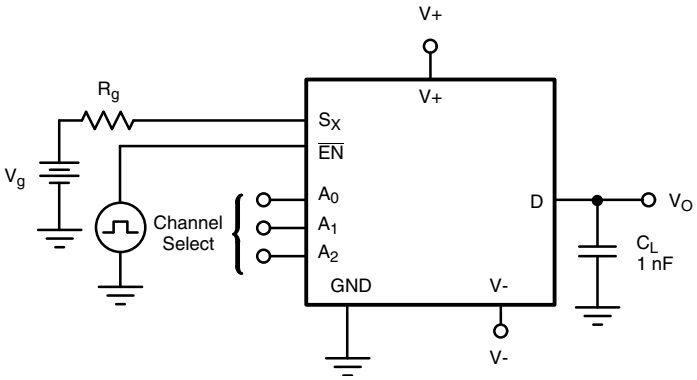
TEST CIRCUITS

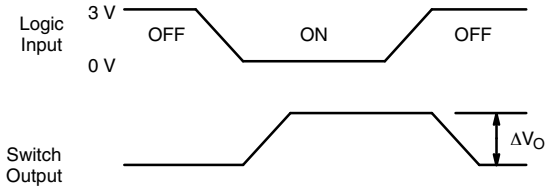




Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 4. Break-Before-Make Interval

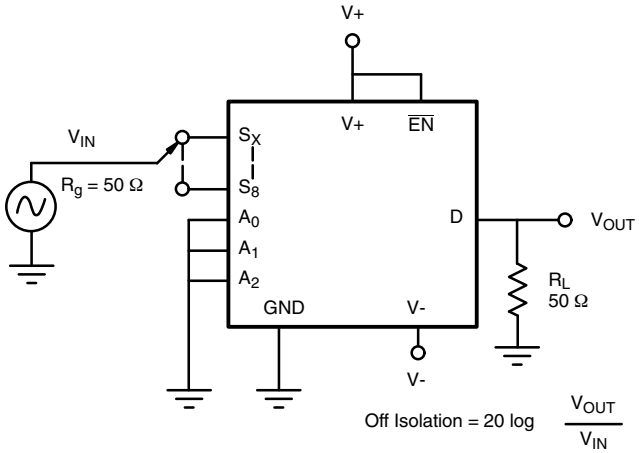




ΔVO is the measured voltage due to charge transfer error Q, when the channel turns off.

$$Q = C_L \times \Delta V_O$$

Figure 5. Charge Injection



$$\text{Off Isolation} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Figure 6. Off Isolation

TEST CIRCUITS

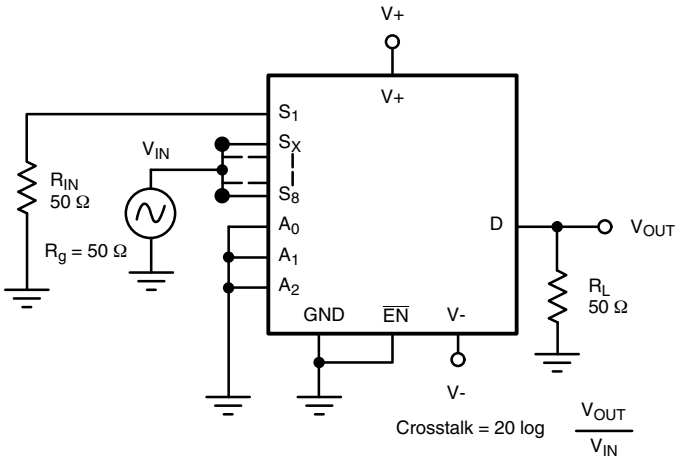


Figure 7. Crosstalk

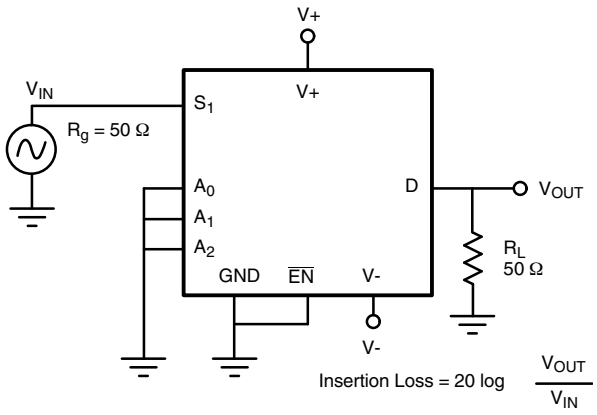


Figure 8. Insertion Loss

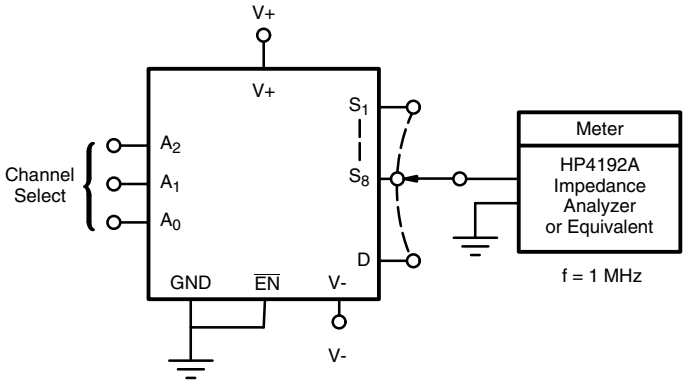
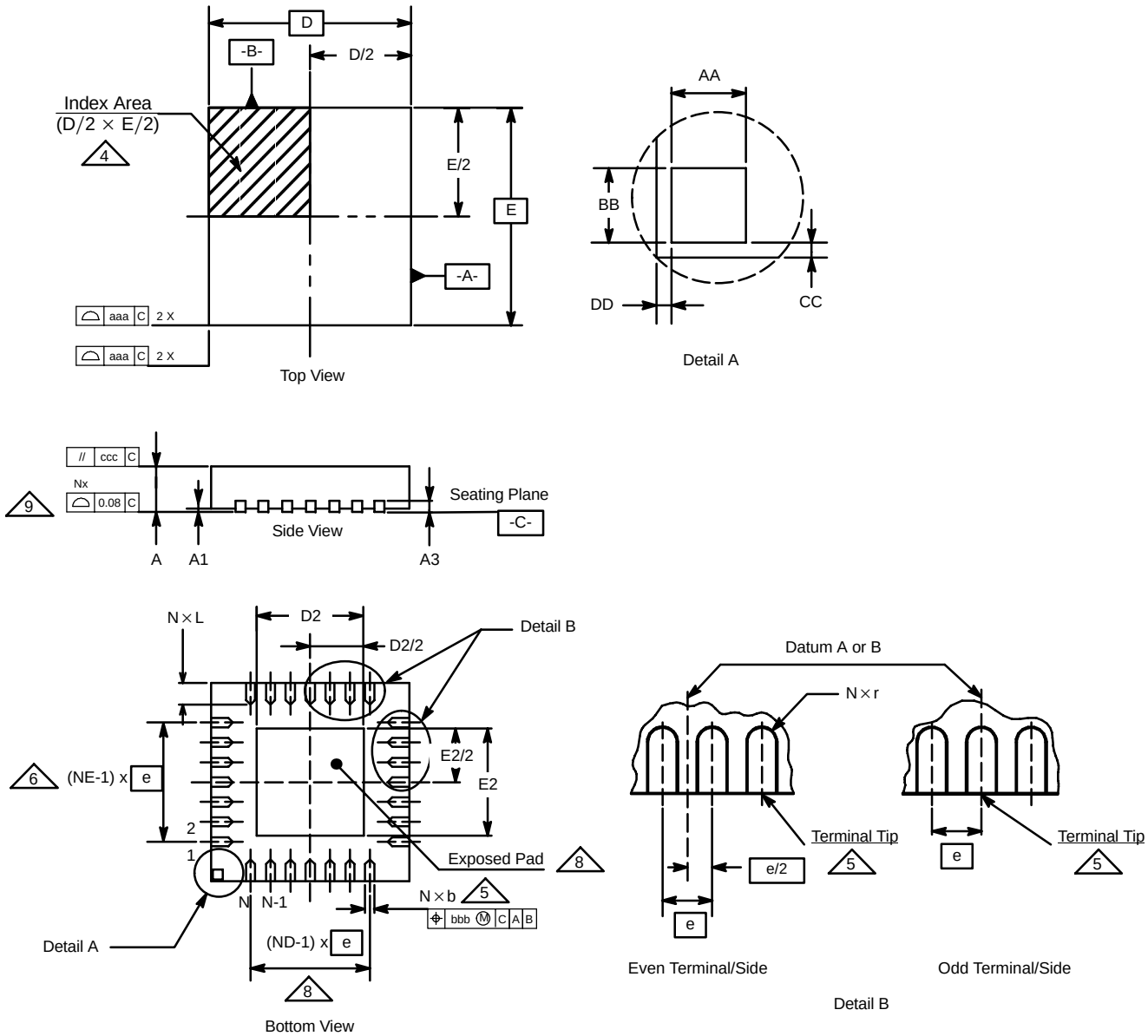


Figure 9. Source Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71870.

QFN-16 (4 × 4 mm)

JEDEC Part Number: MO-220



QFN-16 (4 × 4 mm)
JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	-	0.20 Ref	-	-	0.0079	-	
AA	-	0.345	-	-	0.0136	-	
aaa	-	0.25	-	-	0.0098	-	
BB	-	0.345	-	-	0.0136	-	
b	0.23	0.30	0.38	0.0091	0.0118	0.0150	5
bbb	-	0.10	-	-	0.0039	-	
CC	-	0.18	-	-	0.0071	-	
ccc	-	0.10	-	-	0.0039	-	
D		4.00 BSC			0.1575 BSC		
D2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
DD	-	0.18	-	-	0.0071	-	
E		4.00 BSC			0.1575 BSC		
E2	2.00	2.15	2.25	0.0787	0.0846	0.0886	
e		0.65 BSC			0.0256 BSC		
L	0.45	0.55	0.65	0.0177	0.0217	0.0256	
N		16			16		3, 7
ND	-	4	-	-	4	-	6
NE	-	4	-	-	4	-	6
r	b(min)/2	-	-	b(min)/2	-	-	

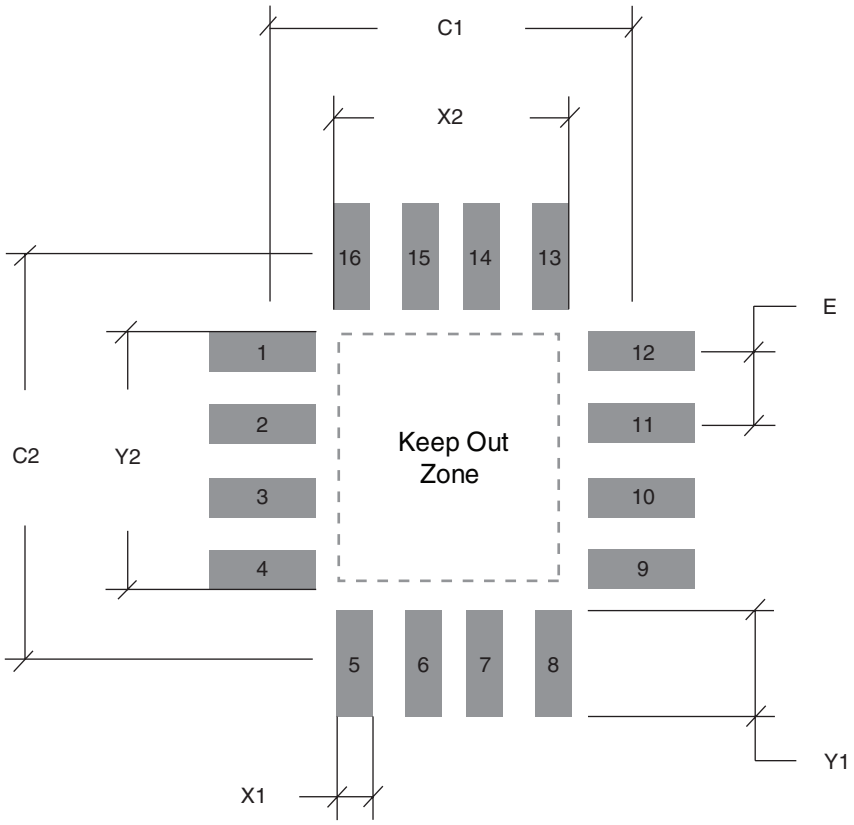
* Use millimeters as the primary measurement.

ECN: S-21437—Rev. A, 19-Aug-02
DWG: 5890

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.

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