Ordering number : EN8302A

SANYO Semiconductors
DATA SHEET

# LC875J64C
# LC875J56C
# LC875J48C

CMOS IC
ROM 64K/56K/48K byte, RAM 2048 byte on-chip
## 8-bit 1-chip Microcontroller

## Overview

The SANYO LC875J64C/56C/48C are 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K/56K/48K byte ROM, 2048 byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a 16-bit timer with a prescaler (may be divided into 8-bit timers), a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, ROM correction function, and a 26-source 10-vector interrupt feature.

## Features

■ROM
- 65536 × 8-bits (LC875J64C)
- 57344 × 8-bits (LC875J56C)
- 49152 × 8-bits (LC875J48C)

■RAM
- 2048 × 9-bits (LC875J64C/56C/48C)

■Minimum Bus Cycle
- 83.3ns (12MHz) $V_{DD}$=3.0 to 5.5V
- 125ns (8MHz) $V_{DD}$=2.5 to 5.5V
- 500ns (2MHz) $V_{DD}$=2.2 to 5.5V

Note : The bus cycle time here refers to the ROM read speed.




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■Minimum Instruction Cycle Time
- 250ns (12MHz) $V_{DD}$=3.0 to 5.5V
- 375ns (8MHz) $V_{DD}$=2.5 to 5.5V
- 1.5μs (2MHz) $V_{DD}$=2.2 to 5.5V

■Ports
- Normal withstand voltage I/O ports
  - Ports whose I/O direction can be designated in 1-bit units: 46 (P1n, P2n, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, XT2)
  - Ports whose I/O direction can be designated in 4-bit units: 8 (P0n)
- Normal withstand voltage input port: 1 (XT1)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pins: 1 ($\overline{RES}$)
- Power pins: 6 ($V_{SS}$1 to 3, $V_{DD}$1 to 3)

■Timers
- Timer 0: 16-bit timer/counter with two capture registers.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8-bits can be used as PWM)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8: 16-bit timer
  - Mode 0: 8-bit timer with an 8-bit prescaler × 2 channels
  - Mode 1: 16-bit timer with an 8-bit prescaler

* Timer 8 is not supported in this version of Emulator. Please use on-chip-debugger (only supported in flash-ROM version) for debugging when developing software.

- Base Timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes

■High-speed Clock Counter

1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Can generate output real-time.

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD Converter: 8-bits × 11 channels

■PWM: Multifrequency 12-bit PWM × 2 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
2) Able to output oscillation clock of sub clock.

■Interrupts
- 26 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|---|---|---|---|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4 |
| 4 | 0001BH | H or L | INT3/INT5/base timer |
| 5 | 00023H | H or L | T0H/INT6 |
| 6 | 0002BH | H or L | T1L/T1H/INT7 |
| 7 | 00033H | H or L | SIO0/UART1 receive/T8L/T8H |
| 8 | 0003BH | H or L | SIO1/UART1 transmit |
| 9 | 00043H | H or L | ADC/T6/T7 |
| 10 | 0004BH | H or L | Port 0/T4/T5/PWM2, PWM3 |

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (list of interrupt source flag function)

3) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the diagram above).

■Subroutine Stack Levels: 1024 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions
- 16-bits × 8-bits (5 tCYC execution time)
- 24-bits × 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf
- Crystal oscillation circuit: For low-speed system clock, with internal Rf
- Frequency variable RC oscillation circuit (internal): For system clock

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are four ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit

■ROM Correction Function

- Executes the correction program on detection of a match with the program counter value.
- Correction program area size : 128 bytes

■Package Form

- QIP64E (14 × 14): Lead-free type
- TQFP64J (10 × 10): Lead-free type

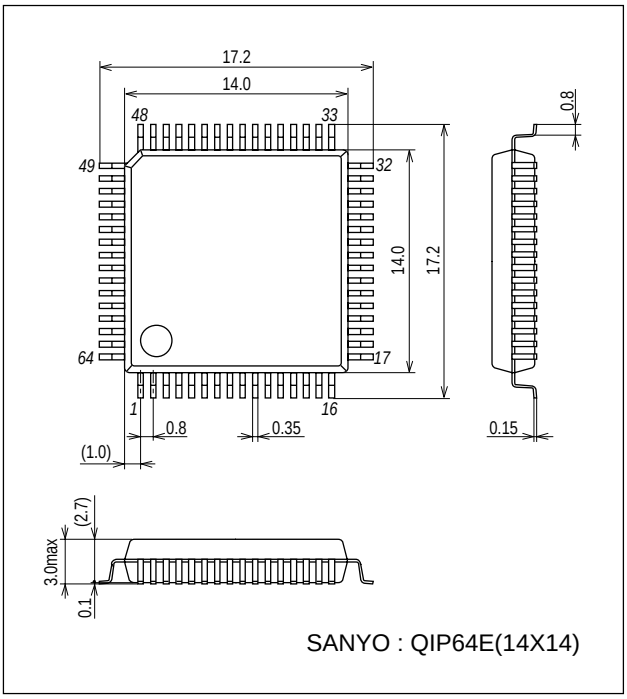
■Development Tools

- Evaluation chip: LC87EV690
- Emulator: EVA62S + ECB876600D + SUB875800 + POD64QFP or POD64SQFP
  ICE-B877300 + SUB875800 + POD64QFP or POD64SQFP
- On-chip debugger: TCB87-TypeA or TCB87-TypeB + LC87F5JC8A

## Package Dimensions

unit : mm (typ)

3159A

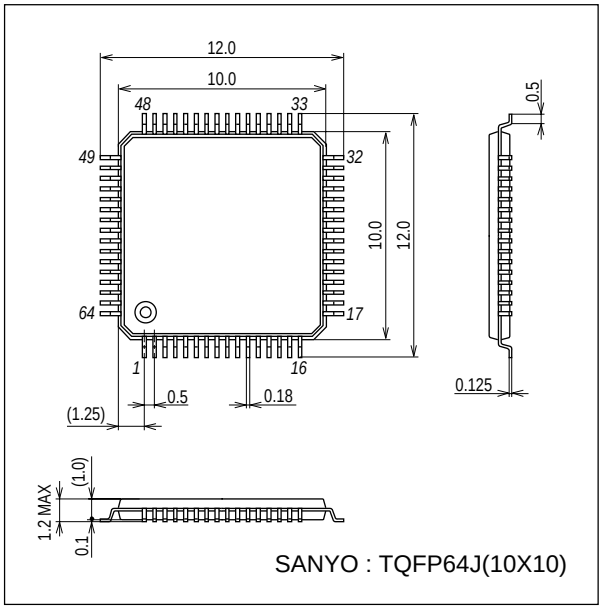



SANYO : QIP64E(14X14)

## Package Dimensions

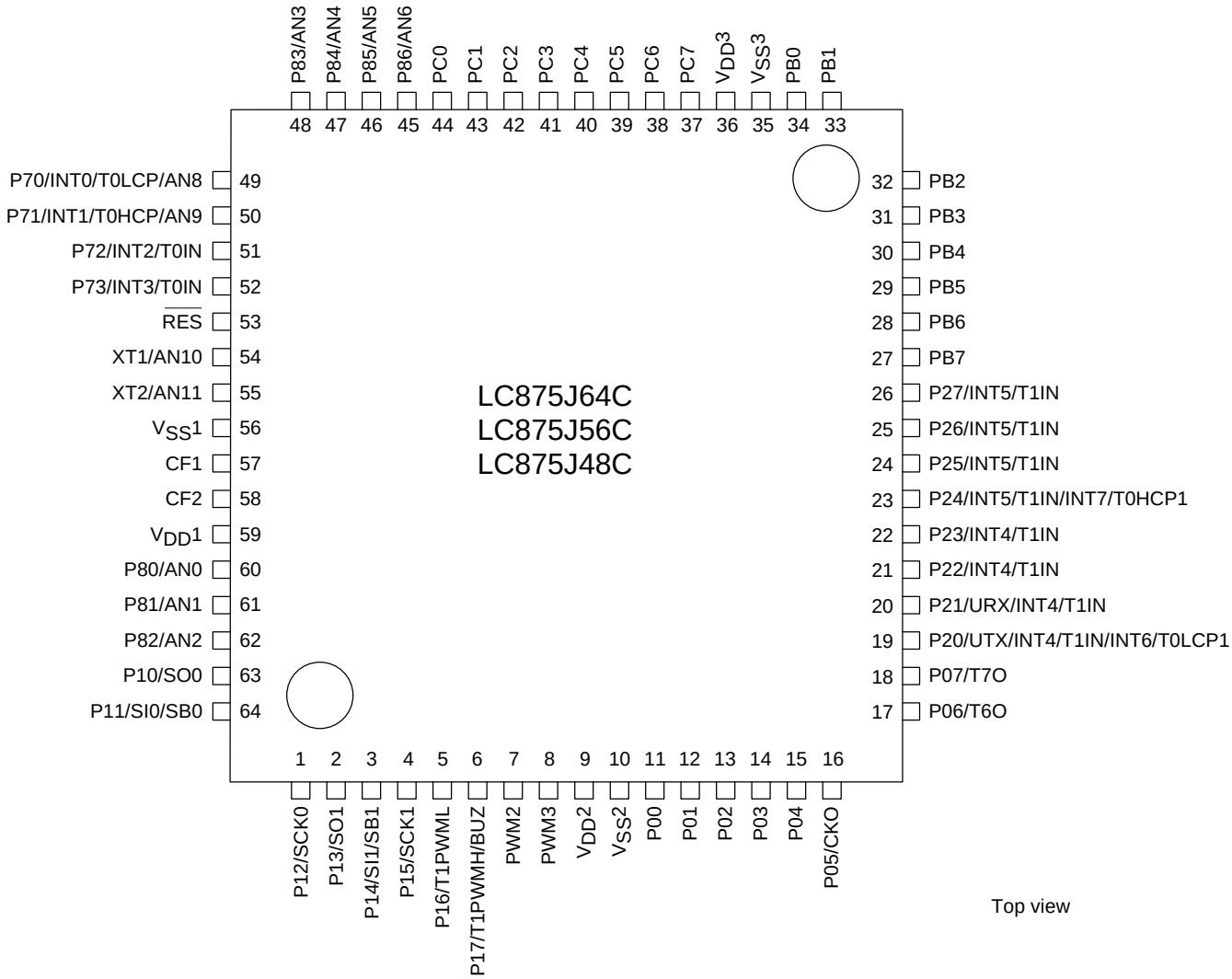
unit : mm (typ)

3310




SANYO : TQFP64J(10X10)

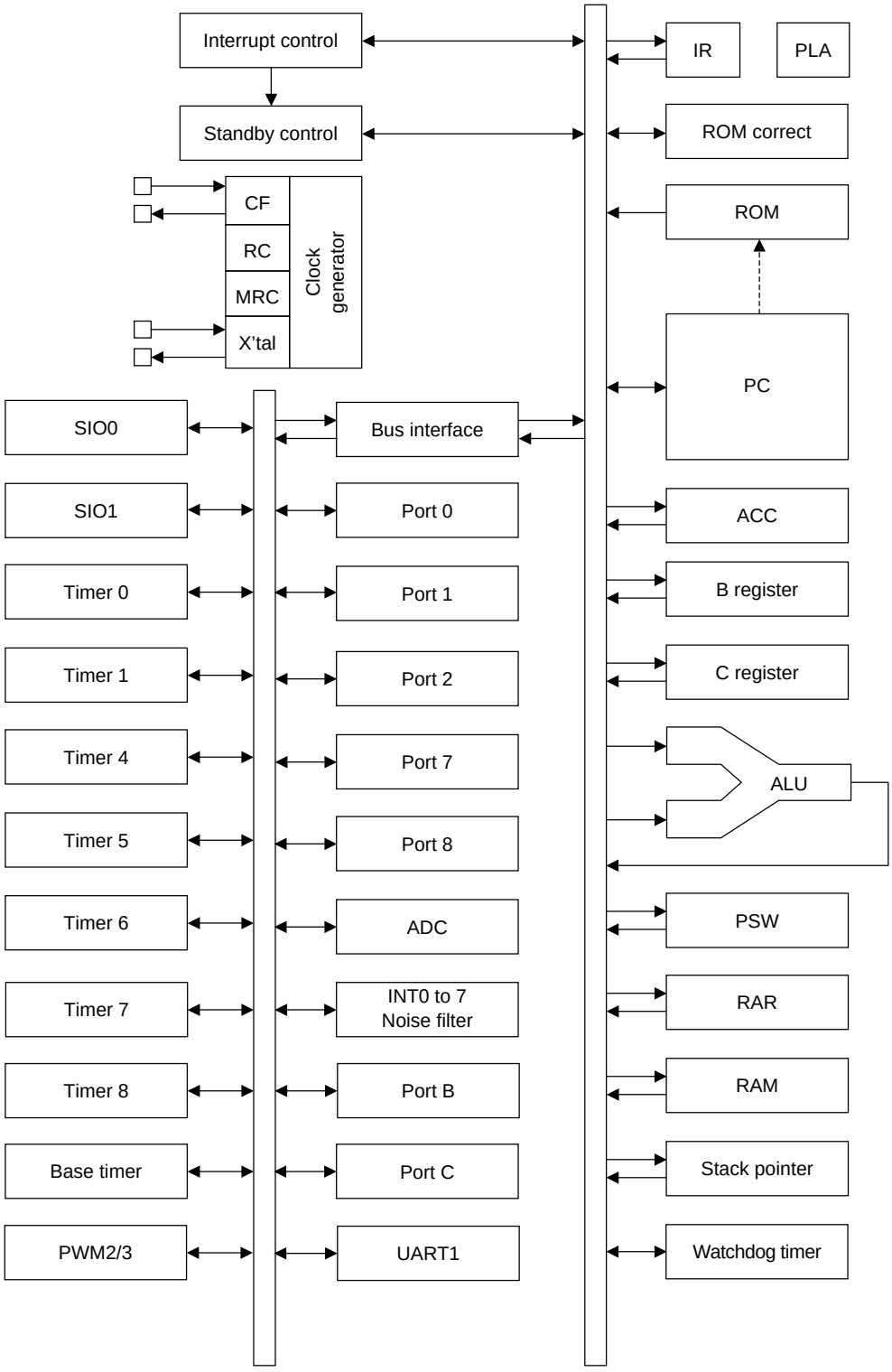
## Pin Assignment




Top view

SANYO: QIP64E(14×14) “Lead-free Type”
SANYO: TQFP64J(10×10) “Lead-free Type”

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$<br>$V_{SS}2$<br>$V_{SS}3$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$<br>$V_{DD}2$<br>$V_{DD}3$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0<br>P00 to P07</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 4-bit units<br>• Pull-up resistors can be turned on and off in 4-bit units.<br>• HOLD reset input<br>• Port 0 interrupt input<br>• Shared pins<br>P05: Clock output (system clock/can selected from sub clock)<br>P06: Timer 6 toggle output<br>P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1<br>P10 to P17</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Pin functions<br>P10: SIO0 data output<br>P11: SIO0 data input/bus I/O<br>P12: SIO0 clock I/O<br>P13: SIO1 data output<br>P14: SIO1 data input/bus I/O<br>P15: SIO1 clock I/O<br>P16: Timer 1PWML output<br>P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2<br>P20 to P27</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Pin functions<br>P20: UART transmit<br>P21: UART receive<br>P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input<br>P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input<br>P20: INT6 input/timer 0L capture 1 input<br>P24: INT7 input/timer 0H capture 1 input<br>Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7<br>P70 to P73</td><td>I/O</td><td>• 4-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.<br>• Shared pins<br>P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output<br>P71: INT1 input/HOLD reset input/timer 0H capture input<br>P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/<br>High speed clock counter input<br>P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input<br>AD converter input port: AN8 (P70), AN9 (P71)<br>Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8<br>P80 to P86</td><td>I/O</td><td>• 7-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Shared pins<br>AD converter input port : AN0 (P80) to AN6 (P86)</td><td>No</td></tr>
<tr><td>PWM2, PWM3</td><td>I/O</td><td>• PWM2 and PWM3 output ports<br>• General-purpose I/O available</td><td>No</td></tr>
<tr><td>Port B<br>PB0 to PB7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.</td><td>Yes</td></tr>
<tr><td>Port C<br>PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistors can be turned on and off in 1-bit units.</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin<br>• Shared pins<br>General-purpose input port<br>AD converter input port: AN10<br>Must be connected to $V_{DD}1$ if not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin<br>• Shared pins<br>General-purpose I/O port<br>AD converter input port: AN11<br>Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

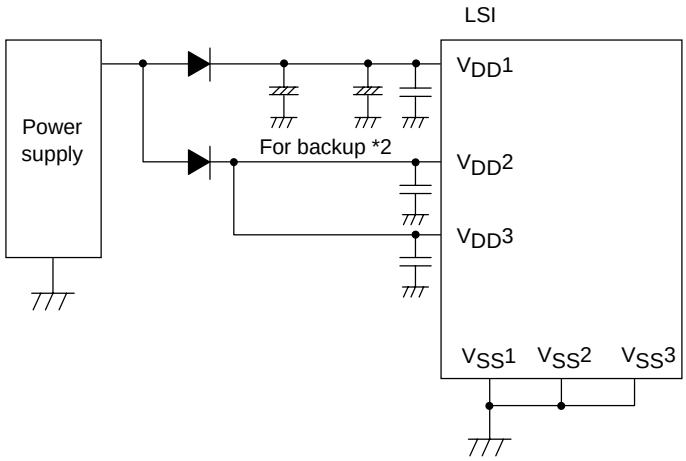
## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port Name | Option Selected in Units of | Option Type | Output Type | Pull-up Resistor |
|---|---|---|---|---|
| P00 to P07 | 1-bit | 1 | CMOS | Programmable (Note 1) |
| | | 2 | Nch-open drain | No |
| P10 to P17 | 1-bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P20 to P27 | 1-bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P70 | - | No | Nch-open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| P80 to P86 | - | No | Nch-open drain | No |
| PWM2, PWM3 | - | No | CMOS | No |
| PB0 to PB7 | 1-bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| PC0 to PC7 | 1-bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| XT1 | - | No | Input for 32.768kHz crystal oscillator (Input only) | No |
| XT2 | - | No | Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode) | No |

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

*1: Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.




*2: The internal memory is sustained by $V_{DD}1$. If none of $V_{DD}2$ and $V_{DD}3$ are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | | Symbol | Pin/Remarks | Conditions | $V_{DD}$ [V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | | -0.3 | | +6.5 | V |
| Input voltage | | $V_I$(1) | XT1, CF1 | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$(1) | Ports 0, 1, 2<br>Ports 7, 8<br>Ports B, C<br>PWM2, PWM3, XT2 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1, 2<br>Ports B, C | CMOS output select<br>Per 1 applicable pin | | -10 | | | mA |
| | | IOPH(2) | PWM2, PWM3 | Per 1 applicable pin | | -20 | | | |
| | | IOPH(3) | P71 to P73 | Per 1 applicable pin | | -5 | | | |
| | Mean output current (Note 1-1) | IOMH(1) | Ports 0, 1, 2<br>Ports B, C | CMOS output select<br>Per 1 applicable pin | | -7.5 | | | |
| | | IOMH(2) | PWM2, PWM3 | Per 1 applicable pin | | -15 | | | |
| | | IOMH(3) | P71 to P73 | Per 1 applicable pin | | -3 | | | |
| | Total output current | ΣIOAH(1) | P71 to P73 | Total of all applicable pins | | -10 | | | |
| | | ΣIOAH(2) | Port 1<br>PWM2, PWM3 | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(3) | Ports 0, 2 | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(4) | Ports 0, 1, 2<br>PWM2, PWM3 | Total of all applicable pins | | -45 | | | |
| | | ΣIOAH(5) | Port B | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(6) | Port C | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(7) | Ports B, C | Total of all applicable pins | | -45 | | | |
| Low level output current | Peak output current | IOPL(1) | P02 to P07<br>Ports 1, 2<br>Ports B, C<br>PWM2, PWM3 | Per 1 applicable pin | | | | 20 | |
| | | IOPL(2) | P00, P01 | Per 1 applicable pin | | | | 30 | |
| | | IOPL(3) | Ports 7, 8<br>XT2 | Per 1 applicable pin | | | | 10 | |
| | Mean output current (Note 1-1) | IOML(1) | P02 to P07<br>Ports 1, 2<br>Ports B, C<br>PWM2, PWM3 | Per 1 applicable pin | | | | 15 | |
| | | IOML(2) | P00, P01 | Per 1 applicable pin | | | | 20 | |
| | | IOML(3) | Ports 7, 8<br>XT2 | Per 1 applicable pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | Port 7<br>P83 to P86, XT2 | Total of all applicable pins | | | | 15 | |
| | | ΣIOAL(2) | P80 to P82 | Total of all applicable pins | | | | 15 | |
| | | ΣIOAL(3) | Ports 7, 8<br>XT2 | Total of all applicable pins | | | | 20 | |
| | | ΣIOAL(4) | Port 1<br>PWM2, PWM3 | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(5) | Ports 0, 2 | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(6) | Ports 0, 1, 2<br>PWM2, PWM3 | Total of all applicable pins | | | | 80 | |
| | | ΣIOAL(7) | Port B | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(8) | Port C | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(9) | Ports B, C | Total of all applicable pins | | | | 80 | |
| Power dissipation | | Pd max | QIP64E (14 × 14) | Ta=-30 to +70°C | | | | 355 | mW |
| | | | TQFP64J (10 × 10) | | | | | 255 | |
| Operating ambient temperature | | Topr | | | | -30 | | +70 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: The mean output current is a mean value measured over 100ms.

## Allowable Operating Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Operating supply voltage | $V_{DD}(1)$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | 0.245µs≤tCYC≤200µs | | 3.0 | | 5.5 | V |
| | | | 0.367µs≤tCYC≤200µs | | 2.5 | | 5.5 | |
| | | | 1.47µs≤tCYC≤200µs | | 2.2 | | 5.5 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3$ | RAM and register contents sustained in HOLD mode. | | 2.0 | | 5.5 | |
| High level input voltage | $V_{IH}(1)$ | Ports 1, 2<br>P71 to P73<br>P70 port input/ interrupt side | | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(2)$ | Ports 0, 8, B, C<br>PWM2, PWM3 | | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(3)$ | Port 70 watchdog timer side | | 2.2 to 5.5 | $0.9V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(4)$ | XT1, XT2, CF1<br>$\overline{RES}$ | | 2.2 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1, 2<br>P71 to P73<br>P70 port input/ interrupt side | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}$ +0.4 | |
| | | | | 2.2 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | Ports 0, 8, B, C<br>PWM2, PWM3 | | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}$ +0.4 | |
| | | | | 2.2 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 70 watchdog timer side | | 2.2 to 5.5 | $V_{SS}$ | | $0.8V_{DD}$ -1.0 | |
| | $V_{IL}(4)$ | XT1, XT2, CF1<br>$\overline{RES}$ | | 2.2 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-1) | tCYC | | | 3.0 to 5.5 | 0.245 | | 200 | µs |
| | | | | 2.5 to 5.5 | 0.367 | | 200 | |
| | | | | 2.2 to 5.5 | 1.47 | | 200 | |
| External system clock frequency | FEXCF(1) | CF1 | • CF2 pin open<br>• System clock frequency division ratio=1/1<br>• External system clock duty =50 ± 5% | 3.0 to 5.5 | 0.1 | | 12 | MHz |
| | | | | 2.5 to 5.5 | 0.1 | | 8 | |
| | | | | 2.2 to 5.5 | 0.1 | | 2 | |
| | | | • CF2 pin open<br>• System clock frequency division ratio=1/2 | 3.0 to 5.5 | 0.2 | | 24.4 | |
| | | | | 2.5 to 5.5 | 0.2 | | 16 | |
| | | | | 2.2 to 5.5 | 0.2 | | 4 | |
| Oscillation frequency range (Note 2-2) | FmCF(1) | CF1, CF2 | 12MHz ceramic oscillation<br>See Fig. 1. | 3.0 to 5.5 | | 12 | | |
| | FmCF(2) | CF1, CF2 | 8MHz ceramic oscillation<br>See Fig. 1. | 2.5 to 5.5 | | 8 | | |
| | FmCF(3) | CF1, CF2 | 4MHz ceramic oscillation<br>See Fig. 1. | 2.2 to 5.5 | | 4 | | |
| | FmRC | | Internal RC oscillation | 2.2 to 5.5 | 0.3 | 1.0 | 2.0 | |
| | FmMRC | | Frequency variable RC oscillation source oscillation | 2.2 to 5.5 | | 16 | | |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation<br>See Fig. 2. | 2.2 to 5.5 | | 32.768 | | kHz |

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See Tables 1 and 2 for the oscillation constants.

## Electrical Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| High level input current | $I_{IH}(1)$ | Ports 0, 1, 2<br>Ports 7, 8<br>Ports B, C<br>$\overline{RES}$<br>PWM2, PWM3 | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{DD}$<br>(Including output Tr's off leakage current) | 2.2 to 5.5 | | | 1 | µA |
| | $I_{IH}(2)$ | XT1, XT2 | For input port specification<br>$V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 1 | |
| | $I_{IH}(3)$ | CF1 | $V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}(1)$ | Ports 0, 1, 2<br>Ports 7, 8<br>Ports B, C<br>$\overline{RES}$<br>PWM2, PWM3 | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{SS}$<br>(Including output Tr's off leakage current) | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(2)$ | XT1, XT2 | For input port specification<br>$V_{IN}=V_{SS}$ | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(3)$ | CF1 | $V_{IN}=V_{SS}$ | 2.2 to 5.5 | -15 | | | |
| High level output voltage | $V_{OH}(1)$ | Ports 0, 1, 2<br>Ports B, C | $I_{OH}$=-1mA | 4.5 to 5.5 | $V_{DD}$-1 | | | V |
| | $V_{OH}(2)$ | | $I_{OH}$=-0.4mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(3)$ | | $I_{OH}$=-0.2mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(4)$ | P71 to P73 | $I_{OH}$=-0.4mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(5)$ | | $I_{OH}$=-0.2mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(6)$ | PWM2, PWM3 | $I_{OH}$=-10mA | 4.5 to 5.5 | $V_{DD}$-1.5 | | | |
| | $V_{OH}(7)$ | | $I_{OH}$=-1.6mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(8)$ | | $I_{OH}$=-1mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| Low level output voltage | $V_{OL}(1)$ | Ports 0, 1, 2<br>Ports B, C<br>PWM2, PWM3 | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(3)$ | | $I_{OL}$=1mA | 2.2 to 5.5 | | | 0.4 | |
| | $V_{OL}(4)$ | Ports 7, 8<br>XT2 | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(5)$ | | $I_{OL}$=1mA | 2.2 to 5.5 | | | 0.4 | |
| | $V_{OL}(6)$ | P00, P01 | $I_{OL}$=30mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(7)$ | | $I_{OL}$=5mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(8)$ | | $I_{OL}$=2.5mA | 2.2 to 5.5 | | | 0.4 | |
| Pull-up resistance | Rpu(1) | Ports 0, 1, 2, 7<br>Ports B, C | $V_{OH}=0.9V_{DD}$ | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 2.2 to 5.5 | 18 | 50 | 150 | |
| Hysteresis voltage | VHYS | $\overline{RES}$<br>Ports 1, 2, 7 | | 2.2 to 5.5 | | 0.1<br>$V_{DD}$ | | V |
| Pin capacitance | CP | All pins | For pins other than that under test:<br>$V_{IN}=V_{SS}$<br>f=1MHz<br>Ta=25°C | 2.2 to 5.5 | | 10 | | pF |

## Serial Input/Output Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1) | | • Continuous data transmission/reception mode<br>• See Fig. 6.<br>• (Note 4-1-2) | | 4 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected<br>• See Fig. 6. | 2.2 to 5.5 | 4/3 | | | |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| | | | tSCKHA(2) | | • Continuous data transmission/reception mode<br>• CMOS output selected<br>• See Fig. 6. | | tSCKH(2) +2tCYC | | tSCKH(2) +(10/3) tCYC | tCYC |
| Serial input | Data setup time | | tsDI(1) | SB0(P11), SI0(P11) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(1) | | | | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdD0(1) | SO0(P10), SB0(P11) | • Continuous data transmission/reception mode<br>• (Note 4-1-3) | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |
| | | | tdD0(2) | | • Synchronous 8-bit mode<br>• (Note 4-1-3) | | | | 1tCYC +0.05 | |
| | Output clock | | tdD0(3) | | (Note 4-1-3) | | | | (1/3)tCYC +0.05 | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig. 6. | | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected<br>• See Fig. 6. | | 2 | | | |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 6. | | 0.03 | | | µs |
| | Data hold time | | thDI(2) | | | | 0.03 | | | |
| Serial output | Output delay time | | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 6. | | | | (1/3)tCYC +0.05 | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

## Pulse Input Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70),<br>INT1(P71),<br>INT2(P72),<br>INT4(P20 to P23),<br>INT5(P24 to P27),<br>INT6(P20),<br>INT7(P24) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 2.2 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P73) when noise filter time constant is 1/32 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P73) when noise filter time constant is 1/128 | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{RES}$ | Resetting is enabled. | 2.2 to 5.5 | 200 | | | µs |

## AD Converter Characteristics / Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Resolution | N | AN0(P80) to AN6(P86), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2) | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2) | 4.5 to 5.5 | 15.68 (tCYC= 0.49µs) | | 97.92 (tCYC= 3.06µs) | µs |
| | | | | 3.0 to 5.5 | 23.52 (tCYC= 0.735µs) | | 97.92 (tCYC= 3.06µs) | |
| | | | AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2) | 4.5 to 5.5 | 18.82 (tCYC= 0.294µs) | | 97.92 (tCYC= 1.53µs) | |
| | | | | 3.0 to 5.5 | 47.04 (tCYC= 0.735µs) | | 97.92 (tCYC= 1.53µs) | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

## Consumption Current Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | $V_{DD}$ [V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Normal mode consumption current (Note 7-1) | IDDOP(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio | 4.5 to 5.5 | | 8 | 13.5 | mA |
| | IDDOP(2) | | | 3.0 to 3.6 | | 4.5 | 8 | |
| | IDDOP(3) | | • CF1=24MHz external clock • FmX'tal=32.768kHz crystal oscillation mode • System clock set to CF1 side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio | 4.5 to 5.5 | | 9.5 | 16 | |
| | IDDOP(4) | | | 3.0 to 3.6 | | 5.2 | 8.8 | |
| | IDDOP(5) | | • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/1 frequency division ratio | 4.5 to 5.5 | | 5.5 | 9 | |
| | IDDOP(6) | | | 3.0 to 3.6 | | 3.1 | 5.6 | |
| | IDDOP(7) | | | 2.5 to 3.0 | | 2.2 | 3.8 | |
| | IDDOP(8) | | • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio | 4.5 to 5.5 | | 2 | 3.2 | |
| | IDDOP(9) | | | 3.0 to 3.6 | | 1 | 2 | |
| | IDDOP(10) | | | 2.2 to 3.0 | | 0.7 | 1.4 | |
| | IDDOP(11) | | • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped • 1/2 frequency division ratio | 4.5 to 5.5 | | 0.55 | 2.1 | |
| | IDDOP(12) | | | 3.0 to 3.6 | | 0.3 | 1.4 | |
| | IDDOP(13) | | | 2.2 to 3.0 | | 0.2 | 1 | |
| | IDDOP(14) | | • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped • System clock set to 1MHz with frequency variable RC oscillation • 1/2 frequency division ratio | 4.5 to 5.5 | | 1.2 | 3.5 | |
| | IDDOP(15) | | | 3.0 to 3.6 | | 0.65 | 2.2 | |
| | IDDOP(16) | | | 2.2 to 3.0 | | 0.4 | 1.6 | |
| | IDDOP(17) | | • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped • 1/2 frequency division ratio | 4.5 to 5.5 | | 27 | 65 | μA |
| | IDDOP(18) | | | 3.0 to 3.6 | | 11 | 45 | |
| | IDDOP(19) | | | 2.2 to 3.0 | | 7 | 32 | |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| HALT mode consumption current (Note 7-1) | IDDHALT(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal RC oscillation stopped<br>• Frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 2.7 | 5.5 | mA |
| | IDDHALT(2) | | | 3.0 to 3.6 | | 1.4 | 3 | |
| | IDDHALT(3) | | • HALT mode<br>• CF1=24MHz external clock<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to CF1 side<br>• Internal RC oscillation stopped<br>• Frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 3.6 | 7.4 | |
| | IDDHALT(4) | | | 3.0 to 3.6 | | 1.9 | 4.1 | |
| | IDDHALT(5) | | • HALT mode<br>• FmCF=8MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 8MHz side<br>• Internal RC oscillation stopped<br>• Frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 2 | 4.2 | |
| | IDDHALT(6) | | | 3.0 to 3.6 | | 1.1 | 2.3 | |
| | IDDHALT(7) | | | 2.5 to 3.0 | | 0.7 | 1.5 | |
| | IDDHALT(8) | | • HALT mode<br>• FmCF=4MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 4MHz side<br>• Internal RC oscillation stopped<br>• Frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 1 | 2.1 | |
| | IDDHALT(9) | | | 3.0 to 3.6 | | 0.5 | 1.1 | |
| | IDDHALT(10) | | | 2.2 to 3.0 | | 0.3 | 0.7 | |
| | IDDHALT(11) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal RC oscillation<br>• Frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 0.28 | 1 | |
| | IDDHALT(12) | | | 3.0 to 3.6 | | 0.15 | 0.7 | |
| | IDDHALT(13) | | | 2.2 to 3.0 | | 0.1 | 0.5 | |
| | IDDHALT(14) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• Internal RC oscillation stopped<br>• System clock set to 1MHz with frequency variable RC oscillation<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 1 | 2.9 | |
| | IDDHALT(15) | | | 3.0 to 3.6 | | 0.55 | 1.8 | |
| | IDDHALT(16) | | | 2.2 to 3.0 | | 0.35 | 1.4 | |
| | IDDHALT(17) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal RC oscillation stopped<br>• Frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 19 | 50 | μA |
| | IDDHALT(18) | | | 3.0 to 3.6 | | 6.2 | 30 | |
| | IDDHALT(19) | | | 2.2 to 3.0 | | 3.6 | 20 | |
| HOLD mode consumption current | IDDHOLD(1) | $V_{DD}1$ | • HOLD mode<br>• CF1=$V_{DD}$ or open (external clock mode) | 4.5 to 5.5 | | 0.015 | 10 | |
| | IDDHOLD(2) | | | 3.0 to 3.6 | | 0.009 | 7 | |
| | IDDHOLD(3) | | | 2.2 to 3.0 | | 0.006 | 6 | |
| Timer HOLD mode consumption current | IDDHOLD(4) | | • Timer HOLD mode<br>• CF1=$V_{DD}$ or open (external clock mode)<br>• FmX'tal=32.768kHz crystal oscillation mode | 4.5 to 5.5 | | 16 | 45 | |
| | IDDHOLD(5) | | | 3.0 to 3.6 | | 5.5 | 25 | |
| | IDDHOLD(6) | | | 2.2 to 3.0 | | 3 | 15 | |

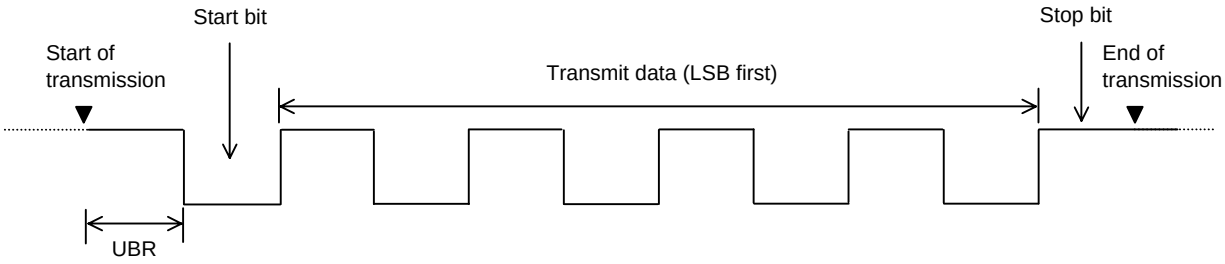
Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

## UART (Full Duplex) Operating Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

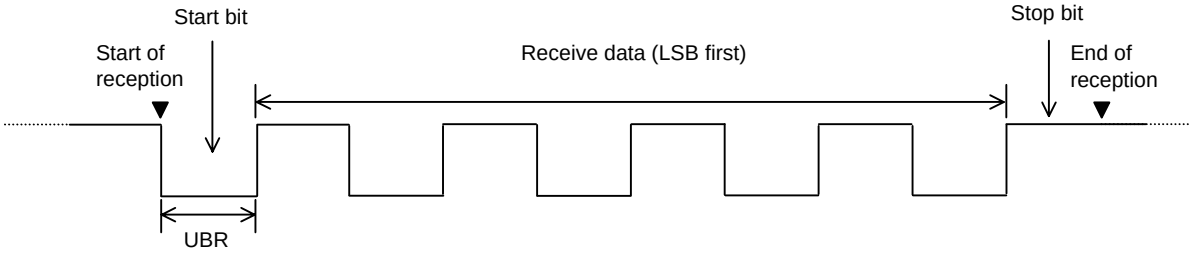
| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ [V] | min | typ | max | unit |
| Transfer rate | UBR | UTX(P20), URX(P21) | 2.2 to 5.5 | 16/3 | | 8192/3 | tCYC |

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1-bit (2-bit in continuous data transmission)
Parity bits: None

*Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)




*Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rf [Ω] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0G52-R0 | (10) | (10) | Open | 470 | 3.0 to 5.5 | 0.1 | 0.5 | Internal C1, C2 |
| 8MHz | MURATA | CSTCE8M00G52-R0 | (10) | (10) | Open | 2.2k | 2.7 to 5.5 | 0.1 | 0.5 | Internal C1, C2 |
| | | CSTLS8M00G53-R0 | (15) | (15) | Open | 680 | 2.5 to 5.5 | 0.1 | 0.5 | |
| 4MHz | MURATA | CSTCR4M00G53-R0 | (15) | (15) | Open | 3.3k | 2.2 to 5.5 | 0.2 | 0.6 | Internal C1, C2 |
| | | CSTLS4M00G53-B0 | (15) | (15) | Open | 3.3k | 2.2 to 5.5 | 0.2 | 0.6 | |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after $V_{DD}$ goes above the operating voltage lower limit (see Figure 4).

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C3 [pF] | C4 [pF] | Rf [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | SEIKO EPSON | MC-306 | 18 | 18 | Open | 560k | 2.2 to 5.5 | 1.4 | 3.0 | Applicable CL value = 12.5pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

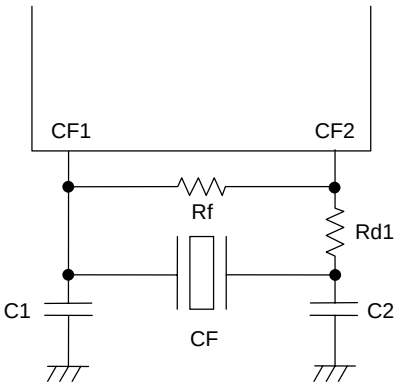



Figure 1 CF Oscillator Circuit

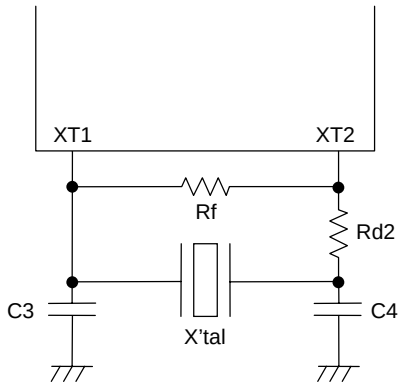



Figure 2 XT Oscillator Circuit

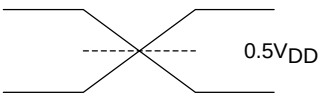
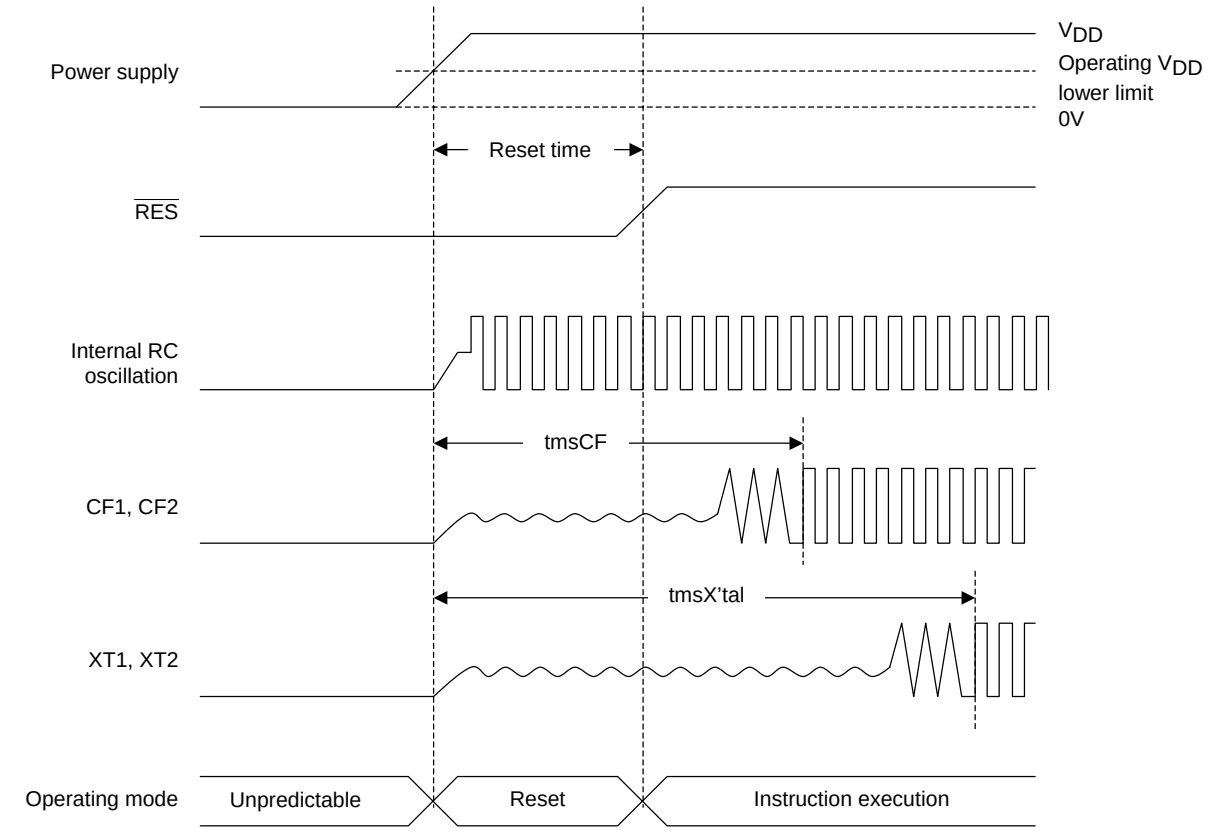
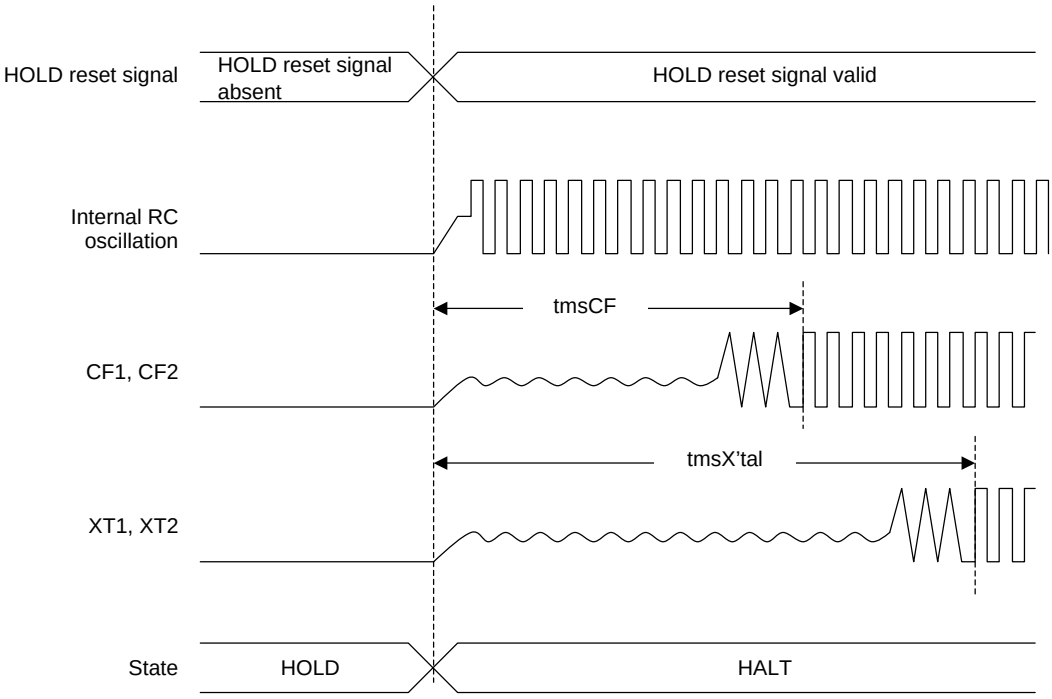



Figure 3 AC Timing Measurement Point

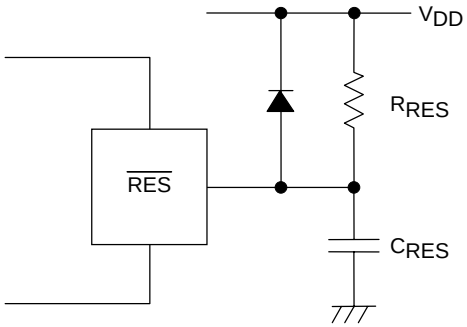



Reset Time and Oscillation Stabilizing Time




HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times




Note:
Determine the value of $C_{RES}$ and $R_{RES}$ so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

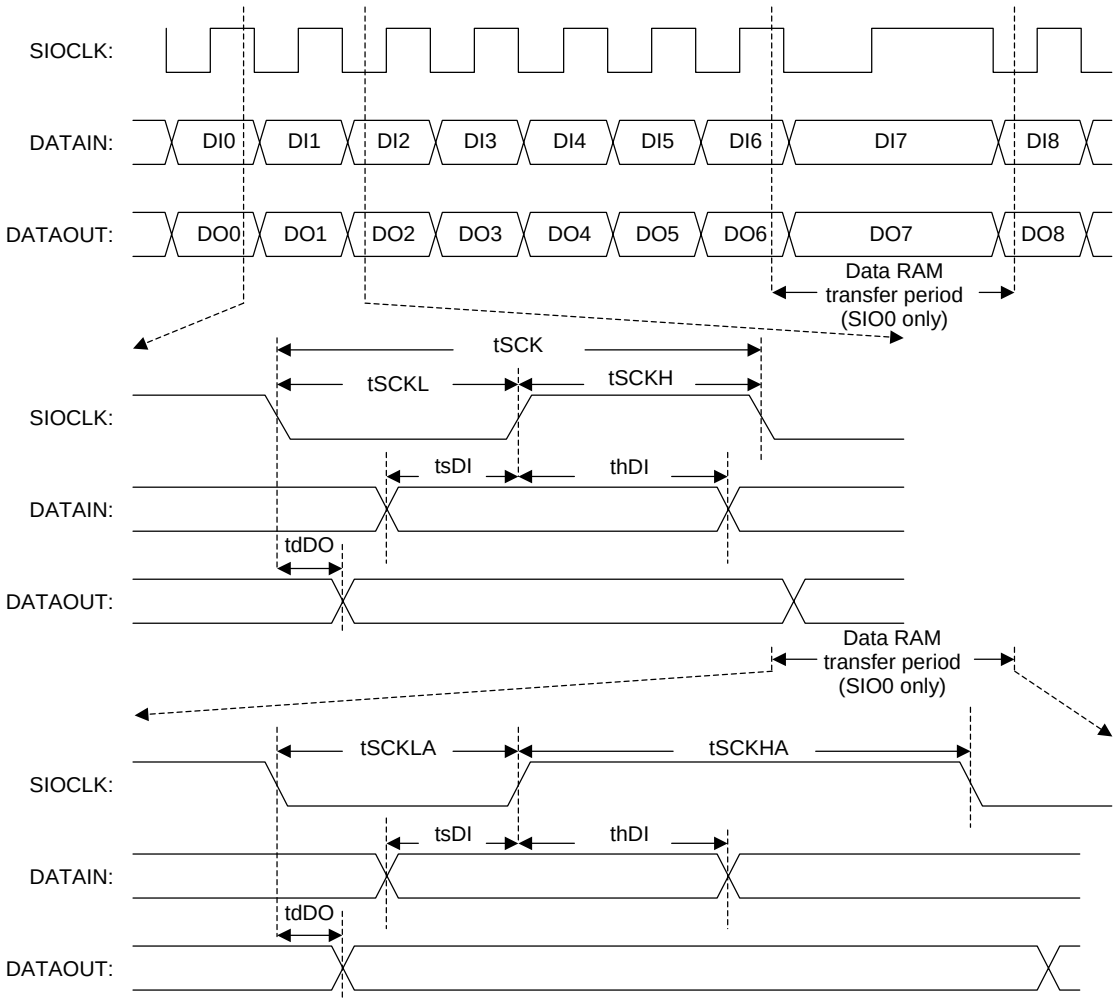



Figure 6 Serial I/O Output Waveforms

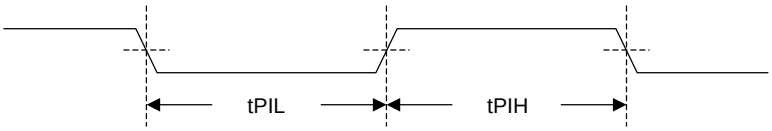



Figure 7 Pulse Input Timing Signal Waveform

This catalog provides information as of February, 2007. Specifications and information herein are subject to change without notice.