freescale
飞思卡尔(深圳)功率半导体有限公司

TK40P04M1

MOSFETs Silicon N-Channel MOS (U-MOSVI-H)

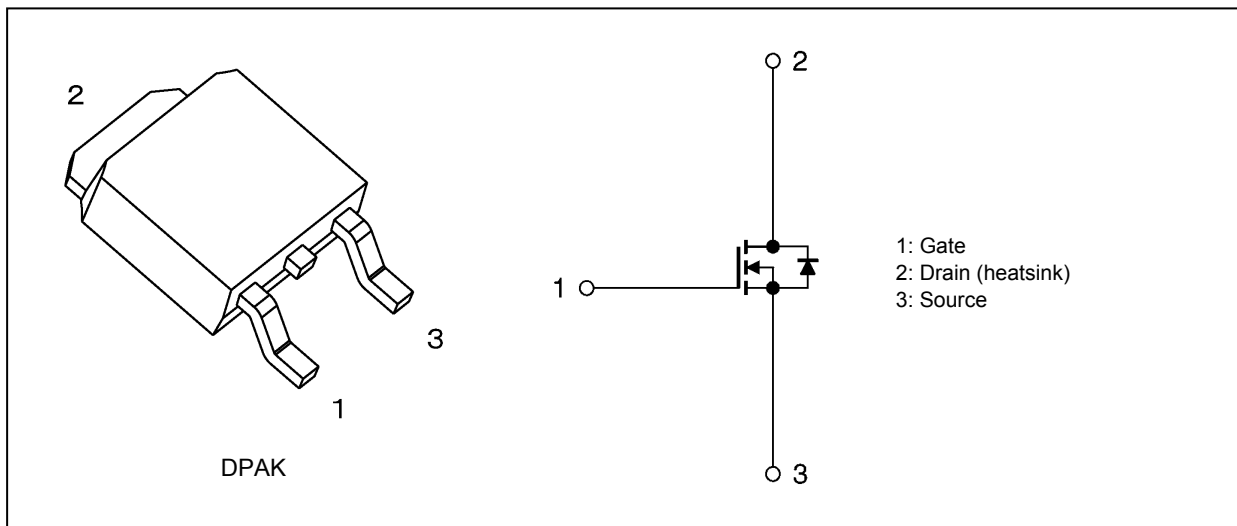## 1. Applications

- Switching Voltage Regulators
- Motor Drivers

2. Features

(1) High-speed switching

(2) Low gate charge: Q_{SW} = 7.4 nC (typ.)

(3) Low drain-source on-resistance: $R_{DS(ON)}$ = 8.5 mΩ (typ.) (V_{GS} = 10 V)

(4) Low leakage current: I_{DSS} = 10 µA (max) (V_{DS} = 40 V)

(5) Enhancement mode: V_{th} = 1.3 to 2.3 V (V_{DS} = 10 V, I_D = 0.2 mA)

3. Packaging and Internal Circuit

DPAK

1: Gate
2: Drain (heatsink)
3: Source

4. Absolute Maximum Ratings (Note) (T_a = 25℃ unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	40	V
Gate-source voltage		V_{GSS}	±20	
Drain current (DC)	(Note 1)	I_D	40	A
Drain current (pulsed)	(Note 1)	I_{DP}	120	
Power dissipation	(T_c = 25℃)	P_D	47	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	41	mJ
Avalanche current		I_{AR}	40	A
Channel temperature		T_{ch}	150	℃
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	2.65	℃/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	125	

Note 1: Ensure that the channel temperature does not exceed 150℃.

Note 2: V_{DD} = 32 V, T_{ch} = 25℃ (initial), L = 20 μH, R_G = 25 Ω, I_{AR} = 40 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25℃ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	40	—	—	V
	$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	25	—	—	
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 0.2 mA	1.3	—	2.3	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 A	—	10.3	13.4	mΩ
		V_{GS} = 10 V, I_D = 20 A	—	8.5	11	

6.2. Dynamic Characteristics (T_a = 25℃ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1920	—	pF
Reverse transfer capacitance	C_{rss}		—	90	—	
Output capacitance	C_{oss}		—	310	—	
Gate resistance	r_g	V_{DS} = 10 V, V_{GS} = 0 V, f = 5 MHz	—	1.6	3.5	Ω
Switching time (rise time)	t_r	See Figure 6.2.1.	—	20	—	ns
Switching time (turn-on time)	t_{on}		—	27	—	
Switching time (fall time)	t_f		—	18	—	
Switching time (turn-off time)	t_{off}		—	63	—	

V_{GS} 10 V 0 V I_D = 20 A V_{OUT} 4.7 Ω R_L = 1.0 Ω $V_{DD} \approx$ 20 V

Duty ≤ 1%, t_W = 10 μs

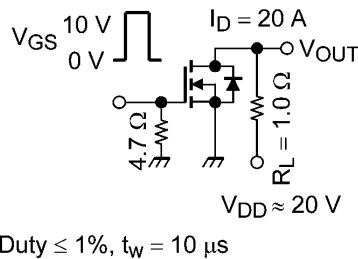**Fig. 6.2.1   Switching Time Test Circuit**

6.3. Gate Charge Characteristics (T_a = 25℃ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx$ 32 V, V_{GS} = 10 V, I_D = 40 A	—	29	—	nC
		$V_{DD} \approx$ 32 V, V_{GS} = 5 V, I_D = 40 A	—	15	—	
Gate-source charge 1	Q_{gs1}	$V_{DD} \approx$ 32 V, V_{GS} = 10 V, I_D = 40 A	—	6.0	—	
Gate-drain charge	Q_{gd}		—	4.7	—	
Gate switch charge	Q_{SW}		—	7.4	—	

6.4. Source-Drain Characteristics (T_a = 25℃ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 3)	I_{DRP}	—	—	—	120	A
Diode forward voltage	V_{DSF}	I_{DR} = 40 A, V_{GS} = 0 V	—	—	-1.2	V

Note 3: Ensure that the channel temperature does not exceed 150℃.

7. Marking

Fig. 7.1   Marking
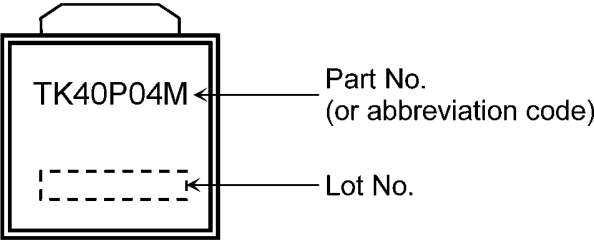
Part No.
(or abbreviation code)

Lot No.
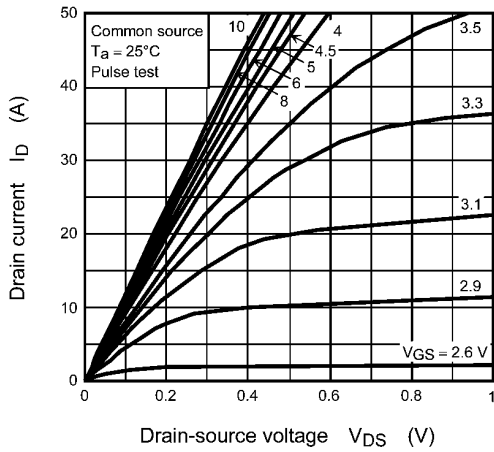
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8. Characteristics Curves (Note)
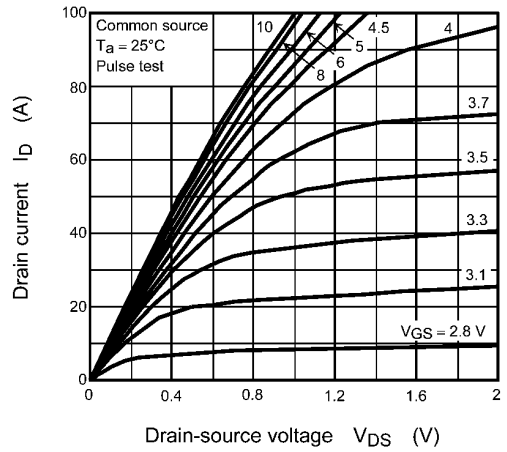

Fig. 8.1 $I_D - V_{DS}$

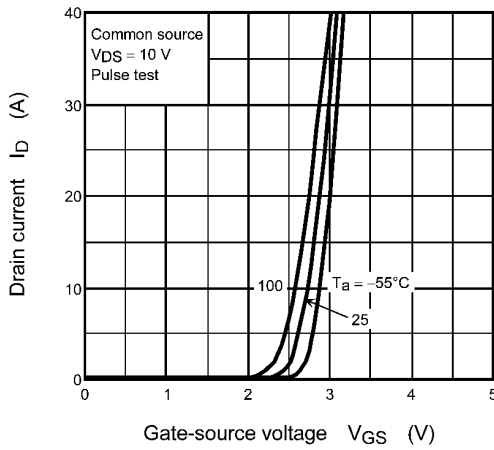**Fig. 8.2** $I_D - V_{DS}$

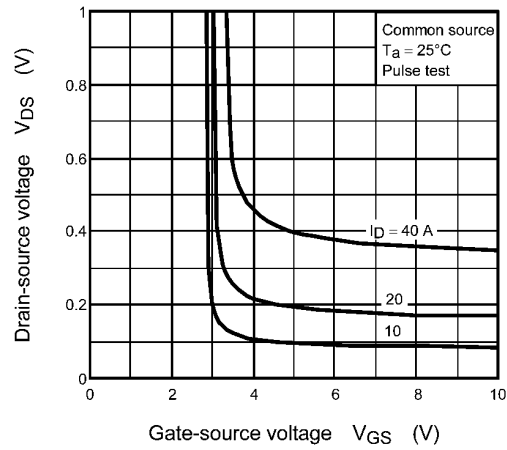**Fig. 8.3** $I_D - V_{GS}$

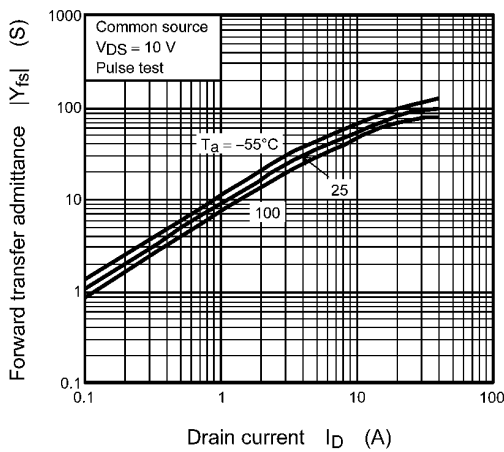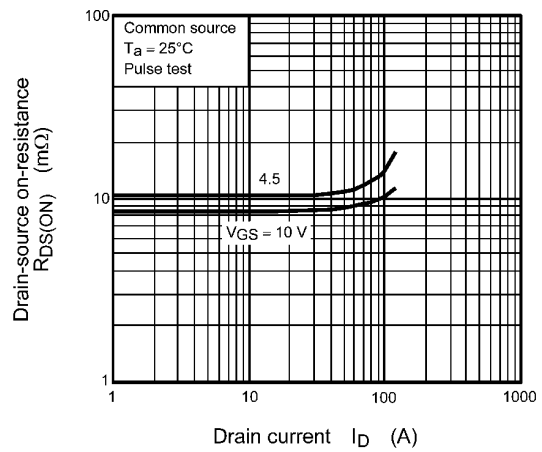**Fig. 8.4** $V_{DS} - V_{GS}$

Fig. 8.5 $|Y_{fs}| - I_D$

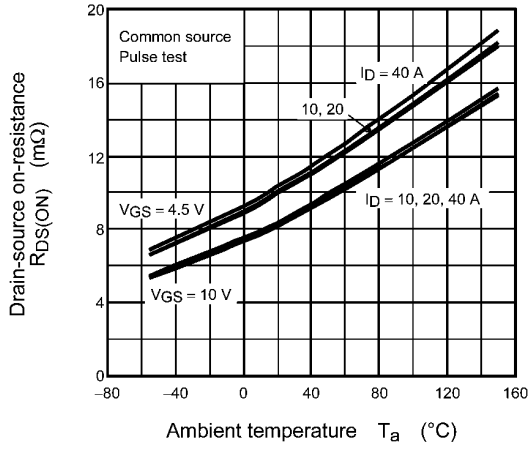**Fig. 8.6** $R_{DS(ON)} - I_D$
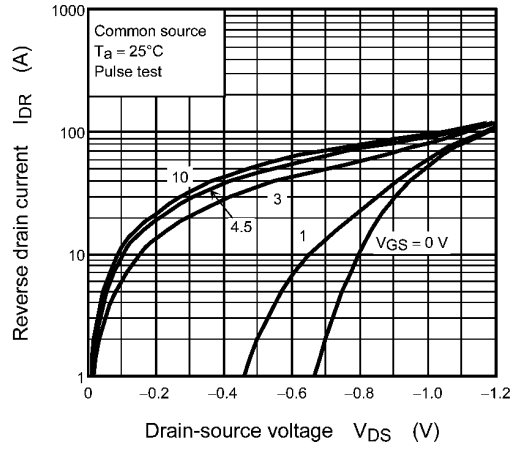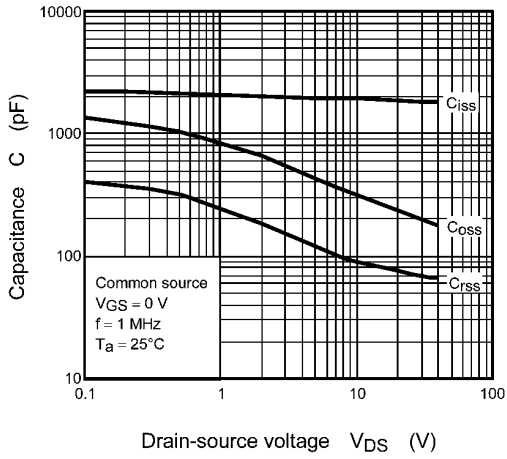
Fig. 8.7 $R_{DS(ON)}$ - T_a

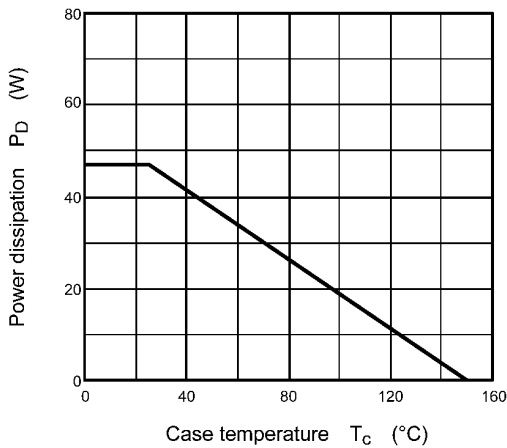Fig. 8.8 I_{DR} - V_{DS}

Fig. 8.9 Capacitance - V_{DS}
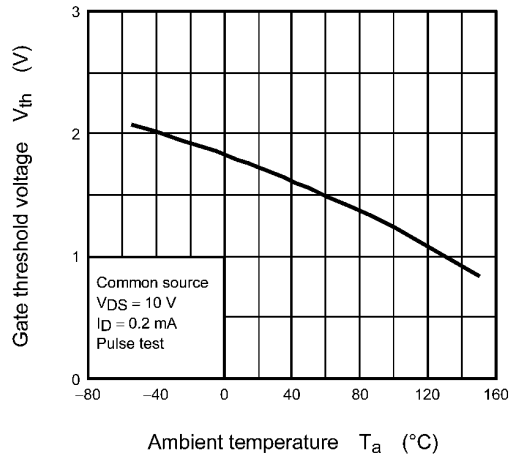
Fig. 8.10 V_{th} - T_a
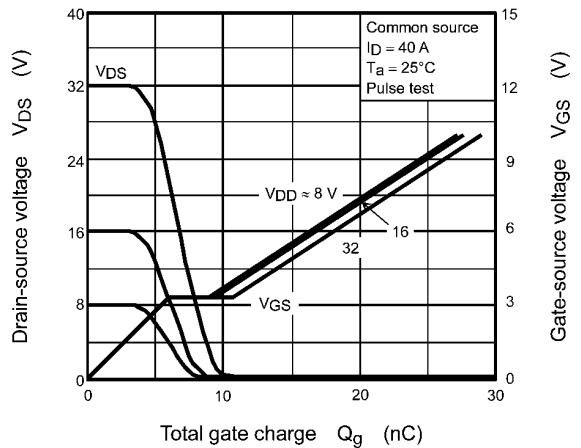
Fig. 8.11 P_D - T_c
(Guaranteed Maximum)

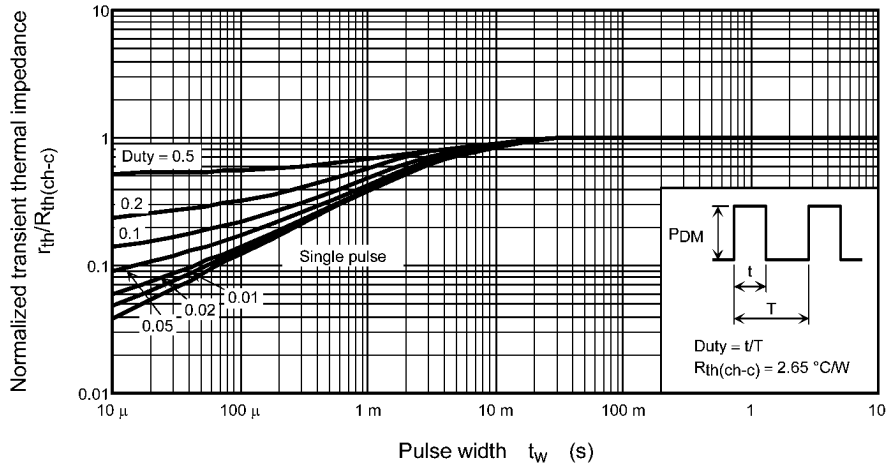Fig. 8.12 Dynamic Input/Output Characteristics

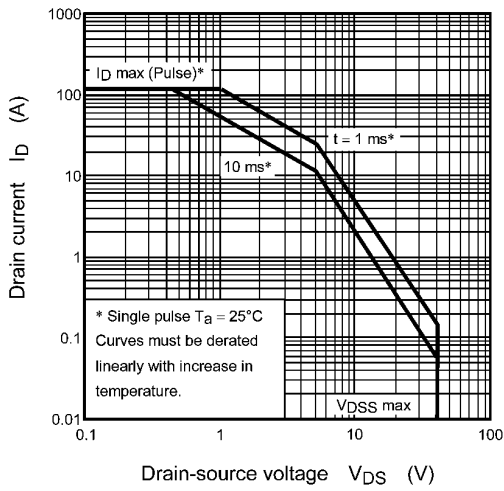Fig. 8.13 $r_{th}/R_{th(ch-c)}$ - t_w
(Guaranteed Maximum)
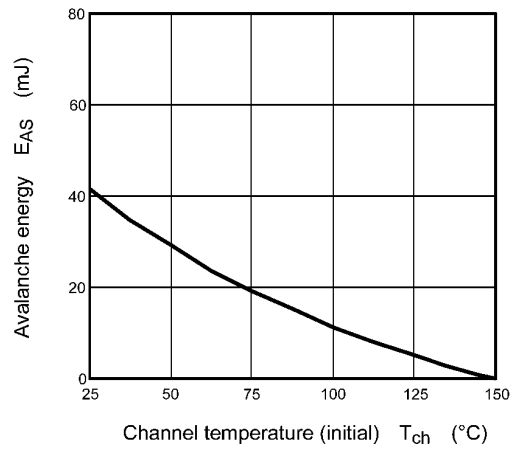
Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)
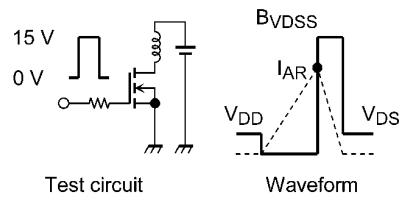
Fig. 8.15 E_{AS} - T_{ch}
(Guaranteed Maximum)

$R_G = 25\ \Omega$
$V_{DD} = 32\ V,\ L = 20\ \mu H$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2_{AR} \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Fig. 8.16 Test Circuit/Waveform

Package Dimensions

6.6 ± 0.2

5.34 ± 0.13

1.08 ± 0.2

2.3 ± 0.1

0.58Max

1.0Max

6.1 ± 0.12

$10.0 \, ^{+0.4}_{-0.6}$

1.14Max

$1.52 \, ^{+0.25}_{-0.12}$

2.29

2.29

0.76 ± 0.12

⊕ 0.15 Ⓜ A

A

1   2   3

0.07 ± 0.07