



WT60P1

Digital Monitor Controller

Ver. 1.51 Jul-31-1998

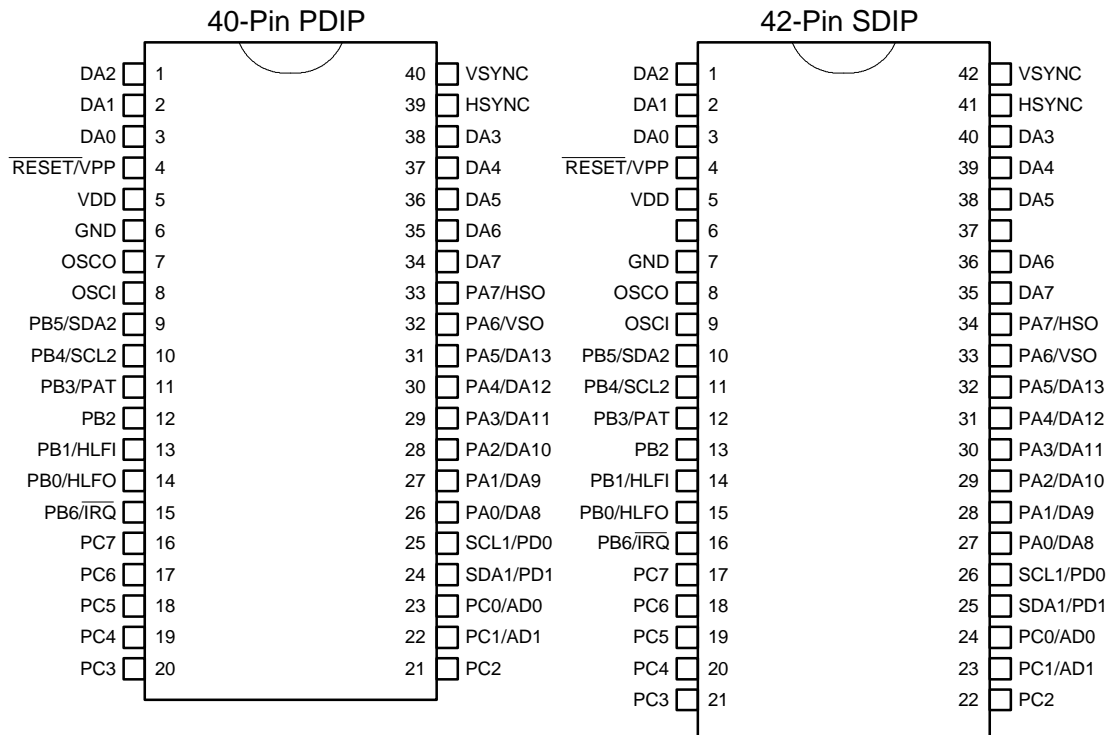
GENERAL DESCRIPTION

The WT60P1 is a MTP (Multiple-Time-Programmable) version of WT60xx microcontroller which is specially designed for digital controlled multi-sync monitor. It contains 8-bit CPU, 16K bytes flash memory, 288 bytes RAM, 14 PWMs, parallel I/O, SYNC processor, timer, one DDC interface (slave mode I²C interface with DDC1), one master/slave I²C interface, two 4-bit A/D converters and watch-dog timer.

FEATURES

- * 8-bit 6502 compatible CPU, 4MHz operating frequency
- * 16384 bytes flash memory, 288 bytes SRAM
- * 8MHz crystal oscillator
- * 14 channels 8-bit/62.5kHz PWM outputs (8 open drain outputs & 6 CMOS outputs)
- * Sync signal processor with H+V separation, frequency calculation, H/V polarity detection/control
- * Three free-running sync signal outputs for burn-in test (64kHz/62.5Hz, 48kHz/75Hz, 31kHz/60Hz)
- * Self-test pattern generator generates cross hatch picture
- * DDC interface supports VESA DDC1/DDC2B standard
- * Master/slave I²C interface
- * Watch-dog timer (0.524 second)
- * Maximum 25 programmable I/O pins
- * One 8-bit programmable timer
- * Two 4-bit A/D converter
- * One external interrupt request
- * Built-in low VDD voltage reset
- * +5V power supply

PIN CONFIGURATION



* I²C is a trademark of Philips Corporation.
 * DDC is a trademark of Video Electronics Standard Association (VESA).



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PIN DESCRIPTION

| Pin No. | Pin Name | I/O | Descriptions | |
|---------|----------|------------|--------------|---|
| 40 | 42 | | | |
| 1 | 1 | DA2 | O | D/A converter 2. Open-drain output. External applied voltage can up to 10V. |
| 2 | 2 | DA1 | O | D/A converter 1. Open-drain output. External applied voltage can up to 10V. |
| 3 | 3 | DA0 | O | D/A converter 0. Open-drain output. External applied voltage can up to 10V. |
| 4 | 4 | /RESET/VPP | I | Reset or Vpp. Active low reset input or Vpp for erase/write flash memory. |
| 5 | 5 | VDD | | Power supply (+5V). |
| 6 | 7 | GND | | Ground (0V). |
| 7 | 8 | OSCO | O | Oscillator Output. Connects a 8MHz crystal. |
| 8 | 9 | OSCI | I | Oscillator Input. Connects a 8MHz crystal. |
| 9 | 10 | PB5/SDA2 | I/O | I/O Port B5 or I²C data pin. This pin can be an I/O port or I ² C serial data pin. |
| 10 | 11 | PB4/SCL2 | I/O | I/O Port B4 or I²C clock pin. This pin can be I/O port or I ² C clock pin. |
| 11 | 12 | PB3/PAT | I/O | I/O Port B3 or self-test pattern output. When as an I/O port, it is same as PB5. When it is configured to test pattern output, a vedio signal is output. |
| 12 | 13 | PB2 | I/O | I/O Port B2. When it is an input pin, it has an internal pull-up resistor. When it is an output pin, the source/sink current is 5mA. |
| 13 | 14 | PB1/HLFI | I/O | I/O Port B1 or half frequency input. |
| 14 | 15 | PB0/HLFO | I/O | I/O Port B0 or half frequency output. |
| 15 | 16 | PB6/IRQ | I/O | I/O Port B6 or Interrupt Request. When as interrupt request input, it has an internal pull high resistor. When as an I/O port, it is same as PB3. |
| 16 | 17 | PC7 | I/O | I/O Port C7. When it is an input pin, it has an internal pull-up resistor. When it is an output pin, the sink current is 10mA and the source current is 5mA. |
| 17 | 18 | PC6 | I/O | I/O Port C6. Same as PC7. |
| 18 | 19 | PC5 | I/O | I/O Port C5. Same as PC7. |
| 19 | 20 | PC4 | I/O | I/O Port C4. Same as PC7. |
| 20 | 21 | PC3 | I/O | I/O Port C3. Same as PC7. |
| 21 | 22 | PC2 | I/O | I/O Port C2. Same as PC7. |
| 22 | 23 | PC1/AD1 | I/O | I/O Port C1 or A/D converter input 0. |
| 23 | 24 | PC0/AD0 | I/O | I/O Port C0 or A/D converter input 1. |
| 24 | 25 | SDA1/PD1 | I/O | DDC serial data or I/O Port D1. When it is a DDC interface pin, It is an open- drain output. When as an I/O port, it is same as Port B. |
| 25 | 26 | SCL1/PD0 | I/O | DDC serial clock or I/O Port D0. When it is a DDC interface pin, It is an open- drain output. When as an I/O port, it is same as Port B. |
| 26 | 27 | PA0/DA8 | I/O | I/O Port A0 or D/A converter 8. This pin can be the output of D/A converter 8 (source/sink = 5mA) or an I/O pin (source = -100uA, sink = 5mA). |
| 27 | 28 | PA1/DA9 | I/O | I/O Port A1 or D/A converter 9. Same as PA0/DA8. |
| 28 | 29 | PA2/DA10 | I/O | I/O Port A2 or D/A converter 10. Same as PA0/DA8. |
| 29 | 30 | PA3/DA11 | I/O | I/O Port A3 or D/A converter 11. Same as PA0/DA8. |
| 30 | 31 | PA4/DA12 | I/O | I/O Port A4 or D/A converter 12. Same as PA0/DA8. |
| 31 | 32 | PA5/DA13 | I/O | I/O Port A5 or D/A converter 13. Same as PA0/DA8. |
| 32 | 33 | PA6/VSO | I/O | I/O Port A6 / VSYNC OUT. This pin can be the output of VSYNC or an I/O pin. When as an I/O pin, it is same as PA0. |
| 33 | 34 | PA7/HSO | I/O | I/O Port A7 / HSYNC OUT. This pin can be the output of HSYNC or an I/O pin. When as an I/O pin, it is same as PA0. |
| 34 | 35 | DA7 | O | D/A converter 7. Open-drain output. External applied voltage can up to 10V. |
| 35 | 36 | DA6 | O | D/A converter 6. Open-drain output. External applied voltage can up to 10V. |
| 36 | 38 | DA5 | O | D/A converter 5. Open-drain output. External applied voltage can up to 10V. |
| 37 | 39 | DA4 | O | D/A converter 4. Open-drain output. External applied voltage can up to 10V. |
| 38 | 40 | DA3 | O | D/A converter 3. Open-drain output. External applied voltage can up to 10V. |
| 39 | 41 | HSYNC | I | HSYNC input. Schmitt trigger input. |
| 40 | 42 | VSYNC | I | VSYNC input. Schmitt trigger input. |



FUNCTIONAL DESCRIPTION

CPU

The CPU core is 6502 compatible, operating frequency is 4MHz. Address bus is 16-bit and data bus is 8-bit. the non-maskable interrupt (/NMI) of 6502 is changed to maskable interrupt and is defined as the INT0. The interrupt request (/IRQ) of 6502 is defined as the INT1.

Default stack pointer is 01FFH.

Please refer the 6502 reference menu for more detail.

ROM

16384 bytes flash memory are provided for program codes.

Address is located from C000H to FFFFH.

The following addresses are reserved for special purpose :

FFFAH (low byte) and FFFBH (high byte) : INT0 interrupt vector.

FFFCH (low byte) and FFFDH (high byte) : program reset vector.

FFFEH (low byte) and FFFFH (high byte) : INT1 interrupt vector.

RAM

Built-in 288 bytes SRAM, address is located from 0080H to 019FH. Because the initial stack pointer is 01FFH, so program must set proper stack pointer when program starts. A recommended value is 019FH.

Note : If user wants to emulate WT6014, please set bit 7 in REG#7FH. This will set stack pointer to 00FFH.

| | |
|------------------------------------|-----------|
| 0000H : 0020H | REGISTERS |
| 0021H : 007FH | Reserved |
| 0080H : 019FH | RAM |
| 01A0H : BFFFH | Reserved |
| C000H : : : : FFFFH | ROM |

Low VDD Voltage Reset

A VDD voltage detector is built inside the chip. When VDD is below 4.0 volts, the whole chip will be reset just like power-on-reset.

Note that the 4.0 volts varies with temperature and process. Please refer the electrical characteristics.



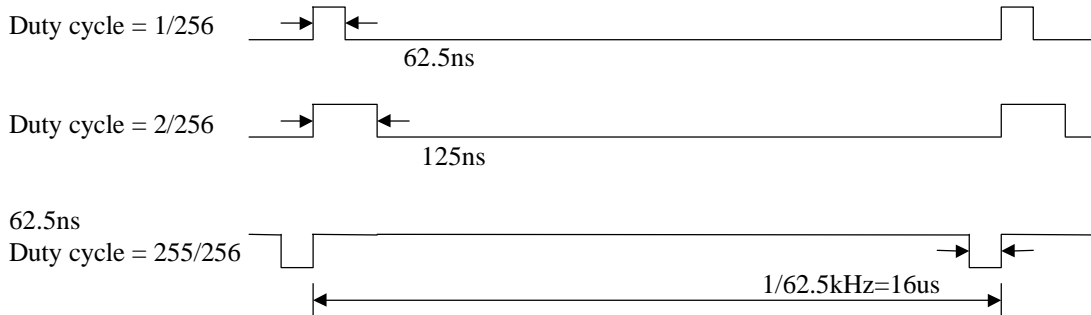
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PWM D/A Converter

The WT6018 provides 14 PWM D/A converters. DA0 to DA7 are open-drain outputs and external applied voltage on these pins can be up to 10 volts. DA8 to DA13 are 5 volts push-pull CMOS outputs and are shared with I/O Port PA0 to PA5. All D/A converters are 62.5kHz frequency with 8-bit resolution. Each D/A converter is controlled by the corresponding register (REG#00H to REG#0DH), the duty cycle can be programmed from 1/256 (data = 01H) to 255/256 (data = FFH).



To program the PWM D/A converters, write the corresponding registers (REG#00H to REG#0DH).

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 0000H | R/W | 80H | DA0 ₇ | DA0 ₆ | DA0 ₅ | DA0 ₄ | DA0 ₃ | DA0 ₂ | DA0 ₁ | DA0 ₀ |
| 0001H | R/W | 80H | DA1 ₇ | DA1 ₆ | DA1 ₅ | DA1 ₄ | DA1 ₃ | DA1 ₂ | DA1 ₁ | DA1 ₀ |
| 0002H | R/W | 80H | DA2 ₇ | DA2 ₆ | DA2 ₅ | DA2 ₄ | DA2 ₃ | DA2 ₂ | DA2 ₁ | DA2 ₀ |
| 0003H | R/W | 80H | DA3 ₇ | DA3 ₆ | DA3 ₅ | DA3 ₄ | DA3 ₃ | DA3 ₂ | DA3 ₁ | DA3 ₀ |
| 0004H | R/W | 80H | DA4 ₇ | DA4 ₆ | DA4 ₅ | DA4 ₄ | DA4 ₃ | DA4 ₂ | DA4 ₁ | DA4 ₀ |
| 0005H | R/W | 80H | DA5 ₇ | DA5 ₆ | DA5 ₅ | DA5 ₄ | DA5 ₃ | DA5 ₂ | DA5 ₁ | DA5 ₀ |
| 0006H | R/W | 80H | DA6 ₇ | DA6 ₆ | DA6 ₅ | DA6 ₄ | DA6 ₃ | DA6 ₂ | DA6 ₁ | DA6 ₀ |
| 0007H | R/W | 80H | DA7 ₇ | DA7 ₆ | DA7 ₅ | DA7 ₄ | DA7 ₃ | DA7 ₂ | DA7 ₁ | DA7 ₀ |
| 0008H | R/W | 80H | DA8 ₇ | DA8 ₆ | DA8 ₅ | DA8 ₄ | DA8 ₃ | DA8 ₂ | DA8 ₁ | DA8 ₀ |
| 0009H | R/W | 80H | DA9 ₇ | DA9 ₆ | DA9 ₅ | DA9 ₄ | DA9 ₃ | DA9 ₂ | DA9 ₁ | DA9 ₀ |
| 000AH | R/W | 80H | DA10 ₇ | DA10 ₆ | DA10 ₅ | DA10 ₄ | DA10 ₃ | DA10 ₂ | DA10 ₁ | DA10 ₀ |
| 000BH | R/W | 80H | DA11 ₇ | DA11 ₆ | DA11 ₅ | DA11 ₄ | DA11 ₃ | DA11 ₂ | DA11 ₁ | DA11 ₀ |
| 000CH | R/W | 80H | DA12 ₇ | DA12 ₆ | DA12 ₅ | DA12 ₄ | DA12 ₃ | DA12 ₂ | DA12 ₁ | DA12 ₀ |
| 000DH | R/W | 80H | DA13 ₇ | DA13 ₆ | DA13 ₅ | DA13 ₄ | DA13 ₃ | DA13 ₂ | DA13 ₁ | DA13 ₀ |

| Bit Name | Bit value |
|-----------|---|
| DAx7-DAx0 | 01H : 1/256 duty cycle 02H : 2/256 duty cycle 03H : 3/256 duty cycle : FFH : 255/256 duty cycle |

****Do not write 00H to the PWM registers. This will cause unstable output.**

I/O Ports

Port_A :

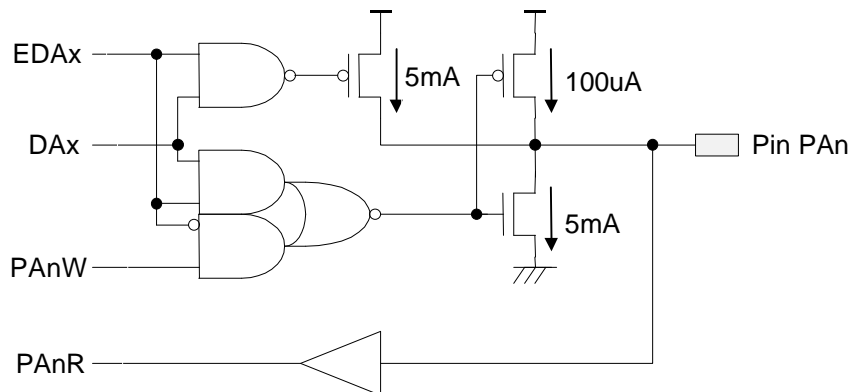
- Pin PA0/DA8 - general purpose I/O shared with DA8 output.
- Pin PA1/DA9 - general purpose I/O shared with DA9 output.
- Pin PA2/DA10 - general purpose I/O shared with DA10 output.
- Pin PA3/DA11 - general purpose I/O shared with DA11 output.
- Pin PA4/DA12 - general purpose I/O shared with DA12 output.
- Pin PA5/DA13 - general purpose I/O shared with DA13 output.
- Pin PA6/VSO - general purpose I/O shared with VSYNC output.
- Pin PA7/HSO - general purpose I/O shared with HSYNC output.

Port_A is controlled by REG#10H & REG#11H. In REG#10H, each corresponding bit enables HSYNC output, VSYNC output or D/A converter output when it is "1". If the corresponding bit is "0", the output level is decided by REG#11H. In REG#11H, if the I/O corresponding bit (PAn) is "0", the output is low level ($I_{OL}=5mA$). If PAn bit is "1", the output is high level ($I_{OH}= -100uA$) and can be used as an input.

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|------|------|-------|-------|-------|-------|------|------|
| 0010H | W | 00H | EHO | EVO | EDA13 | EDA12 | EDA11 | EDA10 | EDA9 | EDA8 |
| 0011H | W | FFH | PA7W | PA6W | PA5W | PA4W | PA3W | PA2W | PA1W | PA0W |
| 0011H | R | -- | PA7R | PA6R | PA5R | PA4R | PA3R | PA2R | PA1R | PA0R |

| Bit Name | Bit value = "1" | Bit value = "0" |
|-------------|--|--------------------------------------|
| EHO | Enable PA7 as HSYNC output. | PA7 as general purpose I/O. |
| EVO | Enable PA6 as VSYNC output. | PA6 as general purpose I/O. |
| EDA13 | Enable PA5 as DA13 output. | PA5 as general purpose I/O. |
| EDA12 | Enable PA4 as DA12 output. | PA4 as general purpose I/O. |
| EDA11 | Enable PA3 as DA11 output. | PA3 as general purpose I/O. |
| EDA10 | Enable PA2 as DA10 output. | PA2 as general purpose I/O. |
| EDA9 | Enable PA1 as DA9 output. | PA1 as general purpose I/O. |
| EDA8 | Enable PA0 as DA8 output. | PA0 as general purpose I/O. |
| PA7W - PA0W | Outputs high level ($I_{OH}= -100uA$). | Outputs low level ($I_{OL}= 5mA$). |
| PA7R- PA0R | Pin is high level. | Pin is low level. |

* If the program wants to force VSYNC output (VSO pin) in low state, write "0" to PA6 bit first, then write "0" to EVO bit. This is used to prevent high frequency output on VSO pin when the VSYNC frequency is increased to read EDID data in DDC1 mode.



Port_B :

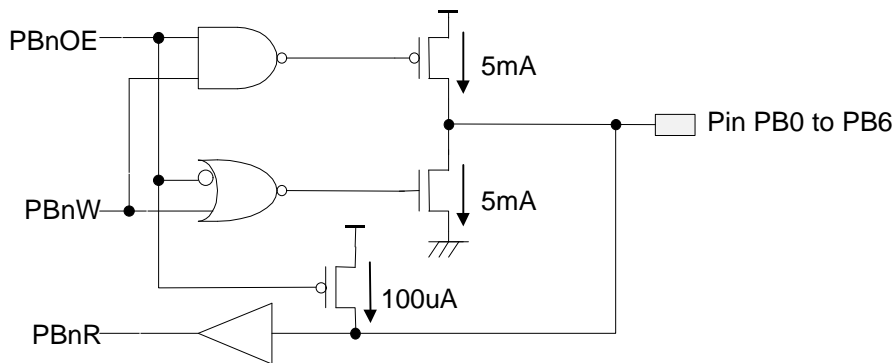
- Pin PB0/HLFO - general purpose I/O pin shared with half frequency output.
- Pin PB1/HLFI - general purpose I/O pin shared with half frequency output.
- Pin PB2 - general purpose I/O pin.
- Pin PB3/PAT - general purpose I/O pin shared with self-test pattern output.
- Pin PB4/SCL2 - general purpose I/O pin shared with I²C interface clock pin.
- Pin PB5/SDA2 - general purpose I/O pin shared with I²C interface data pin.
- Pin PB6/IRQB - general purpose I/O pin shared with interrupt request input.

The source/sink current of port_B is 5mA when as an output. When it is input, an internal pull high resistor is connected.

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|------|-------|-------|-------|-------|-------|-------|-------|
| 0012H | W | 00H | 0 | PB6OE | PB5OE | PB4OE | PB3OE | PB2OE | PB1OE | PB0OE |
| 0013H | W | FFH | 1 | PB6W | PB5W | PB4W | PB3W | PB2W | PB1W | PB0W |
| 0013H | R | -- | -- | PB6R | PB5R | PB4R | PB3R | PB2R | PB1R | PB0R |

| Bit Name | Bit value = "1" | Bit value = "0" |
|---------------|--|--|
| PB6OE - PB0OE | Output enable. | Output disable (internal pull-up). |
| PB6W - PB0W | Outputs high level (I _{OH} = -5mA). | Outputs low level (I _{OL} = 5mA). |
| PB6R- PB0R | Pin is high level. | Pin is low level. |

- * If IEN_D bit in REG#1AH is "1" and PB6OE bit is "0", the PB6 pin becomes interrupt request input.
- * If ENI2C bit in REG#1EH is "1", the PB5 and PB4 pins becomes I²C interface pins.
- * If ENPAT bit in REG#16H is "1", the PB3 pin becomes self-test pattern output.
- * If ENHALF bit in REG#17H is "1", the PB1 pin becomes half frequency input and PB0 pin becomes half frequency output pin.



Structure of Port B

Port_C :

Pin PC0 - general purpose I/O pin shared with 4-bit A/D converter 0 input.
 Pin PC1 - general purpose I/O pin shared with 4-bit A/D converter 1 input
 Pin PC2 to PC7 - general purpose I/O pins.
 The REG#14H defines the I/O direction and the REG#15H controls the output level.

The structure of Port_C is same as the Port_B except the sink current is 10mA. When PC0 and PC1 are programmed as the A/D converter inputs, the pull high transistor is disconnected.

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0014H | W | 00H | PC7OE | PC6OE | PC5OE | PC4OE | PC3OE | PC2OE | PC1OE | PC0OE |
| 0015H | W | FFH | PC7W | PC6W | PC5W | PC4W | PC3W | PC2W | PC1W | PC0W |
| 0015H | R | -- | PC7R | PC6R | PC5R | PC4R | PC3R | PC2R | PC1R | PC0R |

| Bit Name | Bit value = "1" | Bit value = "0" |
|---------------|--|---|
| PC7OE - PC0OE | Output enable. | Output disable (internal pull-up). |
| PC7W - PC0W | Outputs high level (I _{OH} = -5mA). | Outputs low level (I _{OL} = 10mA). |
| PC7R - PC0R | Pin is high level. | Pin is low level. |

Port_D :

Pin SCL1/PD0 - general purpose I/O pin shared with DDC interface serial clock.
 Pin SDA1/PD1 - general purpose I/O pin shared with DDC interface serial data.

The structure of these two pins are same as the PB4 and PB5. Default is DDC interface and can be changed to I/O port D by setting ENPD bit.

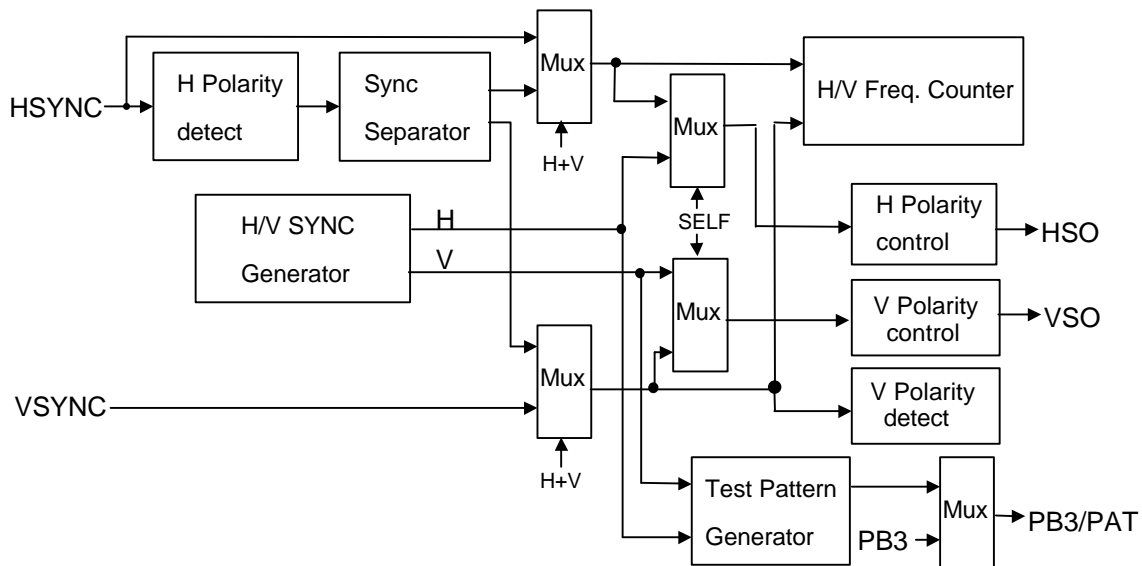
| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|------|------|------|------|-------|-------|------|------|
| 000FH | W | 00H | -- | -- | -- | ENPD | PD1OE | PD0OE | PD1W | PD0W |
| 000FH | R | -- | -- | -- | -- | -- | -- | -- | PD1R | PD0R |

| Bit Name | Bit value = "1" | Bit value = "0" |
|---------------|--|--|
| ENPD | Enable I/O Port_D. | DDC interface.(open drain) |
| PD1OE - PD0OE | Output enable. | Output disable (internal pull-up). |
| PD1W - PD0W | Outputs high level (I _{OH} = -5mA). | Outputs low level (I _{OL} = 5mA). |
| PD1R- PD0R | Pin is high level. | Pin is low level. |

* If program wants to read current status on the I/O pins (any I/O port), do not set output enable bit to "0". Because the registers for reading I/O are always indicating the current state on the I/O pins, set output enable bit to "0" will change the level on the I/O pin. Please reference the I/O pin structure.

SYNC Processor

The SYNC processor can : (1) separate the composite sync signal; (2) calculate HSYNC and VSYNC frequencies; (3) detect polarities of HSYNC and VSYNC inputs; (4) control the output polarities of HSO and VSO pins. (5) generate free-running horizontal and vertical sync signals for burn-in test; (6) generate self-test pattern signal.

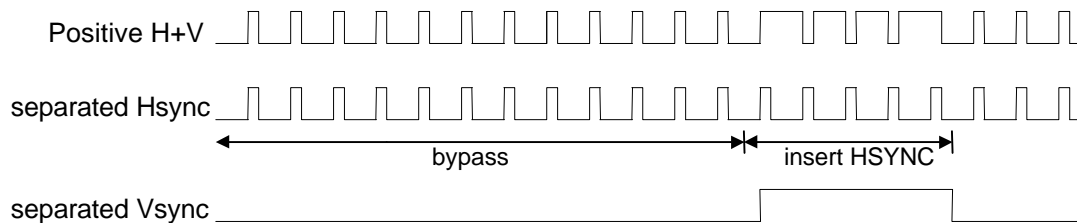


Composite Sync Signal Separation

The composite sync signal comes from HSYNC pin and is separated by the sync separator.

The operations of sync separator are:

- detect the polarity and convert composite sync signal to positive polarity.
- extract Vsync
 - Pulse width less than 8 μ s will be filtered, but the Vsync will be widened about 8 μ s.
- count the pulses during the separated Vsync is low and save the counter value (N_H).
- bypass the composite sync pulses before the counter equals to N_H .
- start inserting Hsync after the counter equals to N_H until the separated Vsync is low.
- the period of inserted Hsync is decided by the last two bypassed Hsync.
- the pulse width of the inserted Hsync is 2 μ s.



To decide whether the HSYNC input is a composite sync signal or not, program should check the frequency of VSYNC first (reset H+V bit to "0"). If the VSYNC frequency is lower than 15.25Hz (OVF2=1), set H+V bit to "1" and check VSYNC frequency again. If VSYNC still has no frequency, that is power saving condition, program should reset H+V bit. If it has a valid frequency, the HSYNC input is composite signal.

Frequency Calculation

Horizontal frequency and vertical frequencies calculation are done by using one 10-bit up counter. After power is on, the SYNC processor calculates the vertical frequency first (H/V bit = "0"). A 31.25KHz clock counts the time interval between two VSYNC pulses, then sets the FRDY bit and generates an INT1 interrupt (if IEN_S bit is "1"). The software can either use interrupt or polling the FRDY bit to read the correct vertical frequency. After reading the REG#16H, the FRDY bit is cleared to "0", counter is reset and H/V bit is set. The SYNC processor starts to count horizontal frequency. The horizontal frequency calculation is done by counting the HSYNC pulses in 8.192 ms. Like the vertical frequency, the horizontal frequency can be read when the FRDY bit is set or INT1 occurs. After reading the REG#16H, the FRDY, INT_S and H/V bits are cleared. The SYNC processor starts to calculate the vertical frequency again, and so on.

The relationships between counter value and frequency are :

$$\begin{aligned} \text{Hfreq} &= (\text{counter value} \times 122.07) \text{ Hz} \\ \text{Vfreq} &= (31250 / \text{counter value}) \text{ Hz} \end{aligned}$$

The frequency range :

$$\begin{aligned} \text{Hfreq range} &: 122.07 \text{ Hz to } 124.8 \text{ kHz} ; \text{ Resolution} : 122.07\text{Hz} \\ \text{Vfreq range} &: 30.5 \text{ Hz to } 31.25 \text{ kHz} \end{aligned}$$

If counter overflowed, the OVF1 bit will be set to "1". The counter keeps on counting until it overflowed again. The OVF2 bit and FRDY bit will be set when counter overflowed twice. This is designed for finding the vertical frequency bellows 15.25Hz. The program should check REG#17H before reading REG#16H.

Polarity Detect/Control

The polarities of HSYNC and VSYNC are automatically detected and are shown in the H_POL and V_POL bits. The polarities of HSO and VSO are controlled by the HOP and VOP bits. For example, set HOP bit to "1", the HSO pin always outputs positive horizontal sync signal, whatever the HSYNC input's polarity is.

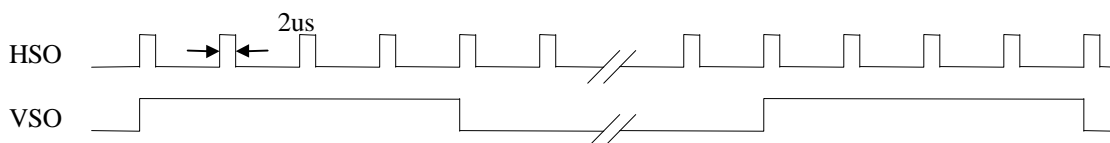
Free-running Sync Signal

The self-generated sync signals are output from HSO and VSO pins if SELF bit is "1". Three kinds of frequencies are provided :

- (1) Hfreq = 8MHz/125 = 64.0kHz, Vfreq = Hfreq/1024 = 62.5Hz.
- (2) Hfreq = 8MHz/167 = 47.9kHz, Vfreq = Hfreq/640 = 74.9Hz.
- (3) Hfreq = 8MHz/257 = 31.1kHz, Vfreq = Hfreq/512 = 60.8Hz .

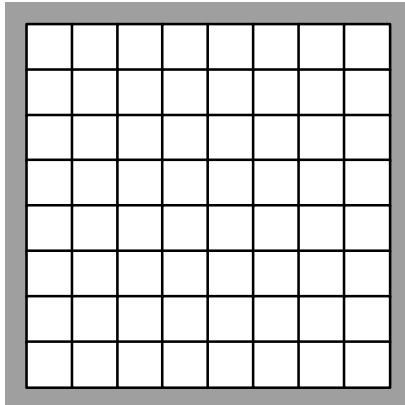
The output polarities are controlled by the HOP and VOP bits.

The pulse width of HSO is 2us and VSO is four HSO cycles. The timing relationship is shown in the following :

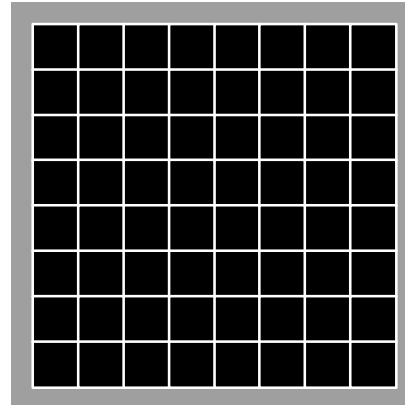


Test Pattern Generation

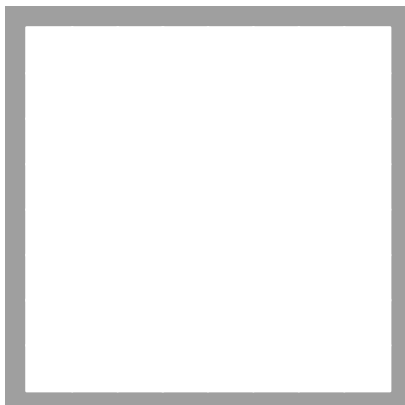
A self-test pattern signal comes out from pin PB3/PAT. It can generate a cross hatch picture, a inverted cross hatch picture, a white picture or a black picture.



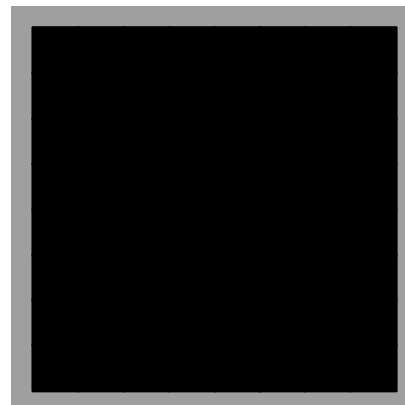
8 X 8 cross hatch



Inverted 8 X 8 cross hatch

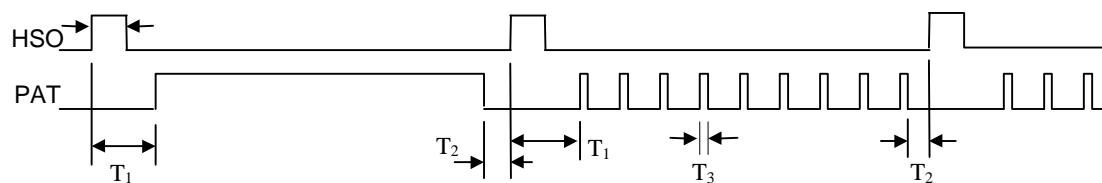


White Picture



Black Picture

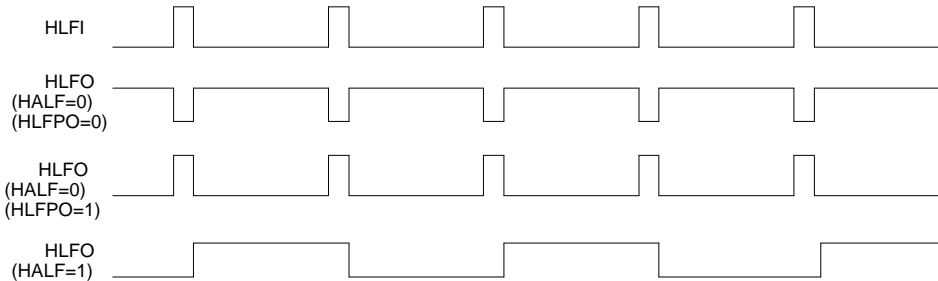
The test pattern signal is generated when SELF and ENPAT are both set to "1". This video signal will synchronize to the free-running Hsync and Vsync, no matter which frequency is chosen. The following diagram shows the timing relationship of cross hatch picture.



| HSO | VSO | T ₁ | T ₂ | T ₃ |
|---------|--------|----------------|----------------|----------------|
| 31.1kHz | 60.8Hz | 6us | 1us | 62.5ns |
| 47.9kHz | 74.9Hz | 5.125us | 0.625us | 62.5ns |
| 64kHz | 62.5Hz | 3.625us | 0.875us | 62.5ns |

Half Frequency

HLFO pin outputs same or half frequency from HLF1 pin. The divide-by-2 operation is done on the falling edge of HLF1 pin when HALF bit is set. Polarity of HLFO is specified by HLFPO bit.

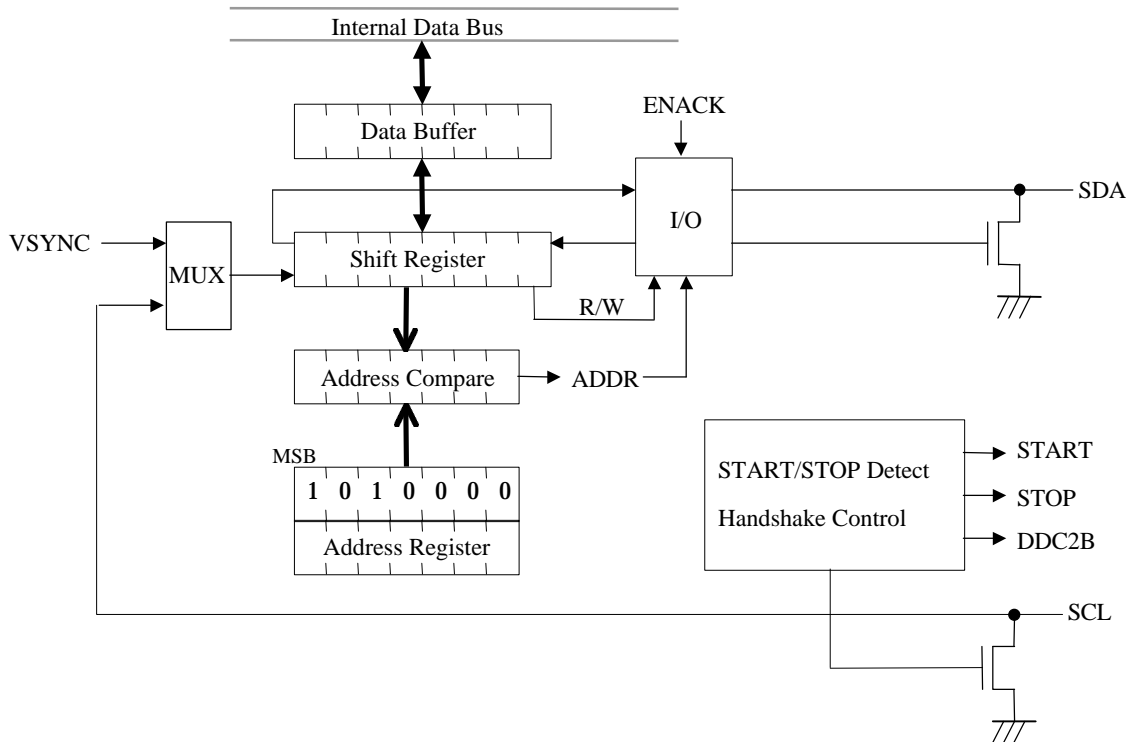


| | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|-----|---------|------|------|-------|-------|-------|------|------|------|
| 0016H | W | -- | 0 | 0 | ENPAT | PAT1 | PAT0 | SELF | H64K | H48K |
| 0016H | R | -- | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 |
| 0017H | W | -- | -- | -- | ENHLF | HALF | HLFPO | H+V | HOP | VOP |
| 0017H | R | 00H | H/V | -- | H_POL | V_POL | OVF2 | OVF1 | F1 | F0 |

| Bit Name | Bit value = "1" | Bit value = "0" |
|------------|--|--|
| ENPAT | Pin PB3/PAT outputs test pattern. | Pin PB3/PAT is I/O port. |
| PAT1,PAT0 | If PAT1=0, PAT0=0, cross hatch picture. If PAT1=0, PAT0=1, white picture. If PAT1=1, PAT0=0, inverted cross hatch picture. If PAT1=1, PAT0=1, black picture. | |
| SELF | HSO and VSO output free-running frequency. | HSO and VSO output sync signals. |
| H64K, H48K | H64K="1",H48K="1" : Burn-in frequency=47.9kHz/74.9Hz H64K="0",H48K="1" : Burn-in frequency=47.9kHz/74.9Hz H64K="1",H48K="0" : Burn-in frequency=64kHz/62.5Hz H64K="0",H48K="0" : Burn-in frequency=31.1kHz/60.8Hz | |
| ENHLF | Pin PB1/HLFI is frequency input. Pin PB0/HLFO is half frequency output. | Pin PB1/HLFI and PB0/HLFO is I/O port. |
| HALF | HLFO outputs half frequency of HLF1. | HLFO outputs same frequency of HLF1 |
| HLFPO | HLFO is positive polarity. | HLFO is negative polarity. |
| H+V | Enable H+V separation function. This will select the sync signals come from the sync separator. | Disable H+V separation. |
| HOP | HSO pin is always positive polarity. | HSO pin is always negative polarity. |
| VOP | VSO pin is always positive polarity. | VSO pin is always negative polarity. |
| H/V | Counter stores horizontal frequency. | Counter stores vertical frequency. |
| H_POL | HSYNC input is positive polarity. | HSYNC input is negative polarity. |
| V_POL | VSYNC input is positive polarity. | VSYNC input is negative polarity. |
| OVF2, OVF1 | OVF2="1",OVF1="0" : Counter overflowed twice. OVF2="0",OVF1="1" : Counter overflowed once. OVF2="0",OVF1="0" : No overflow. OVF2="1",OVF1="1" : No such condition. | |
| F9-F0 | Frequency counter value. (F9 is MSB) | |

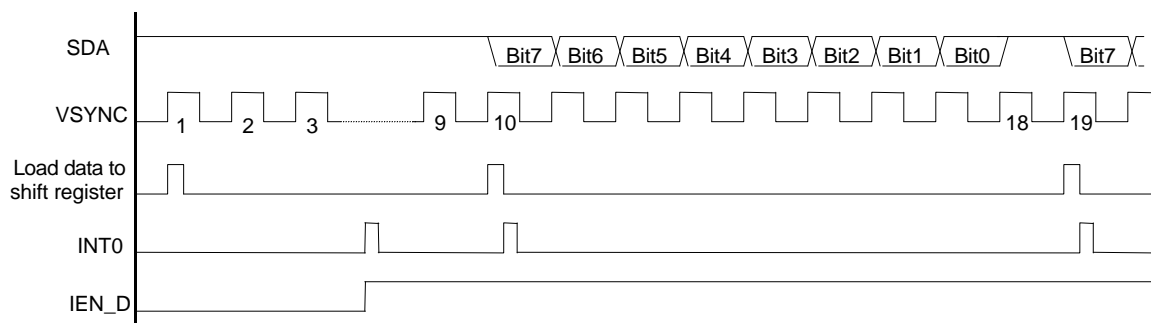
DDC Interface

The DDC interface is a slave mode I²C interface with DDC1 function. It is fully compatible with VEAS DDC1/2B standard. The functional block diagram is shown in the below.



After power on or reset the DDC interface, it is in DDC1 state. The shift register shifts out data to SDA pin on the rising edge of VSYNC clock. Data format is an 8-bit byte followed by a null bit. Most significant bit (MSB) is transmitted first. Every time when the ninth bit has been transmitted, the shift register will load a data byte from data buffer (REG#18H). After loading data to the shift register, the data buffer becomes empty and generates an INT0 interrupt. So the program must write one data byte into REG#18 every nine VSYNC clocks.

Since the default values of data buffer(REG#22) and shift register are FFH, the SDA pin outputs high level if no data had been written into data buffer after power on reset. When program finished initialization and set the IEN_D bit to "1", the INT0 will occur because the data buffer is empty. The INT0 service routine should check the DDC2B bit is "0" and then writes the first EDID data byte into data buffer. When the second INT0 occurs, the INT0 service routine writes the second EDID data byte into data buffer and so on.





If a low level occurs on the SCL pin in DDC1 state, the DDC interface will switch to DDC2B state immediately and set the DDC2B bit to "1". No interrupt will be generated. But, if there is no valid device address and it receives 128 VSYNC pulses while the SCL is high level, it will go back to DDC1 state automatically. If it receives a valid device address, it will lock into DDC2B state and disregard VSYNC.

In some case, program wants to go back DDC1 state, set RDDC bit in REG#1AH and reset it again. This operation resets the DDC interface to the initial condition.

When it is in DDC2B state, the VSYNC clock is disregarded and the communication protocol follows the DDC standard. The data format on SDA pin is:

| | | | | | | | | | |
|---|---------|-----|---|----------------|---|--|----------------|---|---|
| S | Address | R/W | A | D7,D6,...., D0 | A | | D7,D6,...., D0 | A | P |
|---|---------|-----|---|----------------|---|--|----------------|---|---|

- S : Start condition. A falling edge occurs when SCL is high level.
- P : Stop condition. A rising edge occurs when SCL is high level.
- A : Acknowledge bit. "0" means acknowledge and "1" means non-acknowledge.
- Address : 7-bit device address.
- R/W : Read/Write control bit, "1" is read and "0" is write.
- D7,D6,...., D0 : data byte.

The hardware operations in DDC2B state are :

(1) *START/STOP detection*

When the START condition is detected, the DDC interface is enabled and set START bit to "1". When the STOP condition is detected, the DDC interface is disabled, set STOP bit to "1" and generate INTO interrupt.

- The START bit is cleared when the following data byte received.
- The STOP bit is cleared after writing REG#19H.

(2) *Address Recognition*

It contains two device addresses in WT6018. One fixed address ('1010000') is for EDID reading and one programmable address (REG#19H) is for external control, such as auto alignment.

- If the address is equal to "1010000", set ADDR bit to "0".
- If the address is equal to the bit A6 to bit A0 (REG#19H), set ADDR bit to "1".
- If the address is not equal to anyone above, the DDC interface will not response acknowledge.
- The ADDR bit is updated when a new device address is received.

(3) *Store R/W bit and decide the direction of SDA pin*

The R/W bit on the SDA pin will be stored in the RW bit.

(4) *Acknowledge bit control/detection*

- Acknowledge bit control in receive direction :
 - If ENACK=1 and address compare is true, response acknowledge (Acknowledge bit ="0").
 - If ENACK=0 or address compare is false, response non-acknowledge (Acknowledge bit ="1").

- Acknowledge bit detect in transmit direction :
 - If the acknowledge bit is "1", the DDC interface will be disabled and release the SDA pin.
 - If the acknowledge bit is "0", the DDC interface keeps on communicating.



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(5) *Data bytes transmit/receive*

If the RW bit is "1", the shift register will load data from the data buffer (REG#18H) before the data byte is transmitted and shift out data to the SDA pin before the rising edge of the SCL clock.

If the RW bit is "0", the shift register will shift in data on the rising edge of the SCL clock and the whole data byte is latched to the data buffer(REG#18H).

(6) *Handshaking procedure*

The handshaking is done on the byte level. The DDC interface will hold the SCL pin low after the acknowledge bit automatically. The bus master will be forced to wait until the WT6018 is ready for the next byte transfer. To release the SCL pin, write REG#19H will release clear the wait state.

(7) *Interrupt INTO*

The DDC interface interrupt is enabled by setting the IEN_D bit in the REG#1AH.

Interrupt INTO occurs when:

- Transmit buffer empty in DDC1 state.
The INTO occurs when the shift register load data from data buffer.
Write REG#18H will clear the transmit buffer empty condition.
- Acknowledge is detected in DDC2B state.

The INTO occurs on the falling edge of the SCL clock after the acknowledge had been detected.

The SCL pin will be pulled low to force the bus master to wait until the service routine write REG#19H.

- STOP condition occurs in DDC2B mode

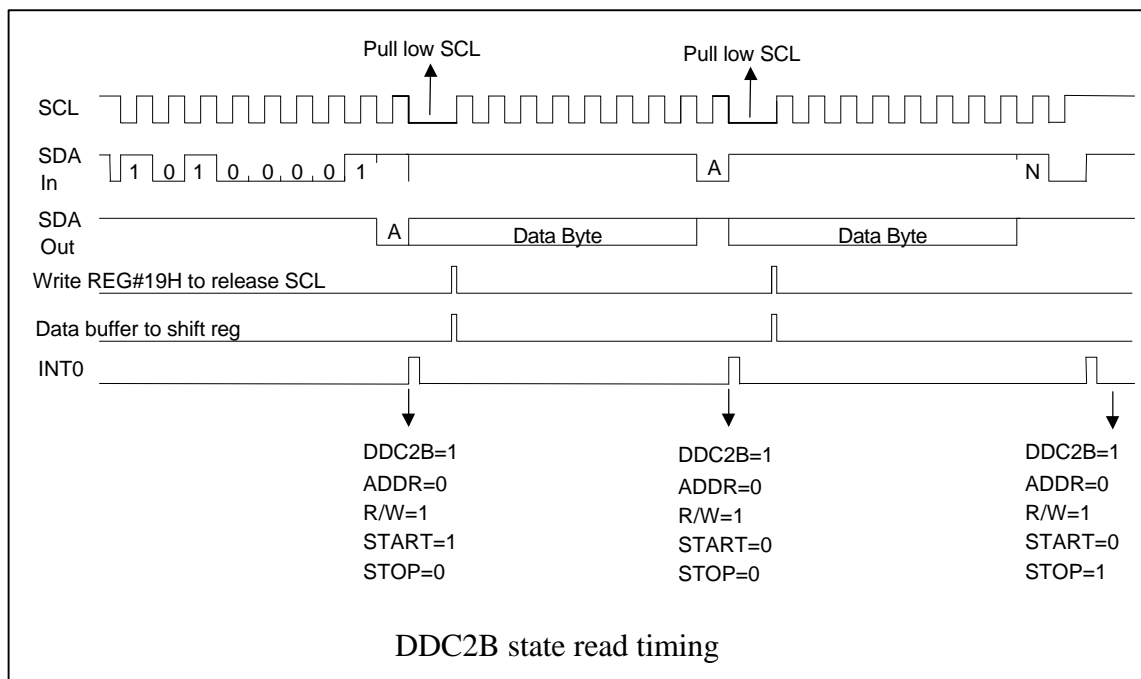
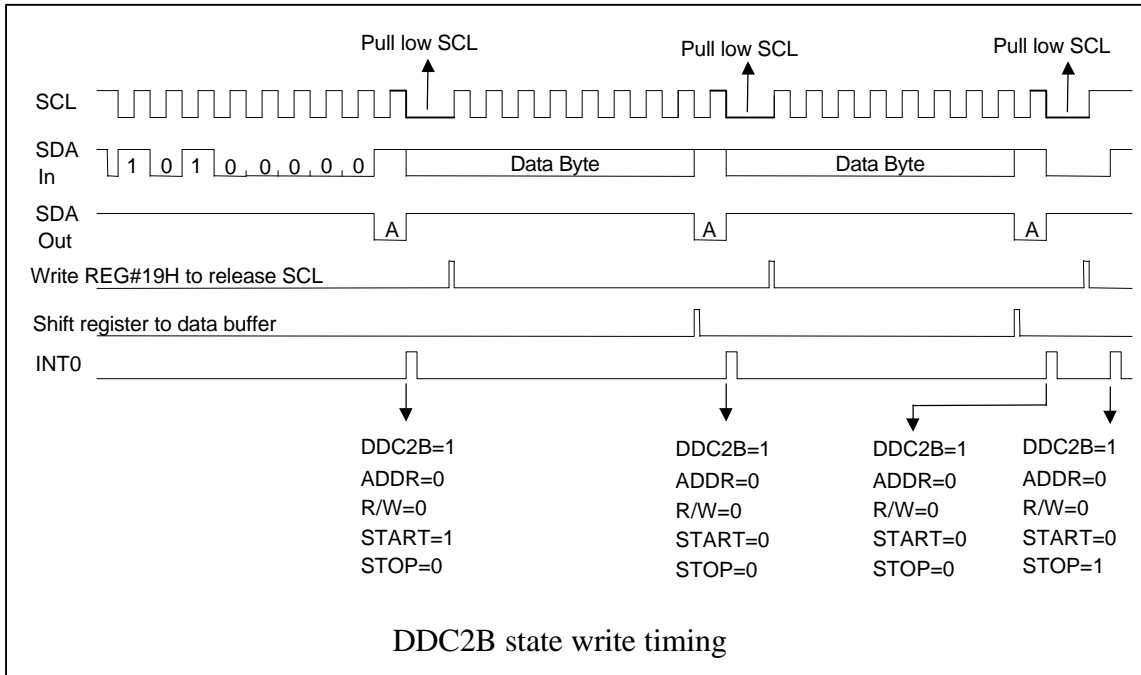
| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|-------|------|------|-------|------|------|------|-------|
| 0018H | R/W | FFH | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0019H | R | 40H | DDC2B | ADDR | RW | START | STOP | -- | -- | -- |
| 0019H | W | A0H | A6 | A5 | A4 | A3 | A2 | A1 | A0 | ENACK |

| Bit Name | Bit value = "1" | Bit value = "0" |
|----------------|---|---------------------------------------|
| DDC2B | DDC2B state. | DDC1 state. |
| ADDR | received address equals to the address in REG#19H(W). | received address equals to '1010000'. |
| RW | received R/W bit is '1'. | received R/W bit is '0'. |
| START | START condition is detected. | No START condition is detected. |
| STOP | STOP condition is detected. | No STOP condition is detected. |
| ENACK | Enable acknowledge. | Disable acknowledge. |
| A6,A5, ..., A0 | 7-bit slave address | |
| D7,D6, ..., D0 | Data to be transmitted or received data. | |



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I²C Interface

This is a master/slave mode I²C interface. In slave mode, the structure is same as the DDC2B mode of DDC interface.

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|------|------|------|-------|------|-------|------|-------|
| 001DH | R/W | FFH | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | D0 |
| 001EH | W | 00H | IA6 | IA5 | IA4 | IA3 | IA2 | IA1 | IA0 | ENADR |
| 001FH | R | -- | MS | ACK | BB | AL | RW | START | -- | -- |
| 001FH | W | 00H | MSS | MACK | CLK | ENI2C | 0 | 0 | 0 | 0 |

| Bit Name | Bit value = "1" | Bit value = "0" |
|------------------|---|--|
| MS | I ² C interface is in master mode. | I ² C interface is in slave mode. |
| ACK | Received Acknowledge bit is "1". | Received Acknowledge bit is "0". |
| BB | Bus busy. | Bus idle. |
| AL | Arbitration loss. | Arbitration success. |
| RW | Received R/W bit is "1". | Received R/W bit is "0". |
| START | START condition is detected. | No START condition is detected. |
| ENADR | Enable address compare. | No address compare. |
| MSS | Set master mode. If this bit is from 0→1, it will send START. | Set slave mode. If this bit is from 1→0, it will send a STOP. |
| MACK | Master send acknowledge. | Master send non-acknowledge. |
| CLK | SCL2 pin clock frequency is 996Hz. | SCL2 pin clock frequency is 62.5kHz. |
| ENI2C | Enable I ² C interface. | Disable I ² C interface. These two pins become I/O pins and reset I ² C interface. |
| IA6,IA5, ...,IA0 | 7-bit device address of I ² C interface. | |
| ID7,ID6, ...,ID0 | Data to be transmitted(W) or received data(R). | |

Write data to register \$001EH will send out clock for receive or transmit one data byte.

Interrupt Control

There are two interrupt sources : INT0 and INT1. INT0 has the higher priority.

Interrupt vector :

INT0 : FFFAH (low byte) and FFFBH (high byte).

INT1 : FFFEH (low byte) and FFFFH (high byte).

INT0 occurs when :

(1) data buffer empty in the DDC1 mode (DDC="1" and DDC2B="0").

(2) acknowledge or STOP condition is detected in the DDC2B mode (DDC="1" and DDC2B="0").

INT1 occurs when :

(1) a falling edge or a low level occurs on the /IRQ pin (EXT="1").

(2) the timer is time out (TIM="1").

(3) SYNC processor has a valid frequency (SYNC="1").

If H/V ="0" , it is vertical frequency ready.

If H/V ="1" , it is horizontal frequency ready.

(4) I²C interface interrupt.

INT0 is cleared when :

(1) writing the REG#18H in DDC1 state.

(2) writing the REG#19H in DDC2B state.

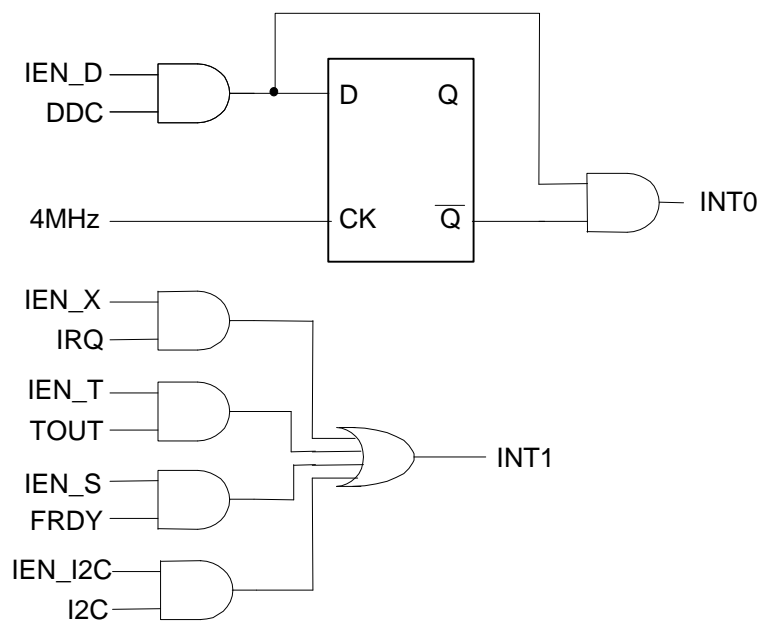
INT1 is cleared when :

(1) reading the REG#1AH if EXT="1".

(2) reading the REG#1BH if TIM="1".

(3) reading the REG#16H if SYNC="1".

(4) writing the REG#1EH if I2C="1".





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| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|-------|-------|-------|-------|------|------|------|---------|
| 001AH | W | 00H | IEN_X | IEN_T | IEN_S | IEN_D | EDGE | RDDC | 0 | IEN_I2C |
| 001AH | R | 00H | EXT | TIM | SYNC | DDC | IRQ | TOUT | FRDY | I2C |

| Bit Name | Bit value = "1" | Bit value = "0" |
|----------|---|--|
| IEN_X | Enable /IRQ pin interrupt. | Disable /IRQ pin interrupt. |
| IEN_T | Enable timer interrupt. | Disable timer interrupt. |
| IEN_S | Enable SYNC processor interrupt. | Disable SYNC processor interrupt. |
| IEN_D | Enable DDC interface interrupt. | Disable DDC interface interrupt. |
| EDGE | /IRQ pin interrupt is edge trigger. | /IRQ pin interrupt is level trigger. |
| RDDC | Reset DDC interface. It will always reset DDC interface if this bit keeps "1". | Clear the reset of DDC interface. |
| IEN_I2C | Enable I ² C interface interrupt. | Disable I ² C interface interrupt. |
| EXT | /IRQ pin interrupt occurs. | No /IRQ pin interrupt. |
| TIM | Timer interrupt occurs. | No timer interrupt. |
| SYNC | SYNC processor interrupt occurs. | No SYNC processor interrupt. |
| DDC | DDC interface interrupt occurs. | No DDC interface interrupt. |
| IRQ | /IRQ pin is low level | /IRQ pin is high level |
| TOUT | Timer is time-out. | Timer is not time-out. |
| FRDY | H/V frequency counter is ready. The counter value is valid. | H/V frequency counter is not ready. The counter value is invalid. |
| I2C | I ² C interface interrupt occurs. | No I ² C interface interrupt. |



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Timer

It is a 8-bit down counter and clock frequency is 976.5625Hz (period=1.024ms). The timer is started by writing a value into REG#1BH. When the timer counts down to zero, the timer stops, sets the TOUT bit and generates an INT1 interrupt (if the IEN_T bit is "1"). The TOUT bit will be cleared after REG#1BH is read.

Watch-Dog Timer

The watch-dog timer is enabled after the power is on. Software must clear the watch-dog timer within every 524ms. If the watch-dog timer expired, It will cause the whole chip reset just like external reset. If user want to disable the watch-dog timer when debugging program, set bit 6 of REG#7FH. But user must remember that the watch-dog timer is always enabled in mask-rom type IC.

To clear the watch-dog timer, write any data to REG#1CH.

| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|-------|------|------|------|------|------|------|------|
| 001BH | R/W | -- | TM7 | TM6 | TM5 | TM4 | TM3 | TM2 | TM1 | TM0 |
| 001CH | W | -- | WDT | WDT | WDT | WDT | WDT | WDT | WDT | WDT |
| 007FH | W | 00H | SET14 | DWDT | -- | -- | -- | -- | -- | -- |

| Bit Name | Bit value = "1" | Bit value = "0" |
|------------|---|-------------------------|
| TM7 to TM0 | Timer value (0 - 255) | |
| WDT | Write any value to this register will reset the watchdog timer. | |
| SET14 | Ser to WT6014. Page 1 mapping to page 0. So the stack pointer is 00FFH. | No memory mapping. |
| DWDT | Disable watch-dog timer. | Enable watch-dog timer. |



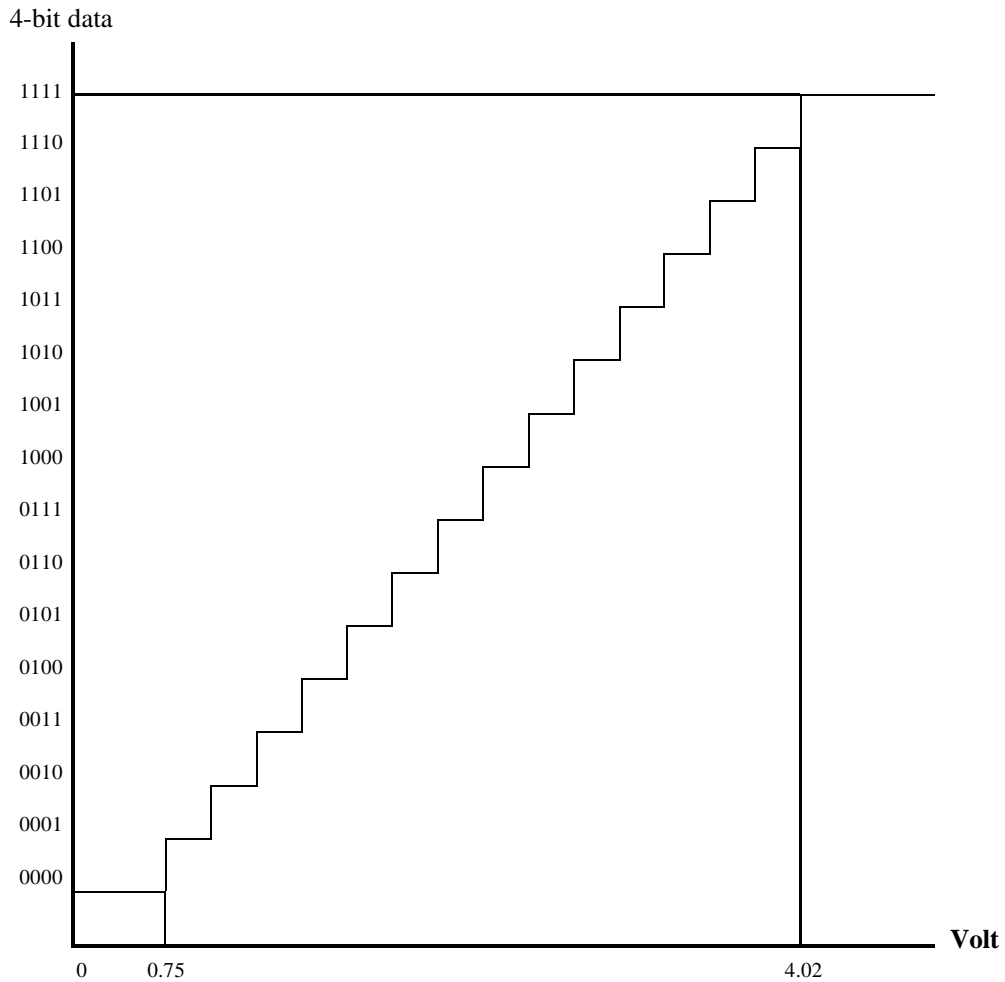
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A/D Converter

Two 4-bit A/D converter inputs are shared with I/O port_C PC0 and PC1. Use ENAD1 bit and ENAD0 bit to enable the corresponding A/D converter. The sampling rate is 488.3Hz and converted value is store in REG#20H.



| Address | R/W | Initial | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|-----|---------|------|------|------|------|------|------|-------|-------|
| 0020H | R | -- | AD13 | AD12 | AD11 | AD10 | AD03 | AD02 | AD01 | AD00 |
| 0020H | W | 00H | 0 | 0 | 0 | 0 | 0 | 0 | ENAD1 | ENAD0 |

| Bit Name | Bit value = "1" | Bit value = "0" |
|--------------|---|---|
| ENAD1 | Enable A/D converter 1. Pin PC1 is the input of A/D converter 1. | Disable A/D converter 1. Pin PC1 is I/O. |
| ENAD0 | Enable A/D converter 0. Pin PC0 is the input of A/D converter 0. | Disable A/D converter 0. Pin PC0 is I/O. |
| AD13,..,AD10 | 4-bit data of A/D converter 1. | |
| AD03,..,AD00 | 4-bit data of A/D converter 0. | |

REGISTER MAP

| Address | R/W | Initial value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|----------|---------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 0000H | R/W | 80H | DA0 ₇ | DA0 ₆ | DA0 ₅ | DA0 ₄ | DA0 ₃ | DA0 ₂ | DA0 ₁ | DA0 ₀ |
| 0001H | R/W | 80H | DA1 ₇ | DA1 ₆ | DA1 ₅ | DA1 ₄ | DA1 ₃ | DA1 ₂ | DA1 ₁ | DA1 ₀ |
| 0002H | R/W | 80H | DA2 ₇ | DA2 ₆ | DA2 ₅ | DA2 ₄ | DA2 ₃ | DA2 ₂ | DA2 ₁ | DA2 ₀ |
| 0003H | R/W | 80H | DA3 ₇ | DA3 ₆ | DA3 ₅ | DA3 ₄ | DA3 ₃ | DA3 ₂ | DA3 ₁ | DA3 ₀ |
| 0004H | R/W | 80H | DA4 ₇ | DA4 ₆ | DA4 ₅ | DA4 ₄ | DA4 ₃ | DA4 ₂ | DA4 ₁ | DA4 ₀ |
| 0005H | R/W | 80H | DA5 ₇ | DA5 ₆ | DA5 ₅ | DA5 ₄ | DA5 ₃ | DA5 ₂ | DA5 ₁ | DA5 ₀ |
| 0006H | R/W | 80H | DA6 ₇ | DA6 ₆ | DA6 ₅ | DA6 ₄ | DA6 ₃ | DA6 ₂ | DA6 ₁ | DA6 ₀ |
| 0007H | R/W | 80H | DA7 ₇ | DA7 ₆ | DA7 ₅ | DA7 ₄ | DA7 ₃ | DA7 ₂ | DA7 ₁ | DA7 ₀ |
| 0008H | R/W | 80H | DA8 ₇ | DA8 ₆ | DA8 ₅ | DA8 ₄ | DA8 ₃ | DA8 ₂ | DA8 ₁ | DA8 ₀ |
| 0009H | R/W | 80H | DA9 ₇ | DA9 ₆ | DA9 ₅ | DA9 ₄ | DA9 ₃ | DA9 ₂ | DA9 ₁ | DA9 ₀ |
| 000AH | R/W | 80H | DA10 ₇ | DA10 ₆ | DA10 ₅ | DA10 ₄ | DA10 ₃ | DA10 ₂ | DA10 ₁ | DA10 ₀ |
| 000BH | R/W | 80H | DA11 ₇ | DA11 ₆ | DA11 ₅ | DA11 ₄ | DA11 ₃ | DA11 ₂ | DA11 ₁ | DA11 ₀ |
| 000CH | R/W | 80H | DA12 ₇ | DA12 ₆ | DA12 ₅ | DA12 ₄ | DA12 ₃ | DA12 ₂ | DA12 ₁ | DA12 ₀ |
| 000DH | R/W | 80H | DA13 ₇ | DA13 ₆ | DA13 ₅ | DA13 ₄ | DA13 ₃ | DA13 ₂ | DA13 ₁ | DA13 ₀ |
| 000EH | Reserved | | | | | | | | | |
| 000FH | R | X | -- | -- | -- | -- | -- | -- | PD1R | PD0R |
| | W | 00H | 0 | 0 | 0 | ENPD | PD1OE | PD0OE | PD1W | PD0W |
| 0010H | W | 00H | EHO | EVO | EDA13 | EDA12 | EDA11 | EDA10 | EDA9 | EDA8 |
| 0011H | R | X | PA7R | PA6R | PA5R | PA4R | PA3R | PA2R | PA1R | PA0R |
| | W | FFH | PA7W | PA6W | PA5W | PA4W | PA3W | PA2W | PA1W | PA0W |
| 0012H | W | 00H | 0 | PB6OE | PB5OE | PB4OE | PB3OE | PB2OE | PB1OE | PB0OE |
| 0013H | R | X | -- | PB6R | PB5R | PB4R | PB3R | PB2R | PB1R | PB0R |
| | W | FFH | 1 | PB6W | PB5W | PB4W | PB3W | PB2W | PB1W | PB0W |
| 0014H | W | 00H | PC7OE | PC6OE | PC5OE | PC4OE | PC3OE | PC2OE | PC1OE | PC0OE |
| 0015H | R | FFH | PC7R | PC6R | PC5R | PC4R | PC3R | PC2R | PC1R | PC0R |
| | W | X | PC7W | PC6W | PC5W | PC4W | PC3W | PC2W | PC1W | PC0W |
| 0016H | R | X | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 |
| | W | 00H | 0 | 0 | ENPAT | PAT1 | PAT0 | SELF | H62K | H48K |
| 0017H | R | 00H | H/V | -- | H_POL | V_POL | OVF2 | OVF1 | F1 | F0 |
| | W | X | 0 | 0 | ENHLF | HALF | HLFPO | H+V | HOP | VOP |
| 0018H | R/W | FFH | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0019H | R | 40H | DDC2B | ADDR | RW | START | STOP | -- | -- | -- |
| | W | A0H | A6 | A5 | A4 | A3 | A2 | A1 | A0 | ENACK |
| 001AH | R | 00H | EXT | TIM | SYNC | DDC | IRQ | TOUT | FRDY | I2C |
| | W | 00H | IEN_X | IEN_T | IEN_S | IEN_D | EDGE | RDDC | 0 | IEN_I2C |
| 001BH | R/W | X | TM7 | TM6 | TM5 | TM4 | TM3 | TM2 | TM1 | TM0 |
| 001CH | W | X | CWDT | CWDT | CWDT | CWDT | CWDT | CWDT | CWDT | CWDT |
| 001DH | R/W | FFH | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | D0 |
| 001EH | W | 00H | IA6 | IA5 | IA4 | IA3 | IA2 | IA1 | IA0 | ENI2C |
| 001FH | R | -- | MS | ACK | BB | AL | RW | START | -- | -- |
| 001FH | W | 00H | MSS | MACK | CLK | ENI2C | 0 | 0 | 0 | 0 |
| 0020H | R | X | AD13 | AD12 | AD11 | AD10 | AD03 | AD02 | AD01 | AD00 |
| | W | 00H | 0 | 0 | 0 | 0 | 0 | 0 | ENAD1 | ENAD0 |
| 007FH | W | 00H | SET14 | DWDT | -- | -- | -- | -- | -- | -- |

X : No default value.

-- : No function.

0 : Must write 0.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Min. | Max | Units |
|---|------|---------|-------|
| DC Supply Voltage (VDD) | -0.3 | 7.0 | V |
| Input and output voltage with respect to Ground | | | |
| All pins except DA0 to DA7 | -0.3 | VDD+0.3 | V |
| DA0 to DA7 | -0.3 | 11.5V | V |
| Storage temperature | -20 | 125 | °C |
| Ambient temperature with power applied | -10 | 70 | °C |

* Note : Stresses above those listed may cause permanent damage to the device.

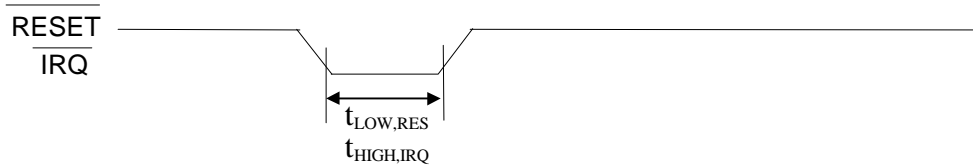
D.C. Characteristics (VDD=5.0V ± 5% , Ta=0 - 70 °C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------------------|-------------------------|---|------|------|---------|-------|
| V _{DD} | Supply Voltage | | 4.0 | 5 | 5.5 | V |
| V _{IH} | Input High Voltage | All input pins (except HSYNC and VSYNC) | 3.0 | - | VDD+0.3 | V |
| V _{IL} | Input Low Voltage | All input pins (except HSYNC and VSYNC) | -0.3 | - | 1.5 | V |
| V _{SIH} | Sync Input High Voltage | HSYNC and VSYNC pin | 2.0 | - | VDD+0.3 | V |
| V _{SIL} | Sync Input Low Voltage | HSYNC and VSYNC pin | -0.3 | - | 0.8 | V |
| V _{OH} | Output High Voltage | I _{OH} = -100uA PA0-PA7 pins | 3.5 | - | - | V |
| | | I _{OH} = -6mA PB0-PB6, PC0-PC7, PD0, PD1, DA8-DA13, HSO, VSO and HSO pins | 3.5 | - | - | V |
| | | DA0-DA7 pins (external voltage) | - | - | 10.5 | V |
| | | SCL and SDA pins (open drain) | - | - | 5.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 5mA PA0-PA7, PB0-PB6, PD0-1, DA0-DA13, SCL, SDA, VSO and HSO pins | - | - | 0.4 | V |
| | | I _{OL} = 10mA PC0-PC7 pins | - | - | 0.4 | V |
| I _{IL} | Input Leakage Current | SDA, SCL, HSYNC and VSYNC pins (V _{IN} = 0 to 5V) | -10 | - | 10 | uA |
| R _{PH} | Pull High Resistance | V _{IN} =0.8V PA0-PA7, PB0-PB6, PC0-PC7, /RESET and /IRQ pins | 16 | 22 | 28 | Kohm |
| I _{DD} | Operating Current | No load. Oscillator frequency=8MHz | - | 13 | 25 | mA |
| V _{RESET} | Reset Voltage | /RESET pin | 3.8 | 4.0 | 4.2 | V |

A.C. Characteristics (VDD=5.0V ± 5%, fosc=8MHz, Ta=0 - 70°C)

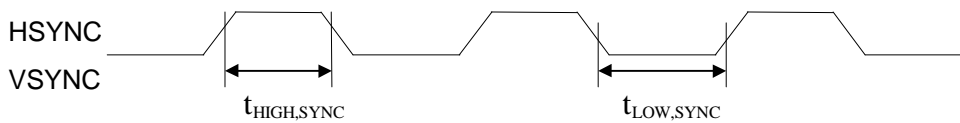
RESET and IRQ Timing

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---------------|--------------------------------|------|------|------|-------|
| $t_{LOW,RES}$ | /RESET pin low pulse | 250 | - | - | ns |
| $t_{LOW,IRQ}$ | /IRQ low pulse (level trigger) | 250 | - | - | ns |



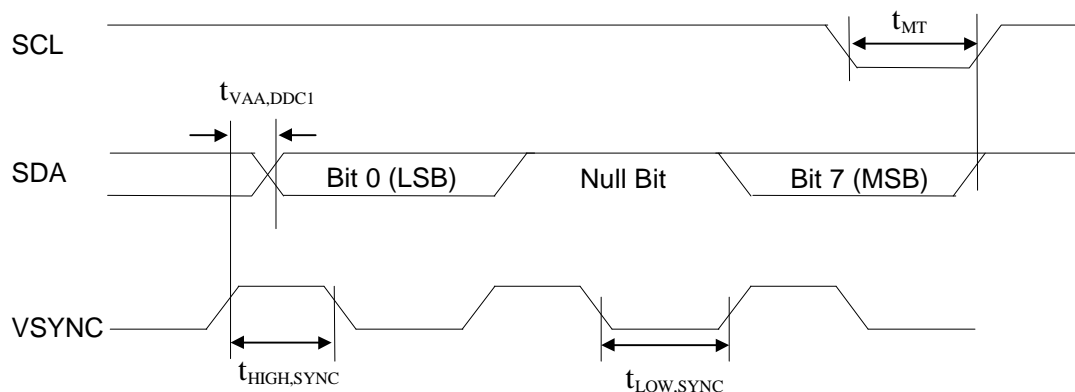
SYNC Processor Timing

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------------|---|----------------|------|------|-------|
| $t_{HIGH,SYNC}$ | HSYNC and VSYNC high time | 250 | - | - | ns |
| $t_{LOW,SYNC}$ | HSYNC and VSYNC low time | 250 | - | - | ns |
| $t_{FPW,H50}$ | Self generated free-running H50 pulse width | - | 2 | - | us |
| $t_{FPW,V50}$ | Self generated free-running V50 pulse width | 4 x H50 period | | | |
| $t_{IPW,H50}$ | Inserted Hsync pulse width (composite sync input) | - | 2 | - | us |



DDC1 Timing

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|----------------|---|------|------|------|-------|
| $t_{VAA,DDC1}$ | SDA output valid from VSYNC rising edge | 125 | - | 500 | ns |
| t_{MT} | Mode transition time (DDC1 to DDC2B) | - | - | 500 | ns |



DDC2B Timing

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|----------------|---------------------------------|------|------|------|-------|
| f_{SCL} | SCL input clock frequency | 0 | - | 100 | kHz |
| t_{BF} | Bus free time | 2 | - | - | us |
| $t_{HD,START}$ | Hold time for START condition | 1 | - | - | us |
| $t_{SU,START}$ | Set-up time for START condition | 1 | - | - | us |
| $t_{HIGH,SCL}$ | SCL clock high time | 1 | - | - | us |
| $t_{LOW,SCL}$ | SCL clock low time | 1 | - | - | us |
| $t_{HD,DATA}$ | Hold time for DATA input | 0 | - | - | ns |
| | Hold time for DATA output | 250 | - | - | ns |
| $t_{SU,DATA}$ | Set-up time for DATA input | 250 | - | - | ns |
| | Set-up time for DATA output | 500 | - | - | ns |
| t_{RISE} | SCL and SDA rise time | - | - | 1 | us |
| t_{FALL} | SCL and SDA fall time | - | - | 300 | ns |
| $t_{SU,STOP}$ | Set-up time for STOP condition | 4 | - | - | us |

