freescale
飞思卡尔(深圳)功率半导体有限公司

AOD409/AOI409

P-Channel Enhancement Mode Field Effect Transistor

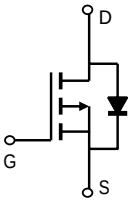
General Description

The AOD/I409 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

Features

V_{DS} (V) = -60V
I_D = -26A (V_{GS} = -10V)
$R_{DS(ON)}$ < 40mΩ (V_{GS} = -10V) @ -20A
$R_{DS(ON)}$ < 55mΩ (V_{GS} = -4.5V)

Green Product



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	-26	A
	T_C=100°C		-18	
Pulsed Drain Current [C]		I_{DM}	-60	
Avalanche Current [C]		I_{AR}	-26	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	33.8	mJ
Power Dissipation [B]	T_C=25°C	P_D	60	W
	T_C=100°C		30	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16.7	25	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		40	50	°C/W
Maximum Junction-to-Case [C]	Steady-State	$R_{\theta JC}$	1.9	2.5	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS}=0V		-0.003	-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.2	-1.9	-2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-20A		32	40	mΩ
		T_J=125°C		53		
		V_{GS}=-4.5V, I_D=-20A		43	55	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A		32		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.73	-1	V
I_S	Maximum Body-Diode Continuous Current				-30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-30V, f=1MHz		2977	3600	pF
C_{oss}	Output Capacitance			241		pF
C_{rss}	Reverse Transfer Capacitance			153		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2	2.4	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-30V, I_D=-20A		44	54	nC
Q_g(4.5V)	Total Gate Charge			22.2	28	nC
Q_{gs}	Gate Source Charge			9		nC
Q_{gd}	Gate Drain Charge			10		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-30V, R_L=1.5Ω, R_{GEN}=3Ω		12		ns
t_r	Turn-On Rise Time			14.5		ns
$t_{D(off)}$	Turn-Off DelayTime			38		ns
t_f	Turn-Off Fall Time			15		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=100A/µs		40	50	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=100A/µs		59		nC

A: The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T $_A$ =25°C. The Power dissipation PDSM is based on R $_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB allows it.

B. The power dissipation PD is based on T $_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T $_{J(MAX)}$=175°C.

D. The R $_{\theta JA}$ is the sum of the thermal impedence from junction to case R qJC and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T $_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T $_A$=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1 ST 2008).

Rev 5: Jan 2011

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

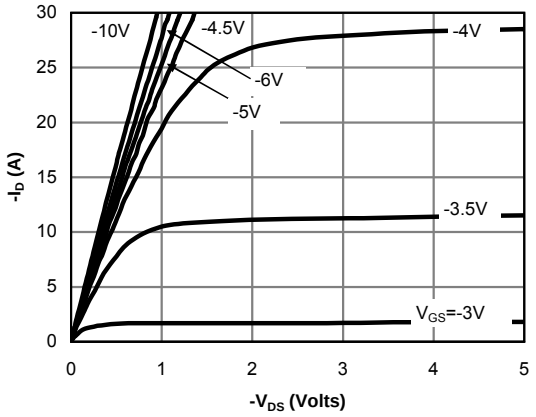


Fig 1: On-Region Characteristics

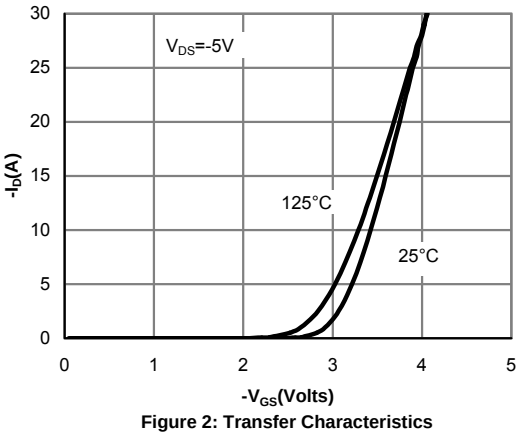


Figure 2: Transfer Characteristics

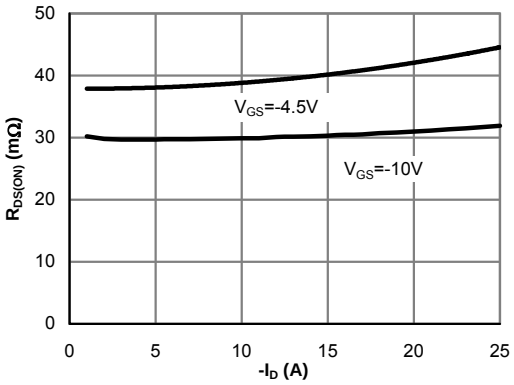


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

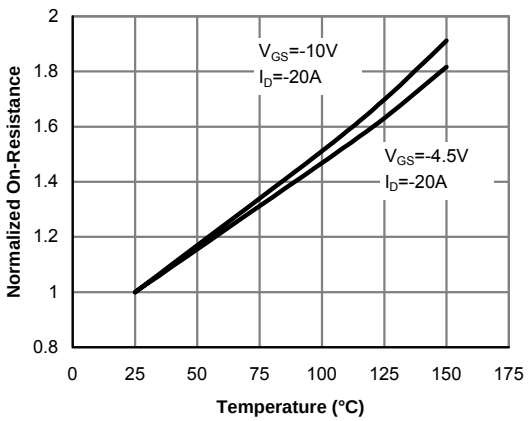


Figure 4: On-Resistance vs. Junction Temperature

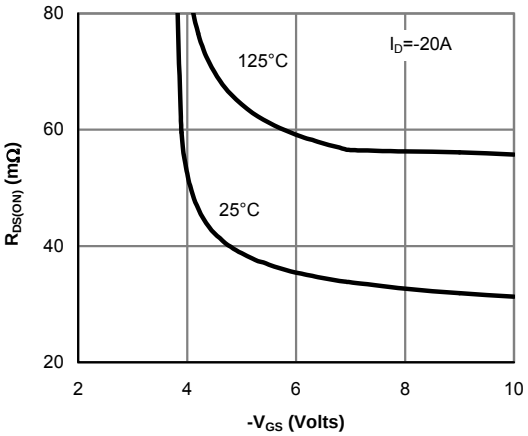


Figure 5: On-Resistance vs. Gate-Source Voltage

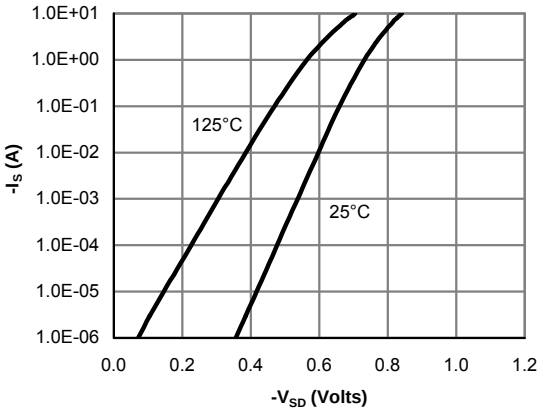


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

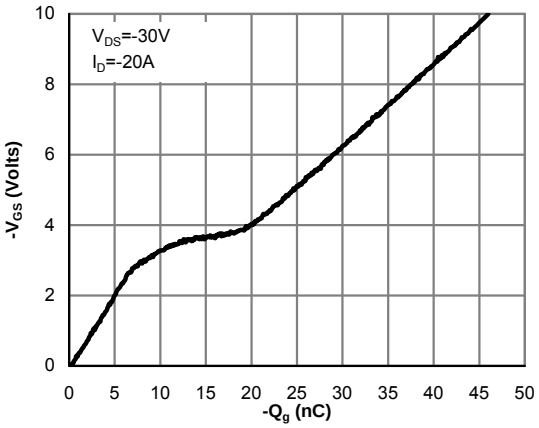


Figure 7: Gate-Charge Characteristics

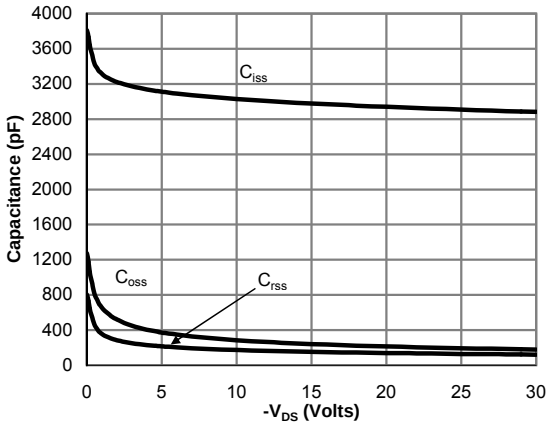


Figure 8: Capacitance Characteristics

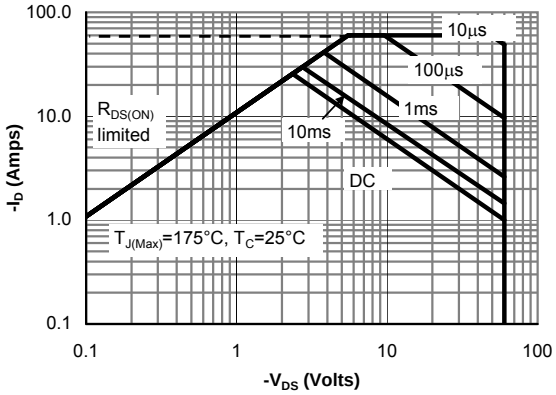


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

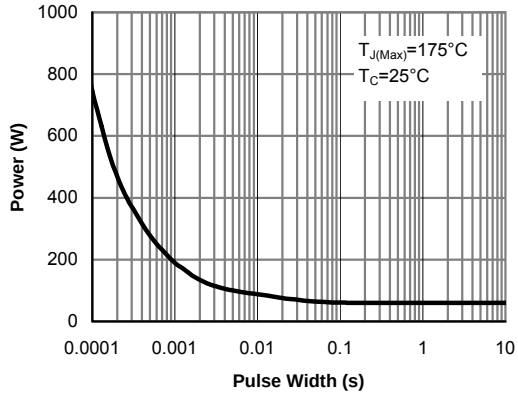


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

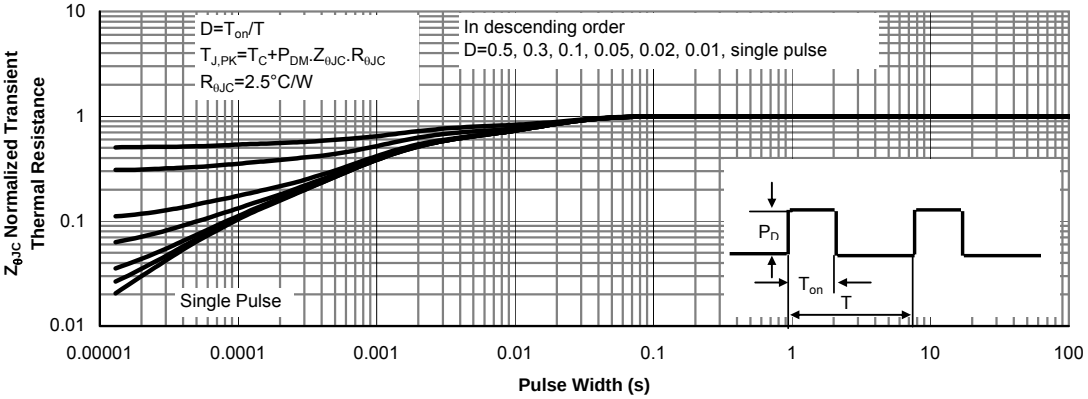


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

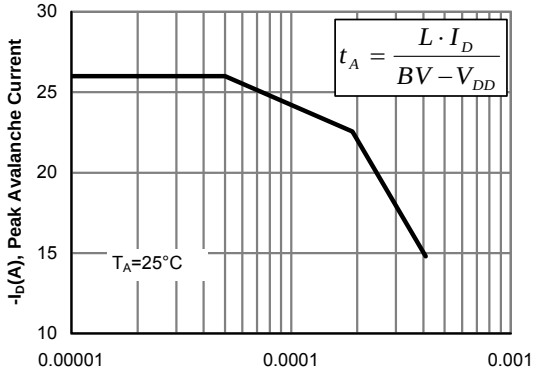


Figure 12: Single Pulse Avalanche capability

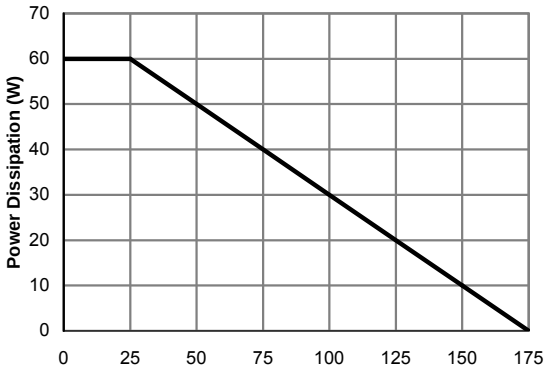


Figure 13: Power De-rating (Note B)

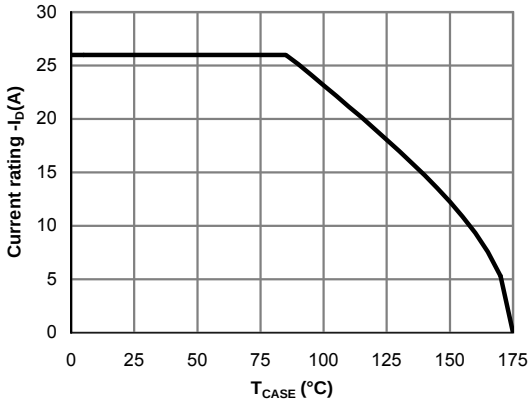


Figure 14: Current De-rating (Note B)

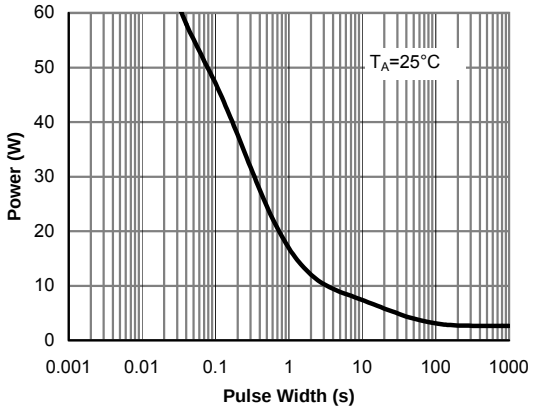


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

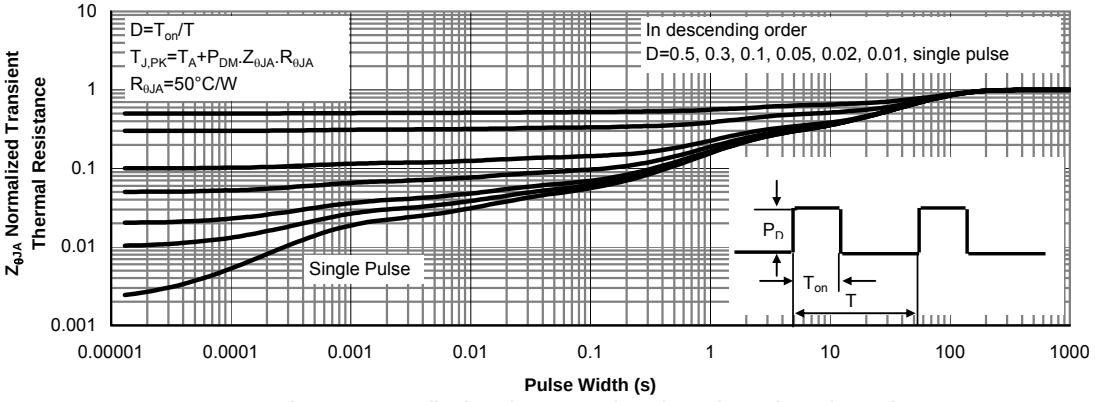
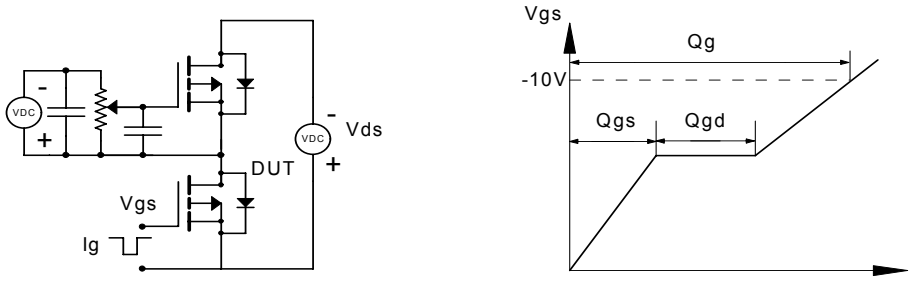
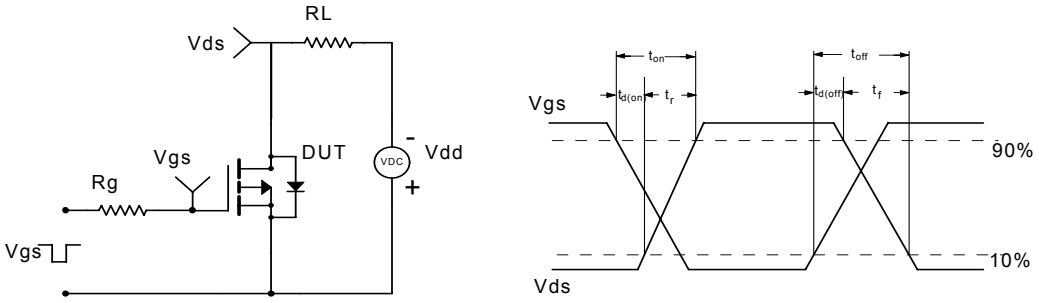


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

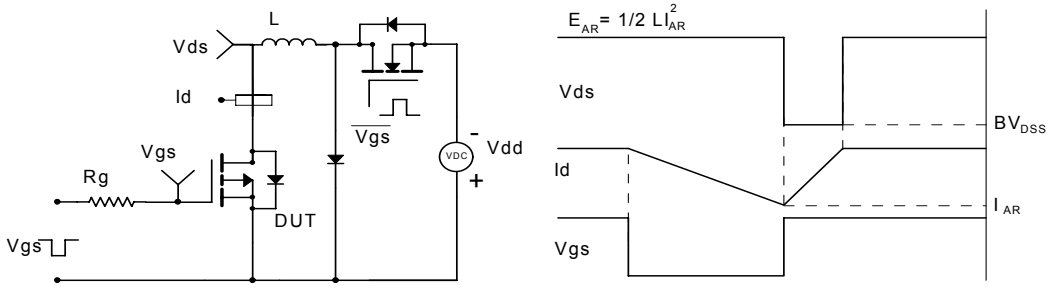
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms